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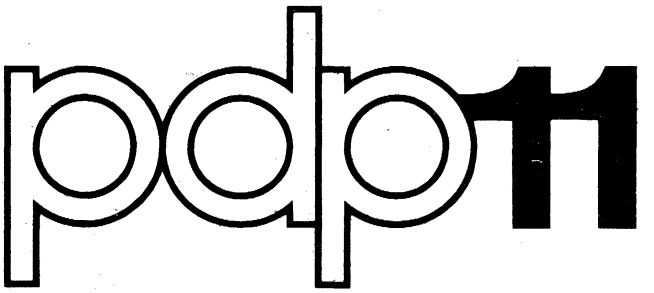

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CHAPTER 1

INTRODUCTION

1.1 GENERAL

The PDP-11 family is a comprehensive set of hardware/software facilities that includes several computers, a large number of peripheral devices and options, and extensive software. New systems will be compatible with existing family members. The user can choose the system which is most suitable for his application, but as needs change or grow he can easily add or change equipment.

Some of the characteristics of PDP-11 equipment are:

- 16-bit word (two 8-bit bytes)
  direct addressing of 32K 16-bit words or 64K 8-bit bytes (K = 1024)
- Word or byte processing
  central processors are hardwired for word and byte instructions
- Asynchronous operation
  systems run at their highest possible speed, replacement with faster devices means faster operation with no other hardware or software changes
- Modular component design
  extreme ease and flexibility in configuring systems
- Direct Memory Access (DMA)
  inherent in the architecture is direct memory access for multiple devices
- Automatic Priority Interrupt
  four-line, multi-level system permits grouping of interrupt lines according to response requirements
- Vectored interrupts
  fast interrupt response without device polling
- Power Fail & Automatic Restart
  hardware detection and software protection for fluctuations in the AC power

1.2 SCOPE AND CONTENTS

This Handbook is intended to be a reference for PDP-11 equipment, other than central processors. Descriptions, specifications, programming, and interfacing information is presented on the PDP-11 peripherals and options.

Peripherals

Programming	(chapter 2)
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Programming

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1.3 REFERENCES

The information in the Handbook supplements material found in:

PDP-11 Processor Handbook

Processor Handbooks are available for the various PDP-11 computers. Familiarity with or access to such a Handbook would greatly facilitate an understanding of the material in this Handbook. However, some introductory PDP-11 information is included in this Handbook.

1.4 PERIPHERALS

Digital Equipment Corporation designs and manufactures many of the peripheral devices offered with PDP-11's. As a designer and manufacturer of peripherals, Digital can offer extremely reliable equipment, lower prices, more choice and quantity discounts.

1.5 UNIBUS

All computer system components and peripherals connect to and communicate with each other on a single high-speed bus known as the UNIBUS, see Figure 1-1.

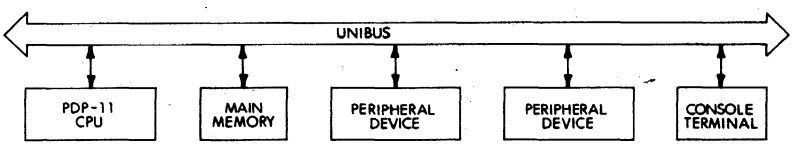


Figure 1-1 PDP-11 System Block Diagram

The form of communication is the same for every device on the UNIBUS. The central processing unit (CPU) uses the same set of signals to communicate with main memory as with peripheral devices. Peripheral de-

vices also use this set of signals when communicating with the processor, memory or other peripheral devices. Each device, including memory locations, processor registers, and peripheral device registers, is assigned an address on the UNIBUS.

With bidirectional and asynchronous communications on the UNIBUS, devices can send, receive, and exchange data with minimum processor intervention. Because it is asynchronous, the UNIBUS is compatible with devices operating over a wide range of speeds. Interfaces to the UNIBUS are not time dependent; there are no pulse-width or rise-time restrictions.

Full 16-bit words or 8-bit bytes of information can be transferred on the bus. The information can be instructions, addresses, or data. Direct data transfers can occur between a peripheral device control and memory.

Refer to Chapter 5 for more detailed information about the UNIBUS and data transfers.

1.6 CENTRAL PROCESSOR

The central processor, connected to the UNIBUS as a subsystem, controls the time allocation of the UNIBUS for peripherals and performs arithmetic and logic operations and instruction decoding. It contains multiple high-speed general-purpose registers which can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between input/output (I/O) devices and memory without disturbing the processor registers; does both single- and double-operand addressing and handles both 16-bit word and 8-bit byte data.

Instruction Set

The instruction complement uses the flexibility of the general-purpose registers to provide over 400 powerful hard-wired instructions. Unlike conventional 16-bit computers, which usually have three classes of instructions (memory reference instructions, operate or control instructions and I/O instructions) all operations in the PDP-11 are accomplished with one set of instructions. Since peripheral device registers can be manipulated as flexibly as core memory by the central processor, instructions that are used to manipulate data in core memory may be used equally well for data in peripheral device registers.

1.7 SOFTWARE

The PDP-11 family of central processors and peripherals is supported by a comprehensive set of operating system software which allows the user to efficiently program his applications. System software is available to support small stand-alone configurations, disk based real-time and program development systems, and large scale multiprogramming and time-sharing systems. Some examples are:

- PAPER TAPE SYSTEM—Core only high speed paper tape configuration with program development in assembly language. Editor, debugger, and linker are supplied along with a relocating assembler.
- CASSETTE PROGRAMMING SYSTEM (CAPS-11)—Monitor based system with cassettes as a file structured medium. Interrupt driven program development system with relocating assembler, linker, editor,

debugger and peripheral interchange program. Can support BASIC as a higher level language processor.

- REAL TIME SINGLE USER SYSTEM (RT-11)—DECtape or DECpack disk based system for real time and program development. Features MACRO assembler, linker, editor, debugger, and peripheral interchange program. Supports BASIC with real time extensions as a higher level language.
- DISK BASED BATCH OPERATING SYSTEM (DOS/BATCH-11)—Disk based system with support for a full line of PDP-11 peripherals. Features interactive or BATCH mode of operation, sophisticated file handling and protection, powerful and flexible command language. Contains MACRO, editor, debugger, linker, librarian, peripheral interchange package, and file utility programs. Supports a powerful FORTRAN IV language processor and scientific package.
- ADVANCED REAL-TIME OPERATING SYSTEM (RSX-11D)—Modular disk based hardware protected multiprogramming systems featuring concurrent multiple real-time task execution and BATCH program development. Contains MACRO, editor, debugger, task builder, librarian, utilities and FORTRAN IV with real-time extensions.
- RESOURCE TIME SHARING SYSTEM (RSTS/E)—Disk based time sharing implementing BASIC-PLUS language, an enriched version of BASIC. Up to 32 simultaneous users via interactive terminals and sharing of system resources with spooling features. Complete file security and manipulation through utilities.

1.8 PDP-11 WORD

The 16-bit PDP-11 word can be represented conveniently as a 6-digit octal word. Bit 15, the Most Significant Bit (MSB), is used directly as the Most Significant Digit of the octal word. The other 5 octal digits are formed from the corresponding groups of 3 bits in the binary word. See Figure 1-2.

Octal Representation

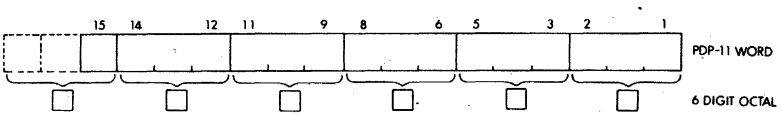


Figure 1-2

When an extended address of 18 bits is used (shown later in the Handbook), the Most Significant Digit of the octal word is formed from bits 17, 16, and 15. For unsigned numbers, the correspondence between decimal and octal is:

Decimal	Octal	
0	000 000	
$(2^{16}-1)=$ 65,535	177 777	(16-bit limit)
$(2^{18}-1)=$262,143	777 777	(18-bit limit)

CHAPTER 2

PROGRAMMING

2.1 GENERAL

Programming of peripherals is extremely simple in the PDP-11; a special class of instruction to deal with input/output operations is unnecessary. The UNIBUS permits a unified addressing structure in which control, status, and data registers for peripheral devices are directly addressed as memory locations. Therefore all operations on these registers, such as transferring information into or out of them or manipulating data within them, are performed by normal memory reference instructions.

The use of all memory reference instructions on peripheral device registers greatly increases the flexibility of input/output programming. For example, information in a device register can be compared directly with a value and a branch made on the result.

All peripheral device registers can be treated as accumulators. There is no need to funnel all data transfers, arithmetic operations, and comparisons through a single or small number of accumulator registers.

NOTE

A summary of the PDP-11 instruction set is contained in Appendix C. A brief description of the PDP-11 Assembly language is provided in Appendix D. Programming examples used throughout this Handbook are in Assembly language.

2.2 ADDRESSES

Words and Bytes

Since the PDP-11 can operate on individual 8-bit bytes, a 16-bit word allows addressing 65,536 bytes ($2^{16} = 65{,}536$). It is common to refer to this as 64K, where K is equal to 1,024. Thus 64K bytes, or 32K 16-bit words are directly addressable. Actually in the PDP-11, the top 4K addresses are reserved for internal CPU registers and external input/output (I/O) registers. If all of the memory space were used, there could be 28K words of physical memory plus 4K locations for the CPU and I/O registers.

A PDP-11 word is divided into a high byte and a low byte as shown in Figure 2-1.

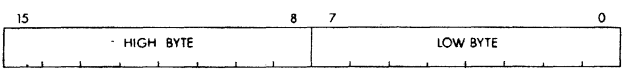


Figure 2-1 PDP-11 Word

Low bytes are stored at even numbered memory locations and high bytes are stored at odd numbered locations. Words always start at even numbered locations.

Expanded Addressing
With the larger PDP-11 computers, expansion above 28K of memory can be achieved by using the Memory Management option. Memory Management provides an 18-bit effective memory address which permits addressing up to 124K words of actual memory.

If the Memory Management option is not used, an octal address between 160 000 and 177 777 is interpreted as 760 000 to 777 777. That is, if bits 15, 14, and 13 are 1's, then bits 17 and 16 (the extended address bits) are considered to be 1's, which relocate the last 4K words (8K bytes) to become the highest locations accessed by the UNIBUS.

2.3 DEVICE REGISTERS

All peripheral devices are specified by a set of registers which are addressed as main memory. There are two types of registers associated with each device:

a) Control and status
b) Data buffer

Control and Status Registers
Each peripheral has one or more control and status registers that contain all the information necessary to communicate with that device. The general form, shown in Figure 2-2 does not necessarily apply to every device, but is presented as a guide.

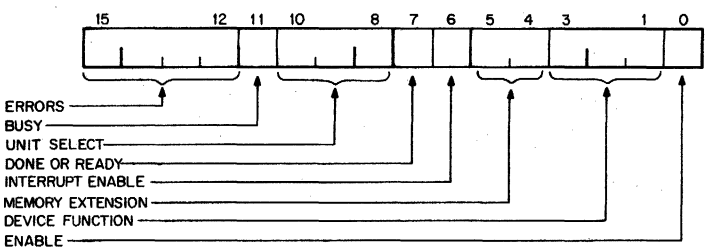


Figure 2-2 Control & Status Register

Many devices require less than 16 status bits. Other devices will require more than 16 bits and therefore will require additional status and control registers.

The bits in the control and status registers are generally assigned as follows:

BIT	NAME	FUNCTION
15-12	Errors	Generally there is an individual bit associated with a specific error. When more bits are required for errors, they can be obtained by expanding the error section in the word or by using another status word. Generally Bit 15 is the inclusive OR of all

		other error bits (if there is more than one). Most devices will have "hard" error conditions which will cause an interrupt if bit 6 is set. Some may also have "soft" errors (warning types) which do not cause immediate interrupts. All errors are generally indicated by individual status bits.
11	Busy	Set to indicate that a device operation is being performed.
10-8	Unit Select	Some peripheral systems have more than one device per control. For example, a disk system can have multiple surfaces per control and an analog-to-digital converter can have multiple channels. The unit bits select the proper surface or channel.
7	Done or Ready	The register can contain a Done bit, a Ready bit or a Done-Busy pair of bits, depending on the device. These bits are set and cleared by the peripheral device, but may be queried by the program to determine the availability of the device.
6	Interrupt Enable	Set by the program to allow an interrupt to occur as a result of a function done or error condition.
5-4	Memory Extension	Allows devices to use a full 18 bits to specify addresses on the bus.
3-1	Device Function Bits	Specifies the operation that a device is to perform.
0	Enable	Set to enable the device to perform an operation.

Data Buffer Registers
The data buffer register is used for temporarily storing data to be transferred into or out of the computer. The number and type of data registers is a function of the device.

2.4 PROCESSOR REGISTERS

2.4.1 General Registers
The central processor contains 8 general registers which can be used for a variety of purposes. The registers can be used as accumulators, index registers, auto-increment registers, auto-decrement registers, or as stack pointers for temporary storage of data. Arithmetic operations can be from one general register to another, from one memory or device register to another, or between memory or a device register and a general register. Refer to Figure 2-3.

R7 is used as the program counter (PC) and contains the address of the next instruction to be executed. It is a general register normally used only for addressing purposes and not as an accumulator for arithmetic operations.

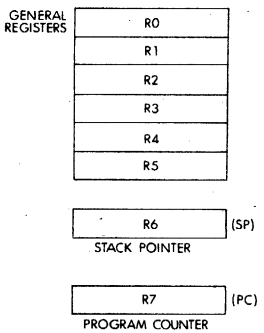


Figure 2-3 General Registers

The R6 register is normally used as the Stack Pointer indicating the last entry in the appropriate stack (a common temporary storage area with "Last-in First-Out" characteristics).

2.4.2 Processor Status Word (PS) 777 776

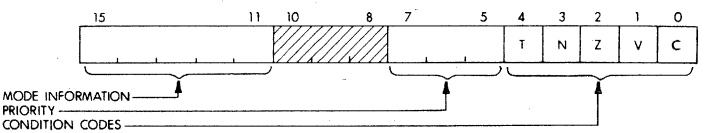


Figure 2-4 Processor Status Word

The Processor Status word, at location 777776, contains information on the current status of the computer. This information includes the condition codes describing the results of the last instruction; and an indicator for detecting the execution of an instruction to be trapped during program debugging, see Figure 2-4.

Bits 15 to 11 are used in the larger PDP-11 computers for operational mode information, and will not be covered in this Handbook. Refer to the 11/40 or 11/45 Handbooks for further information.

Processor Priority

The central processor operates at any one of eight levels of priority, 0-7. When the CPU is operating at level 7 an external device cannot interrupt it with a request for service. The central processor must be operating at a lower priority than the external device's request in order for the interruption to take effect. The current priority is maintained in the Processor Status word (bits 7-5), with bit 5 being the LSB. The 8 processor levels provide an effective interrupt mask.

Condition Codes
The condition codes contain information on the result of the last CPU operation.

The bits are set as follows:

Z = 1, if the result was zero
N = 1, if the result was negative
C = 1, if the operation resulted in a carry from the MSB
V = 1, if the operation resulted in an arithmetic overflow

Trap
The trap bit (T) can be set or cleared under program control. When set, a processor trap will occur through location 14 on completion of instruction execution and a new Processor Status word will be loaded. This bit is especially useful for debugging programs as it provides an efficient method of installing breakpoints.

2.5 INTERRUPT STRUCTURE

If the appropriate Interrupt Enable bit is set in the control and status register of a device, transition from 0 to 1 of the Ready or Error bit causes an interrupt request to be issued to the processor. Also if Ready or Error is a 1 when the Interrupt Enable is turned on, an interrupt request is made. If the device makes the request at a priority greater than that at which the processor is running and no other conflicts exist, the request is granted and the interrupt sequence takes place:

a) the current program counter (PC) and processor status (PS) are pushed onto the processor stack;

b) the new PC and PS are loaded from a pair of locations (the interrupt vector) in addressed memory, unique to the interrupting device.

Since each device has a unique interrupt vector which dispatches control to the appropriate interrupt handling routine immediately, no device polling is required. Furthermore, since the PS contains the processor priority, the priority at which an interrupt request is serviced can be set under program control and is independent of the priority of the interrupt request. The Return from Interrupt Instruction is used to reverse the action of the interrupt sequence. The top two words on the stack are popped into the PC and PS, returning control to the interrupted sequence.

2.6 PROGRAMMING WITH DEVICE REGISTERS

The diagram of Figure 2-5 shows 4 bits that would appear in many common Command and Status registers.

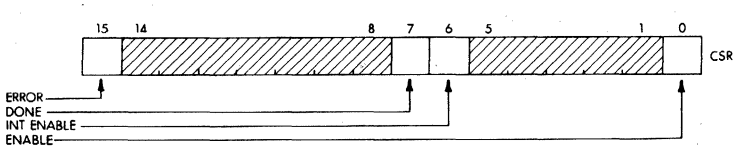


Figure 2-5 CSR Register

BIT	NAME	FUNCTION
15	Error	Set when an error occurs.
7	Done	Set when the device is either ready to accept new information, or has completed an operation and has data available.
6	Interrupt Enable (INT ENBL)	When set, an interrupt will be requested when Done or Error becomes a 1.
1	Device Enable (ENBL)	Set to allow the peripheral device to perform a function.

The diagram of Figure 2-6 shows a typical data buffer that can hold an 8-bit character.

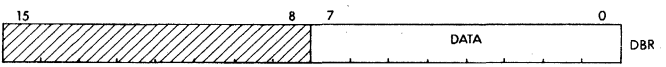


Figure 2-6 DBR Register

BIT	NAME	FUNCTION
7-0	Data	Holds the ASCII code for a character to be either written to or read from the peripheral device.

In the following examples, these two registers will be referred to by the symbolic designations, CSR and DBR.

Example: Transfer information from the peripheral data buffer to general register R3.

```
MOV DBR, R3
```

Since the information is only 8 bits, and it resides in the low part of the DBR, the byte instruction would accomplish the same purpose;

```
MOVB DBR, R3
```

The bit manipulating instructions,

BIT (bit test), set condition codes N & Z according to an AND operation on corresponding bits; neither source nor destination are modified.

BIC (bit clear), put 0's in all positions of the destination that correspond to a 1 in the source.

BIS (bit set), put 1's in all positions of the destination that correspond to a 1 in the source (OR operation).

can be used to conveniently modify or test the contents of the CSR register.

Example: Enable the peripheral device to perform an I/O function:

```
BIS #1, CSR    ; OR CODE 000 001 WITH THE CSR
```

This instruction will set bit 0 of the CSR, but leave all other bits unchanged.

Example: Test for an error, and branch to an error handling routine if there is an error.

```
TST CSR      ;SET CONDITION CODE BITS ON CONTENTS OF CSR
BMI ERRTN    ;TEST BIT 15, BRANCH ON MINUS
```

ERRTN means the address of the error routine. When there is an error, bit 15 = 1, the CSR looks like a negative number (sign bit = 1).

Example: Test to see if the peripheral device has performed a read function, and data is available. Transfer to a read subroutine if data is available.

```
BIT #200, CSR      ;TEST BIT 7 OF THE CSR
BNE SBR            ;BRANCH IF DONE IS SET
```

The CSR register is ANDed with a word of all 0's except for bit 7. If bit 7 (DONE) of the CSR is a 1, the result is not zero, and a branch on not equal to 0 can be made to a service subroutine (SBR).

Example: Prevent the peripheral device from causing an interrupt.

```
BIC #100, CSR          ;CLEAR THE INT ENBL BIT
```

Using a source of 000 100 has the effect of clearing bit 6 (INT ENBL), but leaving all other bits of the CSR alone.

Example: Have the program continuously check the DONE bit, and read a word when it becomes a 1.

```
AGAIN:  TSTB CSR      ;TEST BIT 7, SIGN BIT
        BPL AGAIN     ;BRANCH IF NOT SET
        MOVB DBR, R0  ;TRANSFER DATA TO CPU
```

Bit 7 of the CSR is conveniently the sign bit for the low order byte, and can be tested directly by a single instruction.

2.7 DEVICE PRIORITY

Each peripheral has a priority level assigned to it by hardware, allowing it to interrupt lower priority level devices. To ensure that the CPU which executes the peripheral's service routine is not incorrectly interrupted, the CPU itself must take on the priority level of the interrupting peripheral (Level 4, 5, 6, or 7) while running the service routine, see Figure 2-7.

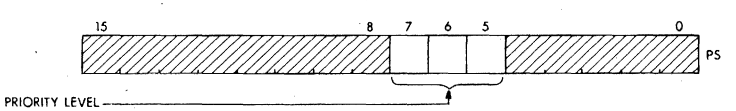


Figure 2-7 Processor Status Word

Example: Write a program to service the input keyboard data (register KBB) from the LA30 DECwriter. The interrupt vector is at location 60, and the priority level is 4.

```
        . = 60
        .WORD KBSBR    ;PC = KEYBOARD SUBR ADDRESS
        . WORD 200     ;PS = 4 (BITS 7, 6, 5, = 100)
KBSBR;  MOV KBB, R1
        RTI
```

Example: Set the priority level of the processor to level 3.

```
PS = 777776    ;ADDRESS OF PROC STATUS WORD
CLR PS         ;START WITH ALL 0's
BIS #140, PS   ;SET BITS 6 & 5, PS = 3
```

Example: A paper tape reader interrupt service could appear as follows: First the user must initialize the service routine by specifying an address pointer and a word count

```
INIT:  MOV #BUFADR,POINTR   ;SET ADDRESS POINTER
       MOV #COUNT,COUNTR    ;SET COUNTER
       MOV #101,PRS         ;ENABLE READER PROGRAM TO CON-
                            ;TINUE UNTIL INTERRUPT
```

When the interrupt occurs and is acknowledged, the processor stores the current PC and PS on the stack. Next it goes to the interrupt vector and picks up the new PC and PS beginning at location 70. When the program was loaded the address of PRSER, the PR service routine, would be put in location 70 and 200_8 in 72 (to set priority at 4). The next instruction executed is the first instruction of PRSER.

```
PRSER:  TST PRS             ;TEST FOR ERROR
        BMI ERROR           ;BRANCH IF BIT 15 SET
        MOVB PRB,@POINTR    ;MOVE CHARACTER TO BUFFER
        INC POINTR          ;INCREMENT POINTER
        DEC COUNTR          ;DECREMENT CHARACTER COUNT
        BEQ DONE            ;BRANCH WHEN INPUT DONE
        INC PRS             ;START READER FOR NEXT CHARAC-
                            ;TER
DONE:   RTI                 ;RETURN TO INTERRUPTED PRO-
                            ;GRAM
```

CHAPTER 3

CATEGORIES OF PERIPHERALS

3.1 GENERAL

This chapter contatins general information and comparisons of the PDP-11 peripherals. Sometimes a peripheral will fall into more than one category, and it will be listed wherever applicable.

This chapter shows the broad range of peripheral equipment offered and the wide span of equipment capabilities. Some of them are compared below.

Comparison of Input Equipment

MEDIUM	PRODUCT	INPUT SPEED (max)
Paper tape	Teletype, LT33	10 characters/sec
	High speed reader/punch, PC11	300
Cards	Card reader, CD11	1,600
Magnetic tape	Cassette, TA11	560
	DECtape, TC11	10,000
	Magtape, TM11	36,000

Comparison of Output Equipment

MEDIUM	PRODUCT	OUTPUT SPEED (max)
Paper tape	Teletype, LT33	10 characters/sec
	High speed reader/punch, PC11	50
Printer	Teletype, LT33	10
	DECwriter, LA30	30
	Line printer, LP11	2,600
CRT terminal	Alphanumeric terminal, VT05	240
	Graphic terminal, GT40	960
Magnetic tape	Cassette, TA11	560
	DECtape, TC11	10,000
	Magtape, TM11	36,000

3.2 MAIN MEMORY

3.2.1 General

Memories with different ranges of speeds and various physical and electrical characteristics can be freely mixed and interchanged within a PDP-11 system. Memory is treated as a physically modular, but electrically integral part of the computing system.

Types of Memory
Core, semiconductor, and read only memory (ROM) is offered for PDP-11 systems. Although semiconductor memory (MOS and bipolar) can be used only with the PDP-11/45, all other memories can be used with any PDP-11 Central Processing Unit.

Parity is an available option for both core and semiconductor memory. No increase in mounting space is required.

Operating Speed
The CPU can begin processing data immediately after accessing it. (Access time is defined as the time interval between request and when the data is available.) Core memory then rewrites itself while the processor is working. (Semiconductor memory contents are not destroyed on read-out.) This makes the access time the important operating parameter for the PDP-11, thus providing increased speed and efficiency. The only effect cycle time has on the PDP-11 is the time needed between successive transfers to memory.

Packaging
Memory is offered as a complete system, including control and interfacing logic, interconnecting cables, and mounting assembly. Several of the PDP-11 processors have dedicated, pre-wired areas within the chassis for holding additional memory. In other cases, memory can be added within the CPU mounting assembly, and the necessary power taken from the cabinet power supplies. A separate, self-contained memory unit is available that includes its own power supply and rack-mountable assembly unit.

Modes of Operation
Read (DATI)—A complete memory cycle is performed, and the contents of core are restored after being read. Transfer is Data In (to the UNIBUS or the CPU). In the master-slave relationship on the bus, memory is always the slave.

Read/Pause (DATIP)—Split cycle operation. Data read from core is not restored because new data is to be entered. This operation must be followed by a write cycle (DATO or DATOB) to the accessed location.

Write (DATO)—A full 16-bit word is loaded into memory. Transfer is Data Out (from the UNIBUS or the CPU).

Write Byte (DATOB)—An 8-bit byte is loaded; otherwise it is the same operation as DATO.

3.2.2 Products

MODEL	DESCRIPTION	ACCESS TIME	CYCLE TIME
MM11	Core memory	360 nsec	900 nsec
MS11-B	MOS memory	350	450
MS11-C	Bipolar memory	200	300
BM792	Read only memory	100	—

3.3 TERMINALS

Characteristics and Applications

a) convenient human interface to the computer
b) typewriter-like keyboard for data entry
c) printer or display for output from computer
d) basic input/output device
e) can be local (console terminal), or remote

Products

MODEL	DESCRIPTION	OUTPUT SPEED (max)
LT33	Teletype	10 characters/sec
LA30	DECwriter	30
VT05	Alphanumeric	240
GT40	Graphic display system (includes a computer)	960 char/sec as a simple serial interfaced terminal, operation can be faster as a synchronous device

3.4 PAPER TAPE

Characteristics and Applications

a) simple medium to use
b) separate tapes for individual programs
c) variable program length
d) data can be read by a person

Products

MODEL	DESCRIPTION	READ SPEED	PUNCH SPEED
LT33	Teletype terminal	10 char/sec	10 char/sec
PC11	Paper tape reader/punch	300	50
PR11	Paper tape reader	300	—

3.5 CARDS

Characteristics and Applications

a) individual records
b) easy to add, delete, or rearrange a card
c) possible to print on the card
d) can be read by a person

Products

MODEL	DESCRIPTION	TYPE	READ SPEED
CM11	Card reader	mark-sense or punch	285 cards/min
CR11	Card reader	punch	300
CD11	Card reader	punch	1200

3.6 PRINTERS

Characteristics and Applications

a) hard copy for permanent records
b) impact types can make multiple copies
c) some plotting capability

Products

MODEL	DESCRIPTION	TYPE	PRINT SPEED	COLUMNS	CHAR.
LT33	Teletype	impact	10 char/sec	64	64
LA30	DECwriter	impact	30 char/sec	80	64
LS11	Line printer	impact	60 lines/min	132	62
LP11	Line printer	impact	170 to 1200 lines/min	80 or 132	64 or 96
LV11	Printer/plotter	electro-static	500 lines/min	132	96

3.7 MAGNETIC TAPE

Characteristics and Applications

a) unlimited off-line storage
b) removable medium

Products

MODEL	DESCRIPTION	STORAGE/REEL	DATA RATE
TA11	Cassette	90,000 char	560 char/sec
TC11/TU56	DECtape	255,000	10,000
TM11/TU10	Magnetic tape (industry compatible)	20,000,000	36,000

3.8 DISKS

Characteristics and Applications

a) fast access to on-line storage
b) swapping programs
c) virtual memory
d) efficient bulk storage

a) Fixed Head—fast access time
b) Moving head—high storage capacity, more economical storage
c) Disk pack—removable medium, unlimited off-line storage

The average access time (avg latency) is equal to ½ the time for a revolution plus the average head positioning time (for moving head disks only).

Products

MODEL	DESCRIPTION	CAPACITY/ DRIVE	AV ACCESS TIME	DATA RATE
RC11/RS64	Fixed head disk	64 K words	17 msec	16 μsec/word
RF11/RS11	Fixed head disk	256 K	17	16
RK11/RK05	Disk cartridge	1.2 million	70	11
RP11/RP03	Disk pack	20 million	42	7.5

3.9 DISPLAYS

Characteristics and Applications

a) pleasing human interface
b) soft copy of information
c) fast presentation of information
d) alphanumeric and graphic capability

Products

MODEL	DESCRIPTION
VR01	Oscilloscope
VR14	Point plot display
VT01	Storage display
VT05	Alphanumeric terminal
GT40	Graphic display system (includes a computer)

3.10 COMMUNICATIONS OPTIONS

Characteristics and Applications

Asynchronous Interfaces—Character transmission time is variable, but bits within the character are timed; a character transmission normally includes a start bit, several data bits, one or more stop bits, and an optional parity bit.

Synchronous Interfaces—Continuous data stream once the receiver is synchronized; data is generally transmitted in message blocks containing both information and timing signals.

Other Communications Options—Provide error detection, autocalling unit interfacing, and signal conditioning.

Products

MODEL	DESCRIPTION	TYPICAL USE
DL11	Single Asynchronous Line Interface	Connects PDP-11 to local terminals (such as Teletype, LA30 and VT05) or to remote terminals via modems.
DC11	Dual Asynchronous Line Interface (Programmable)	Connects PDP-11 to remote terminals via modems. Transmission speed and other parameters may be changed by software.
DJ11	16-Line Asynchronous Multiplexer	Connects PDP-11 to up to 16-local terminals or up to 16-remote terminals via modems. Transmission speeds and other parameters are switch or jumper selectable in 4-line groups.
DH11	16-Line Programmable Asynchronous Multiplexer	Connects PDP-11 to up to 16-local terminals or remote terminals. Transmissions speeds and parameters are programmable.

DP11	Single Line Asynchronous Interface	Connects PDP-11 to modems or communications for high speed transmissions. Can be used in computer-to-computer communications.
KG11	Communication Arithmetic Element	Used to detect errors in serially transmitted data.
DC08 and H316	Telegraph Line Interfaces	Connect PDP-11 to telegraph equipment.
DF11	Signal Conditioning Options	Convert computer (TTL) signals to EIA or 20 ma signals. Can be used with DC11, DL11 and DH11 interfaces.
DF11-B	Integral Modems	Convert TTL signals to audio frequencies. Used to connect PDP-11 directly to Bell Data Access Arrangement options.
DF01	Acoustic Coupler	Connects terminal (VT05, LA30) to standard telephone for communication with computer via phone lines.
H313-A	Voltage Current Adapter	Converts Digital supplied TTY output for use with Bell 103 modems or equivalent.
H312-A	Null Modem	Allows direct connection of a terminal with an EIA cable to a DC11, DP11, DL11, or DM11-DB.

3.11 DATA ACQUISITION

Characteristics and Applications

a) analog conversion equipment
b) analog circuitry
c) digital control and monitoring
d) timing control
e) laboratory experimentation
f) industrial control

Products

MODEL	DESCRIPTION
AA11	Digital-to-analog conversion subsystem, 12 bits
AD01	Analog-to-digital conversion subsystem, 10 or 11 bits

LPS11	Lab Peripheral System, 12 bits (A/D, real time clock, D/A, digital I/O)
AFC11	Low level analog input subsystem, flying capacitor scanner
UDC11	Digital control subsystem
KW11-L	Line clock
KW11-P	Programmable clock

3.12 UNIBUS EQUIPMENT

MODEL	DESCRIPTION
DR11-C	General device interface (program interrupts)
DR11-B	Direct Memory Access interface (NPR data transfers)
DT03	UNIBUS switch
DA11-B	UNIBUS link
DA11-F	UNIBUS window

3.13 MOUNTING EQUIPMENT

MODEL	DESCRIPTION	SYSTEM UNIT SPACE
BB11	Blank mounting panel	1
DD11	Peripheral mounting panel	1
BA11-ES	Extension Mounting Box	6
H960-D	Cabinet with a drawer	9
H960-E	Cabinet with 2 drawers	18
H960-CA	Cabinet	
H961-A	Cabinet without end panels	

CHAPTER 4

DESCRIPTIONS OF PERIPHERALS

4.1 INTRODUCTION

This chapter contains detailed descriptions, specifications, programming, and operating information for PDP-11 peripheral equipment. For ease of reference, the peripherals have been arranged alphanumerically by model number, with the model number appearing on the top right-hand side of each page.

Since some peripherals have similar descriptions and specifications, related peripherals will be described within the same section. Section 4.3 contains a complete list of all equipment described in this chapter. Appendix E contains an index to all equipment described in this Handbook.

4.2 EXPLANATION OF TERMS AND SPECIFICATIONS

4.2.1 Products

All the peripherals mentioned in this chapter must eventually interface to the UNIBUS. Some of the equipment, such as Line Printers, include a control unit as well as the printer itself. The control unit, sometimes referred to as a controller or interface unit, is the actual logic equipment between the UNIBUS and the peripheral device. With terminals, the control unit and the terminal itself are separate products. In this case, several different control units could be used, depending on the application. In other cases, such as disk drives, a single model number includes a control unit and the first disk drive of the system. Other disk drives, up to the limit of the system, are specified by another model number, see Figure 4-1.

4.2.2 Registers

The device registers are shown with their common name, their mnemonic in parentheses, then their UNIBUS address. Note that these addresses begin with 77 or 76 (instead of 17 or 16) to indicate that they are in the highest 4K words of address space. Within the functional description of each bit, if not otherwise indicated, the condition or operation when the bit is set (logic 1) is described.

Some bit positions of the registers are not used (not implemented with hardware). When diagrams are shown, unused positions are indicated by cross-hatching. Some of the bits are controlled only by the peripheral device and are indicated as read only (by the program). Some of the bits are write only (by the program), and are always read as zeros. Some bits are cleared (or set) by the UNIBUS master clear signal called Initialize, which has the mnemonic INIT. It is issued by turning Power ON, Console START, or the RESET instruction. Figure 4-2 summarizes the information about the device registers.

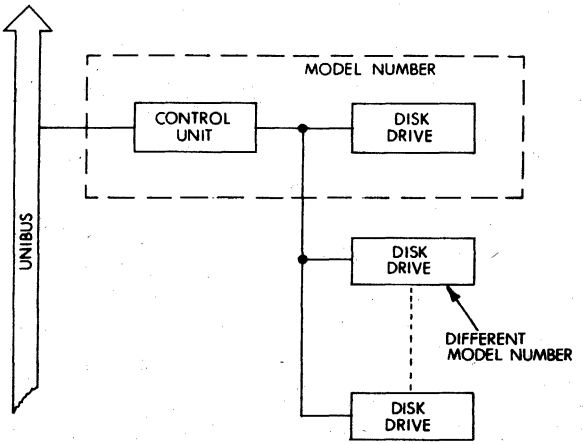
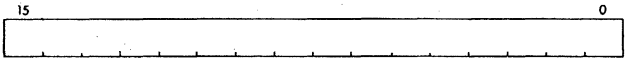


Figure 4-1. Disk Storage System

The unused or write only bits are always read as zeros by the program. Trying to load unused or read only bits has no effect on the addressed register.

Register (REG) 77x xxx



▨ = unused bit

Read only: (with respect to the CPU or bus master)—The program can monitor the bit, but cannot modify it.

Write only: (with respect to the CPU or bus master)—The program can set or clear the bit; but when reading, it will always appear to be a zero.

Figure 4-2. Device Register

4.2.3 Specifications

UNIBUS Interface

Interrupt and trap vectors are assigned to the lowest part of memory, generally in the range 000 000 to 000 377. Bus Request (BR) levels are indicated; also Non-Processor Request (NPR) operation if applicable. Most devices that interface to the UNIBUS represent only 1 bus load.

Mechanical
The mounting arrangement of the equipment is indicated as:

a) module:	plugs into a dedicated logic module slot
b) SPC:	fits in a small peripheral controller slot (quad module)
c) SU:	system unit mounting assembly is included
d) panel:	uses front panel space in a cabinet
e) table top:	suitable for placing on top of a table or a desk
f) free standing:	by itself, not in a cabinet
g) cabinet:	mounts in a standard PDP-11 cabinet

Some peripherals include 2 separate physical parts and are indicated by use of a plus (+) sign.

Relative Humidity
All humidity specifications mean without condensation.

Temperature
Correspondence between Centigrade and Fahrenheit is shown in the following table:

°C	°F
0	32
5	41
10	50
15	59
20	68
25	77
30	86
35	95
40	104
45	113
50	122
55	131

$$\left[(°C) \times \frac{9}{5}\right] + 32 = (°F)$$

4.2.4 Conversion Factors

(inches) × 2.54 = (cm)

(lbs) × 0.454 = (kg)

(Watts) × 3.41 = (BTU/hr)

4.3 LIST OF PERIPHERALS
The peripherals described in this chapter are arranged in the following sequence:

DIGITAL TO ANALOG SUBSYSTEM, AA11-D

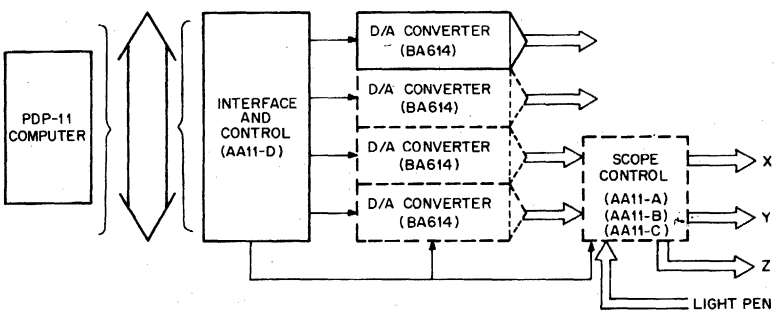
DESCRIPTION

The AA11-D is a low cost, high performance multichannel digital-to-analog conversion subsystem for PDP-11 computers.

Interfacing directly to the PDP-11 UNIBUS, the AA11-D controls up to four single buffered, 12-bit bipolar digital-to-analog converters. Each BA614 converter, which includes output amplifier and reference voltage source, is contained on a plug-in module and provides 10 ma current output at ± 10 volts. Full scale output voltage is trimpot adjustable from ± 1v to ± 10v in two ranges.

Storage scope, display scope, and light pen control options are available for the AA11-D. These options provide Z axis blanking for intensity control and require two D/A converters to control X and Y trace coordinates.

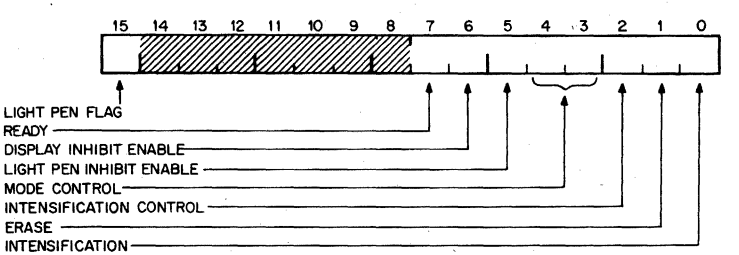
Available as a factory or field installed option, the AA11-D fully implemented with four digital to analog converters and a scope control option, is contained in a single System Unit. A rack mountable power supply is separate.



AA11-D Subsystem

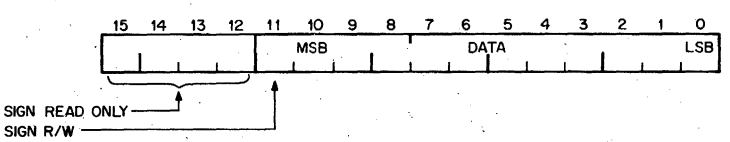
REGISTERS

Command and Status Register (CSR) 776 756



BIT	NAME	FUNCTION
15	Light Pen Flag	If bit 05 is "1," light pen flag causes interrupt. Cleared by INIT and reading the register. Read only.
7	Ready	Set when scope is ready for service, because of INTEN or ERASE commands or X or Y has been loaded. Interrupt occurs if bit 06 is "1." Bit 07 is set by INIT and cleared by displaying new point. Read only.
6	Display Inhibit Enable	Set to permit interrupts to occur when intensification or erasure is completed. This bit is set by program control and cleared by INIT. Read/Write.
5	Light Pen Inhibit Enable	Set to permit interrupts to occur when signal is received from light pen. This bit is set by program control and cleared by INIT. Read/Write.
4-3	Mode Control	Determines intensification on loading X or Y.
2	Intensification Control	Selects Stored Mode or High Intensity Mode depending on scope used. Read/Write
1	Erase	Set to erase storage scope display. Sets READY bit 7 at end of erase.
0	Intensification	Set to delay display until scope deflects to new X, Y values, then strobes intensification (Z axis) and sets READY bit 7.

Data Registers (DAC) 776 760 to 776 766
DAC1 and 2 may be used either in conjunction with the scope or for D/A channels. DAC3 and 4 may be used for additional D/A channels.



BIT	NAME	FUNCTION
15-12	Sign	Read only (2's complement)
11	Sign	Read/Write (2's complement)
10-0	Data	Read/Write.

SPECIFICATIONS FOR AA11-D

Register Addresses

Command and Status (CSR)	776 756
Data Register (DAC1)	776 760
Data Register (DAC2)	776 762
Data Register (DAC3)	776 764
Data Register (DAC4)	776 766

UNIBUS Interface

Interrupt vector address:	140, 144
Priority level:	BR4, or 5
Bus loading:	1 bus load

Mounting: 1 System Unit (SU)

Power

Input current:	0.5 A at 115 VAC 3 A at + 5 V
Heat dissipation:	60 W

Environment

Operating temperature:	10°C to 50°C
Relative humidity:	20% to 95%

Models

AA11-DA: D/A converter subsystem, 115 VAC, 60 Hz
AA11-DB: " 230 VAC, 50 Hz

SPECIFICATIONS FOR D/A CONVERTER (BA614)

Digital Input:	11 bits + sign, 2's complement code.
Digital Storage:	Single buffered.
Update Rate/Channel:	50 KHz
Analog Output Voltage:	2 continuously adjustable full scale ranges: 1v to 5v and 5v to 10v
Current:	10 ma
Gain Accuracy:	± 0.025% of full scale (25°C)
Linearity:	± 1/2 least significant bit (LSB)
Zero Offset:	Adjustable to zero
Settling Time:	20 μs max. to within ½ LSB for full scale step change (at output connector with zero capacitance loading).
Output Impedance:	Less than 1 ohm.
Temp Coefficient: (after 5 min. warmup)	± 50 μv/ °C - zero offset and ± .003%/ °C - gain accuracy

SCOPE CONTROL OPTIONS

The following scope controls each require two BA614 digital to analog converters:

AA11-A Scope Control for Tektronix 611 Storage Display Unit

Display Rate:	30 Hz (min) to 10 KHz (max)
Display Time:	deflection time 80 μs intensification time 20 μs Non-storage mode: deflection time 80 μs intensification time 2 μs
Erase Time:	0.5 sec

AA11-B Scope Control for Tektronix RM503 Oscilloscope

Display Rate:	45 KHz (max)
Display Time:	deflection time 20 μs intensification time 2 μs
Intensification: (program selectable)	two levels

AA11-C Scope Control for VR12 Point Plot Display

Display Rate/point:	40 Hz (min) to 40 KHz (max)
Display Time:	deflection time 20 μs intensification time 2 μs
Intensification: (program selectable)	two levels

ANALOG TO DIGITAL SUBSYSTEM, AD01-D

DESCRIPTION

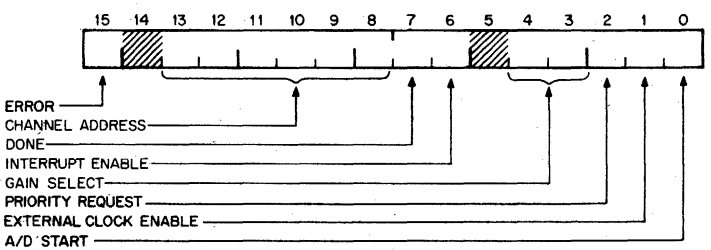
The AD01-D is a flexible, low-cost multichannel analog data acquisition option which interfaces directly to PDP-11 computers. When it is under computer or external clock control, the AD01-D provides 10-bit digitization of unipolar high-level analog signals having a nominal full-scale range of 0 to + 1.25, + 2.5, + 5.0 or + 10.0 volts. An optional sign-bit addition allows 11-bit bipolar operation. Programmable input range selection extends the AD01-D's dynamic range at moderate sampling rates to the equivalent of 13 bits for unipolar signals or 14 bits for bipolar signals.

An optional sample-and-hold amplifier reduces the conversion aperture to 100 nanoseconds.

The standard AD01-D consists of an expandable solid-state input multiplexer, programmable input range selector, A/D converter, control, and bus interface in a single 5¼-inch rack-mountable assembly plus a separate logic power supply. The multiplexer can be expanded by adding 4-channel modules up to 32 channels. An expansion multiplexer may be added to provide a maximum configuration of 64 channels.

REGISTERS

Control and Status Register (ADCS) 776 770



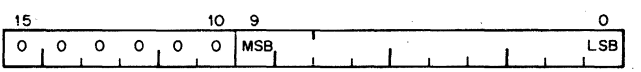
BIT	NAME	FUNCTION
15	Error	Set when a new conversion is initiated while a conversion is being performed. Interrupt is produced when interrupt bit (bit 6) is enabled.
13-8	Channel Address	Selects 1 of 32 multiplexer channels.
7	Done	Set upon completion of conversion and reset upon reading data register.
6	Interrupt Enable	Program selectable interrupt mode. Interrupt produced on A/D done (bit 7) or error (bit 15) when selected.

3-4	Gain Select	Selects input gain range of 1, 2, 4, or 8.
2	Priority Request	Program can select priority request BR7 or BR6, 5, 4.
1	External Clock Enable	Set to initiate conversion by external clock.
0	A/D Start	Set to initiate conversion by program. (Conversion is also started when a new multiplexer channel (and gain) is selected, except when external clock is enabled.)

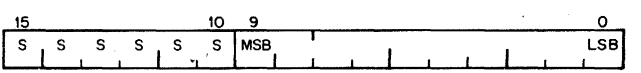
One input channel is selected by the multiplexer and connected to a highly-linear programmable gain selector, which scales the input range to + 10 volts full-scale.

The scaled 10 volt output is directed to the summing junction of the A/D converter input through the sample-and-hold and sign-bit options, if installed. In 10 μsec, the A/D converter digitizes the analog voltage at its input into a 10-bit binary code, using the successive-approximation technique. The sign-bit option permits conversion of bipolar inputs (0 to ± 1.25, ± 2.5, ± 5.0, or ± 10.0 volts) to an 11-bit 2's complement code with an extended sign format.

Data Buffer Register (ADDB) 776 772
The A/D converter Data Register transfers data to the PDP-11 in the following format. To the processor, the data is read only.



OUTPUT WORD FORMAT-UNIPOLAR OPERATION



OUTPUT WORD FORMAT-BIPOLAR OPERATION

Bits 15 to 10 are tied together, and are "0" in the standard unipolar configuration. With the sign bit option, bits 15 to 10 indicate the sign of the input voltage.

OUTPUT NOTATION TABLE *

Analog Input Voltage	Unipolar	Bipolar
−10.0		176 000
− 5.0		177 000
0.0	000 000	000 000
+ 5.0	001 000	001 000
+ 9.9902	001 777	001 777

* For 10 volt full scale input range. Divide by appropriate gain factor for other input ranges.

Each multiplexer channel switch consists of an enhancement mode MOSFET, which is normally open when unselected or when system power is removed. These switches provide overload protection up to ± 20 volts, and signal protection against electrical short-circuit.

SPECIFICATIONS

Main Specifications

Resolution:	Unipolar 10 bits, or 1 part in 1024 Bipolar (option) sign + 10 bits.
System Accuracy:	0.1% of full scale (FS) input
Quantizing Error:	± ½ least significant bit
System Conversion Time: (includes Channel and gain)	Unipolar: 22 μsec Bipolar: 29 μsec
Sample and Hold:	Acquisition: 5 μsec to ± 0.01% of FS step Aperture: 100 nanoseconds
Analog Input Channels:	4 minimum, expandable to 32 in groups of 4
Input voltage range: (program selectable)	Unipolar: 0 to + 1.25, + 2.5, + 5.0, + 10.0v FS Bipolar (option): 0 to ± 1.25, ± 2.5v, ± 5.0, ± 10.0v FS
Input Impedance:	1000 megohms in parallel with 20 pf
Input Isolation:	Enhancement mode MOSFET switches, "off" when unselected or power off.
Analog Input Connectors:	Plug-in cable-module
Channel Selection: (program selectable)	6 bit address
Cross channel attenuation:	78 db, DC-80Hz for 20 volts p-p signals, 100 ohm source impedance
Input Gain:	Program selectable
Modes of Operation:	Interrupting/non-interrupting (program selectable) Synchronous (Program control) Asynchronous (external clock enable + 2.0v minimum into Schmidt trigger, repetition rate, 60k Hz maximum.)

Expansion/Installation

Multiplexer expansion or option inclusion in the basic AD01-D is by module insertion into prewired slots.

Register Addresses

Control and Status (ADCS)	776 770
Data Buffer (ADDB)	776 772

UNIBUS Interface

Interrupt vector address:	130
Priority level:	BR4 to 7
Bus loading:	1 bus load

Mechanical

Mounting:	1 panel mounted unit
Size:	5¼" front panel height
Weight:	15 lbs.

Power

Input current:	0.5 A at 115 VAC
Heat dissipation:	60 W

Environment

Operating temperature:	0°C to 55°C
Relative humidity:	10% to 95%

Models

AD01-DA: A/D converter subsystem, 115 VAC, 60 Hz
AD01-DB: " , 230 VAC, 50 Hz

LOW LEVEL ANALOG INPUT SUBSYSTEM, AFC11

DESCRIPTION

The AFC11 is a flexible, high performance, differential analog input subsystem for IDACS-11 industrial data acquisition control systems.

The AFC11 system multiplexes up to 1024 differential input analog signals, selects gain, and performs a 13-bit analog-to-digital conversion at a 200 channel per second rate under program control. Three signal conditioning modules and eight program-selectable gains allow the system to intermix and accept a wide range of signals: low level (10 mv full scale), high level (100.0v FS), and current inputs (1 to 50 ma FS).

Designed for accurate and reliable operation in demanding industrial environments, the AFC11 achieves high isolation and common mode noise rejection through relay switched capacitor multiplexing. The subsystem also simplifies input wiring, requiring only simple twisted pairs which connect to screw terminals.

Modularly constructed in eight-channel standard hardware units, the AFC11 is easy to configure to user applications, and simple to expand.

The analog input subsystem is particularly suited for data acquisition in the high noise environments encountered in process monitoring and control, production testing and laboratory applications. In such environments common and normal mode noise, cabling and grounding problems can greatly affect the operation of such transducers as thermocouples, strain gages, analytical bridges, and industrial milliamp current transmitters. These problems can also affect the accuracy and performance of the measuring system.

In typical applications, use of ungrounded sensors could cause common mode voltages of up to 150 volts peak-to-peak (at power line frequency) to appear on the input signal leads to the measuring system. For example, if thermocouples become ungrounded during operation, large common mode voltages can appear in coincidence with the signal. The design features of the AFC11 allow either floating or grounded signal sources thus insuring reliable, trouble-free operation. Due to the flying capacitor design, the system tolerates common mode voltages in excess of 200 volts. FET solid-state multiplexers, in contrast, can be seriously damaged with common mode voltages over 25 volts.

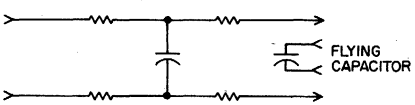
System Organization

The AFC11 system is completely modular for ease of system configuration and expansion. For applications requiring 128 channels or less the system is available in a single cabinet configuration. Systems requiring greater than 128 but less than 512 channels are housed in a dual cabinet configuration—one cabinet to mount the electronics and one for the screw terminal connectors. Two dual cabinet configurations, each containing 512 channels, are required to implement a maximum system of 1024 channels.

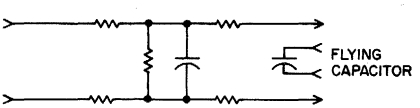
The system's electronic cabinets are organized in files. The first file in the system is a master file which contains the computer interface, system timing and control, an A/D converter, a programmable gain differential amplifier, and address decoding hardware for selection of up to 32 channels. The master file may also contain three additional file units, each providing address decoding and analog bus isolation for up to 32 channels. The hardware for each 32 channel group is implemented by adding up to four eight-channel pairs of multiplexer/signal-conditioning modules and the required screw terminal cable assemblies—one for each module pair. Fully implemented, the master file contains 128 channels.

Expansion beyond 128 channels is by addition of expander files. Each expander file contains a programmable gain amplifier and provision for a total of 192 channels in six file units.

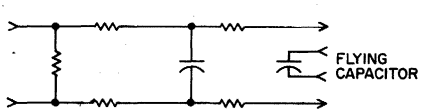
A file unit contains from one to four eight-channel Multiplexer Modules (Model BA150), each of which requires an eight-channel input signal conditioning module. The conditioning modules, which connect to screw terminal blocks via cable assemblies, are available in three types:



Direct Input Module (Model BA903) provides eight channels of normal mode input filtering with a break frequency of 2.5 Hz. Attenuation at 60 Hz is greater than 50 db.



Voltage/Voltage Input Module (Model BA904) provides 8 channels of 10:1 attenuated input with the same normal mode filtering as direct input. Maximum full scale input is + 100 volts.



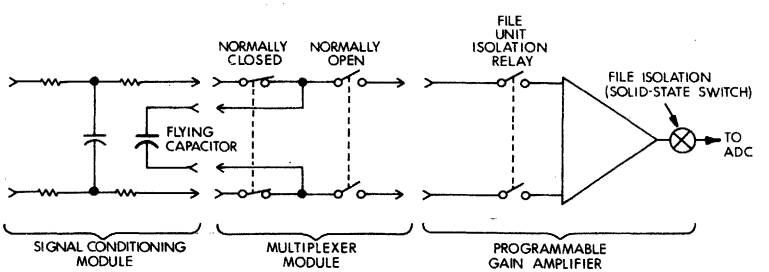
Current/Voltage Input Module (Model BA905) scales eight channels of 50, 20, or 5 ma full scale current inputs to 0.5, 0.2, or 0.05 volts full

scale and provides the same normal mode filtering as the direct input module.

Flying Capacitor Multiplexing
The flying capacitor multiplexing technique permits micro-volt signals to be isolated, switched and digitized by an analog-to-digital converter with a high degree of noise immunity.

The Flying Capacitor is a two pole RC filter network in which a second or "flying" capacitor is charged, then isolated and switched to the measuring circuit. Since the source is never directly connected to the measuring circuit, extremely high isolation is achieved.

Lo-pass filtering per point (2.5 Hz cutoff) plus the high isolation of the flying capacitor technique provide high common mode noise rejection (120 db at 60 Hz) without requiring expensive individually-shielded input wiring.



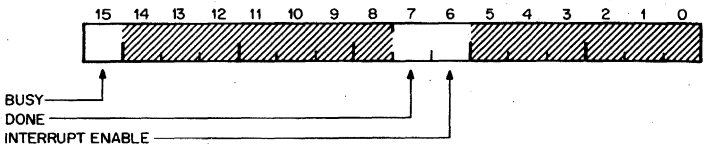
Typical File Unit Channel

Programmable Gain Control Channel Selection
Both gain and channel are under program control. A 16-bit Channel Address Gain/Select Control word is transferred from the IDACS-11 processor to the AFC11 Channel/Gain Register (AFCG). The multiplexer channel address is contained in bits 0-10 and decoded to select 1 out of 64 File Units (6 bits) and 1 out of 32 channels (5 bits) within the File Unit. The programmable gain control on the input amplifier is buffered and FET switched for reliability. Amplifier gain is selected by bits 13-15.

When a channel is selected, the input signal is isolated and the File Unit isolation relay closes to connect the charged capacitor to the Programmable Gain Amplifier. The amplifier is connected to the analog bus and ADC by closing the file isolation switch. Timing is initiated which allows the switches to settle and conversion to begin.

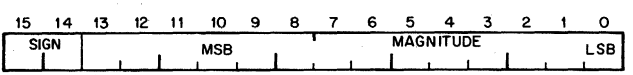
REGISTERS

Control and Status Register (AFCS) 772 570

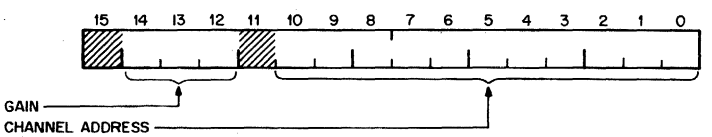


BIT	NAME	FUNCTION
15	Busy	Set by INIT or LOADING MX Channel Gain Register. Reset by A/D DONE.
7	Done	Set by A/D DONE. Reset by reading Data Buffer Register.
6	Interrupt Enable	Set under program control. Reset by INIT or under program control.

Data Buffer Register (AFBR) 772 572



Multiplexer Channel/Gain Register (AFCG) 772 574

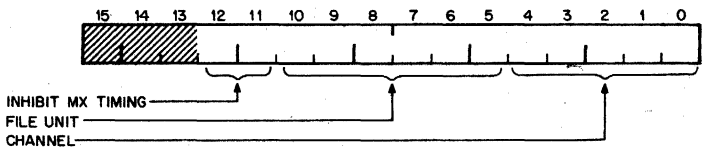


BIT	NAME	FUNCTION
14-12	Gain	Sets amplifier gain according to the following table. Cleared by INIT. (READ/WRITE).

BIT 14	BIT 13	BIT 12	GAIN
0	0	0	1000
0	0	1	200
0	1	0	100
0	1	1	50
1	0	0	20
1	0	1	10
1	1	1	2

10-0	Channel Address	Selects multiplexer channel. Bits 10-05 select 1 or 64 file units. Bits 04-00 select 1 of 32 channels in a file unit. Cleared by INIT. (READ/WRITE).

Maintenance Register (AFMR) 772 576



This Read/Write Register is for diagnostic purposes only. Permits checking of channel address by reading back decoded bits.

SPECIFICATIONS

Analog Input Specifications

Number of Inputs:	8 to 1024, in groups of 8
Type:	differential, 2 wire twisted pair
Connection:	solder lug, or screw terminal

System Performance

Resolution:	Sign + 12 bits (2's complement)
Accuracy: (for direct input)	± 0.025% of full scale or ± 15 μV (whichever is larger) ± ½ least significant bit (LSB)
Scan Rate, Including A/D Conversion:	200 channels/second, maximum (20 samples/second, same channel)
Normal Mode Rejection:	> 50 db for frequencies 60 Hz or above
Common Mode Rejection:	> 120 db DC to 60 Hz
Common Mode Voltage Tolerance:	200 volts
Input Overload:	Amplifier fused against overload
Effects of Overload:	Recovers to within stated accuracy for next channel.
Channel-to-Channel Isolation:	10^{12} ohms at DC, Channel-to-channel. 10^{12} ohms at DC, channels on same multiplexer module.
Gain Accuracy:	± 0.02%
Gain Linearity:	± 0.01%
Temperature Coefficient:	± .005%/ °C or better

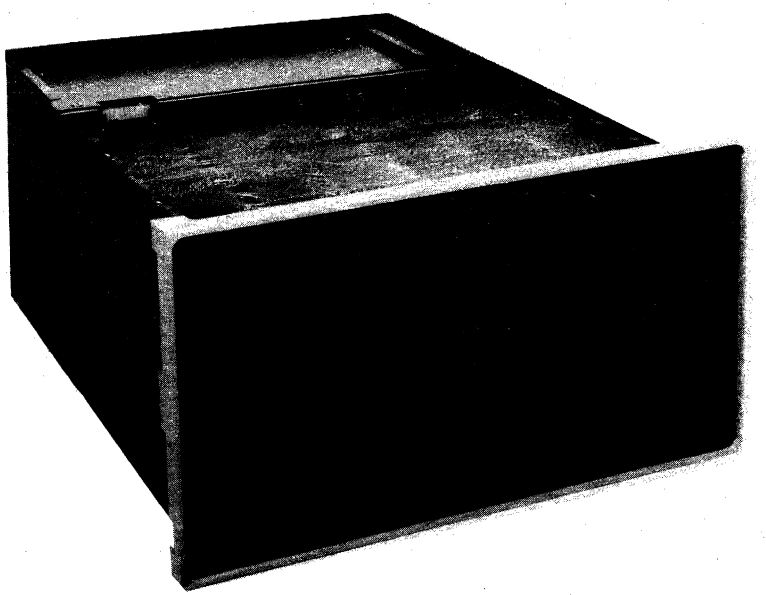
Register Addresses	
Control and Status (AFCS)	772 570
Data Buffer (AFBR)	772 572
MX Channel/Gain (AFCG)	772 574
Maintenance (AFMR)	772 576
UNIBUS Interface	
Interrupt vector address:	134
Priority level:	BR4
Bus loading:	1 bus load
Mechanical	
Size:	each cabinet is 72"H x 21"W x 30"D
Weight:	750 lbs. (dual cabinet, 512 channels)
Power (per cabinet)	
Input current:	15 A at 115 VAC, 40 to 440 Hz, single phase
Heat dissipation:	1700 W
Environment	
Operating temperature:	10°C to 55°C
Relative humidity:	10% to 95%

EXTENSION MOUNTING BOX, BA11-ES

DESCRIPTION

The BA11-ES Extension Mounting Box can hold up to 6 System Units plus an H720 power supply. The box uses 10½" of front panel space, and is supplied with tilt and lock chassis slides.

The mounting box contains fans for forced air cooling, an insulated top cover (not shown) to prevent debris from falling into the wire-wrap pins (this is necessary because the system units are mounted with the pins up and the modules down), and a foam-lined bottom cover, which serves as a module retainer and minimizes module vibration. The bottom cover serves as part of the air plenum to ensure adequate cooling.



BA11 Mounting Box (with wired System Units and H720 Power Supply installed)

The mounting box is fabricated from zinc-plated steel to resist corrosion.

H720 Power Supply

The H720 Power Supply provides power for the BA11-ES Extension Mounting Box. It provides + 5V and — 15V regulated power. The + 5V portion is protected by overvoltage circuits and both portions of the sup-

ply feature dynamic current limiting. The basic regulating element is a high efficiency switching regulator that keeps voltages within a ± 3 percent tolerance. In addition to providing power, the H720 Supply generates three other signals: a line frequency signal that approximates a squarewave referred to as LTC (line time clock), and the AC LO and DC LO UNIBUS signals. The low voltage detection circuits are interlocked so that — 15V is not established until + 5V is established. If the + 5V fails, the — 15V section is shorted to ground to prevent damage to system logic circuits.

There are two H720 Power Supply Models. The H720-E is designed for use with an input of 115V, ± 10 percent. The H720F is designed for an input of 230V, ± 10 percent. In addition, the H720-F has taps for lower voltages of 215 and 200, ± 10 percent. Both models are designed to operate within a 47- to 63-Hz frequency range.

H720 Power Supply Outputs

Output	Regulation	Capacity	Remarks
+ 5V	± 5%	22A	
— 15V	± 3%	10A	
+ 8V, rms	± 15%	1.5A	Full-wave, unfiltered
— 24V	± 20%	1.0A	Unregulated, filtered
LTC L	0 to 5V		Line time clock
AC LO L	Logic level		ac line low
DC LO L	Logic level		dc line low

SPECIFICATIONS (BA11-ES plus H720)

Mechanical

Equipment capacity:	6 System Units
Mounting:	1 panel mounted unit
Size:	10½" front panel space
Weight:	130 lbs.

Power

Output current:	22 A at + 5V 10 A at — 15V
Input current:	6 A at 115 VAC
Heat dissipation:	700 W

Environment

Operating temperature:	0°C to 50°C
Relative humidity:	20% to 95%

Models

BA11-ES:	Extension mounting box (needs a power supply)
H720-E:	Power supply, 115 VAC, 60 Hz
H720-F:	" , 230 VAC, 50 Hz

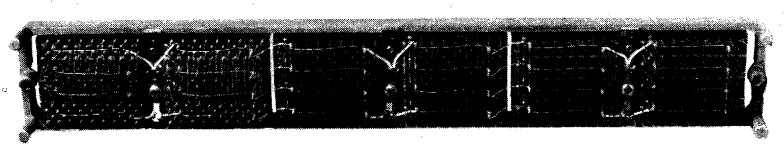
BLANK MOUNTING PANEL, BB11

The BB11 Blank Mounting Panel is a prewired System Unit (SU) designed for general interfacing. It is prewired only for the UNIBUS and power. The unit contains three 288-pin blocks assembled end-to-end in a casting which can be mounted in the various PDP-11 assembly units. Bus and power connectors, described below, use only 6 of the module slots, thereby leaving 18 slots available for customer use.

The BB11 is wired to accept the UNIBUS in slots A1 and B1. This connection can be made with an M920 UNIBUS Connector or a BC11A UNIBUS Cable Assembly. All bus signals, including grant signals, are wired directly to corresponding pins in slots A4 and B4. From this point, the UNIBUS can be continued to the next unit by using an M920 or BC11A. If the BB11 is the last unit on the bus, slot A4-B4 accepts the M930 Bus Terminator Module. Standard bus pin names are listed in Appendix B.

The bus grant signals are wired through the BB11. These grant signal wires must be removed and replaced with wires to and from the user's control circuits for the grant levels used by the customer-supplied device.

Slot A3 accepts the G772 Power Connector (furnished as part of the BA11 Mounting Box). Power for + 5V is distributed to all A2 pins; — 15V is distributed to all B2 pins except in slots A1, B1, A4, and B4; and ground is maintained through the frame and power connector on pins C2 and T1 of all slots.



BB11 System Unit

	A	B	C	D	E	F
4	UNIBUS CONN					
3	POWER					
2	RESERVED					
1	UNIBUS CONN					

BB11 Module Layout

READ ONLY MEMORY (ROM)

Read only memory is available in 32 word increments, and a total of 256 words of ROM can be included in a PDP-11 system. ROM's can be programmed by the user; standard preprogrammed ROM's are offered as bootstrap loaders for various peripheral devices. Access time is 100 nsec per word.

Programmable ROM (M792)
The basic ROM module contains 32 16-bit words of diode read-only memory. The ROM is supplied with a 32 by 16 diode matrix. Diodes can be selectively cut out to yield the desired data pattern; diode in = 1, no diode = 0. The unprogrammed ROM contains all 1's; programming of the memory is accomplished by eliminating diodes for the bits that should be read as 0's. The location of the diodes with respect to word and bit number are indicated on the module.

Addresses
The 32 words are in consecutive memory addresses. The address range of the lowest address is jumper selectable betwen 773 000 and 773 700. The jumper wires affect bits 6 to 8 of the address, and are indicated on the module by the designations W1, W2, and W3.

Bit 8 (W3)	Bit 7 (W2)	Bit 6 (W1)	Address Range
0	0	0	773 000 to 773 076
0	0	1	773 100 to 773 176
0	1	0	773 200 to 773 276
0	1	1	773 300 to 773 376
1	0	0	773 400 to 773 476
1	0	1	773 500 to 773 576
1	1	0	773 600 to 773 676
1	1	1	773 700 to 773 776

To make the jumpers correspond to the desired bit addresses, jumper in = 0, no jumper = 1.

A maximum of 8 ROM modules can fit into the address space allotted, so that a small read-only memory of 256 words can be used. Such a memory could provide non-erasable recovery routines, or lowered program execution times for often-used loops or subroutines.

Bootstrap loaders (BM792-Y)
Several basic M792 modules are preprogrammed (diodes selectively eliminated) as bootstrap loaders for convenient loading of initial programs to handle various I/O and peripheral devices.

An M792 ROM module mounts in one Small Peripheral Controller (SPC) slot. The module is quad height.

READ ONLY MEMORY (M792) SPECIFICATIONS

Access time:	100 nsec
Memory size:	32 words, 16 bits each
UNIBUS loading:	1 bus load
Mounting space:	1 SPC slot (quad module)
Current requirements:	0.3 A at + 5V

Model No.	Address Range	Description
M792	773 000 to 773 776	Basic unit with all diodes included (contents are all 1's). Diodes are selectively removed to make 0's.
BM792-YA	773 000 to 773 076	Papertape bootstrap loader for Teletype or high-speed paper tape reader (PC11).
BM792-YB	773 100 to 773 176	Disk/DECtape bootstrap loader.
BM792-YC	773 200 to 773 276	Card Reader bootstrap loader (CR11)
BM792-YH	773 300 to 773 376	Cassette bootstrap loader (TA11)
MR11-DB	773 100 to 773 276	Bootstrap loader for mass storage devices.

Device	Starting Address
RF11	773 100
RK11	773 110
TC11	773 120
TM11	773 136
RP11	773 154
RC11	773 220

The MR11-DB consists of 2 preprogrammed M792 modules.

HIGH-SPEED PUNCHED CARD READER, CD11

DESCRIPTION

The CD11 High-Speed Card Reader reads EIA standard 80-column punched data cards at up to 1200 cards per minute.

The punched-card reader uses a vacuum picker which works in conjunction with riffle air to make card wear insignificant and card jam virtually impossible, while providing extreme tolerance to damaged cards. The riffling action separates the cards in the input hopper to prevent sticking. The picker uses a strong vacuum to grasp the bottom card and deliver it to the read station on demand. The picker and associated throat-block prevent the unit from multiple picking to the extent that taped or stapled cards are not allowed to enter the card track. In such cases, the reader stops, with pick check alarm on. The operator can then separate the cards and enter them into the input hopper for normal reading. The card track is very short, so that only one card is in motion at any time. The combination of tolerance to damaged cards, gentle card handling and short card track provide virtually jam-proof operation for the CD11.

The CD11 accesses the UNIBUS from both the interrupt and the non-processor request (Direct Memory Access) modes of operation. Control and status information is relayed in the interrupt mode. Data is transferred through Direct Memory Access.

The CD11 reads a series of cards by using the Interrupt and NPR Control. Setting the Read Bit in the Status and Control Register begins the read operation.

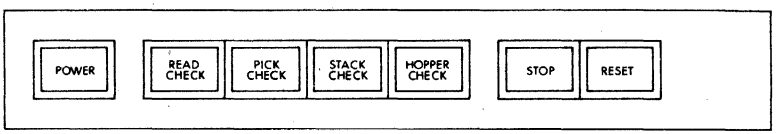
A card is composed of 80 columns, each of which contains 12 zones. When a column is read, an NPR request is generated. Each column is loaded into memory as either a word or a byte. On a word transfer, or non-packing mode, each bit is loaded directly into memory as card image. On a byte transfer, or packing mode, the 12 bits on a column are packed into 8 bits in memory, as described in the Register section.

The Bus Address Register is initially set to the memory location into which the first column is to be read. It then increments by 1 for transfers in the packing mode, or by 2 for transfers in the non-packing mode. The column count register is initially set to the two's complement of the number of columns to be read. When it becomes 0, further transfers into memory are inhibited. If, while reading a card, the column count register becomes 0, further transfers stop and after the card has been read, an interrupt occurs, provided the interrupt enable bit is set. If, after reading a card, the column count register has not become 0, the next card is automatically picked for reading.

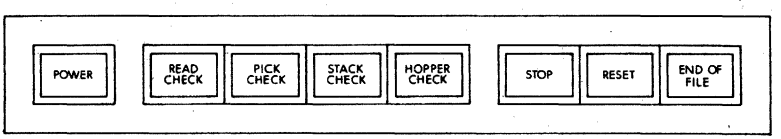
When a READ command is sent from the control to the card reader, the ready line from the card reader becomes 0. The busy line from the card reader then becomes 1, immediately before the card is read. After the last

column has been read, the busy line becomes 0. The ready line from the card reader is set to 1 if an overflow condition occurred in the column count register, otherwise the ready line remains 0 and the next card is picked.

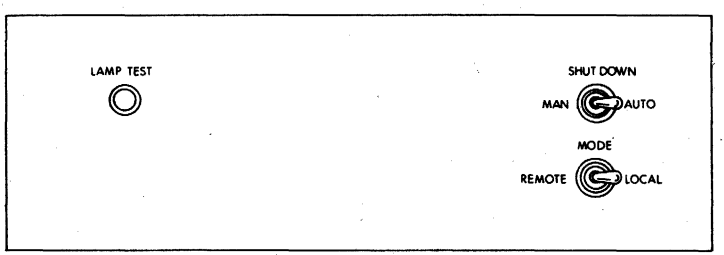
CONTROLS & INDICATORS



a. Front Control Panel—(CD11-A)



b. Front Control Panel—(CD11-E)



c. Rear Control Panel—Both Models

Front Panel Controls and Indicators

Control or Indicator	Type	Function
POWER switch	alternate-action pushbutton/ indicator switch	Controls application of all power to the card reader. When indicator is off, depressing switch applies power to reader and causes associated indicator to light. When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.
READ CHECK indicator	white light	When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in 0 or 81st column positions. Because READ CHECK indicates an error condition, whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.
PICK CHECK indicator	white light	When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ command from the controller. Stops card reader operation and extinguishes RESET indicator.
STACK CHECK indicator	white light	When lit, this light indicates that the previous card was not properly seated in the output stacker and, therefore, may be badly mutilated. Stops card reader operation and extinguishes RESET indicator.
HOPPER CHECK indicator	white light	When lit, this light indicates that either the input hopper is empty or the output stacker is full. In either case, the operator must manually correct the condition before card reader operation can continue.

Front Panel Controls and Indicators (cont.)

Control or Indicator	Type	Function
STOP switch	momentary pushbutton/ indicator switch (red light)	When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read. This switch has no effect on system power; it only stops the current operation.
RESET switch	momentary pushbutton/ indicator switch (green light)	When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller. The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).
END OF FILE switch	momentary pushbutton/indicator switch	This switch is used as a programming aid to inform the user when an end-of-file has been reached. As an example, assume that a particular file greatly exceeds the input hopper capacity. The hopper is loaded to capacity, the card reader operated until a HOPPER CHECK indication occurs, and the hopper is loaded with more cards. When the last group of cards is loaded, the user can then depress END OF FILE. As soon as the last card in this group is read, an END OF FILE bit in the controller is set. This END OF FILE bit can then be read by the program at any time. Whenever the END OF FILE pushbutton is depressed, the card reader functions in a normal manner until

Front Panel Controls and Indicators (cont.)

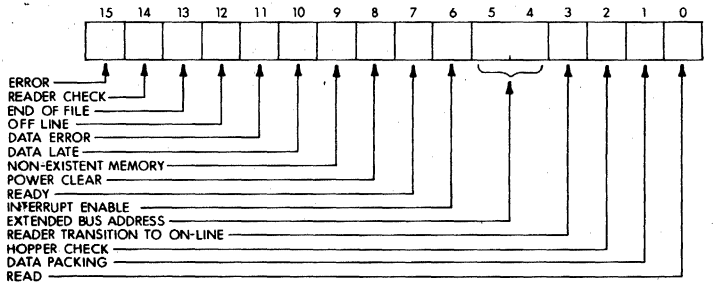
Control or Indicator	Type	Function
		the input hopper is empty (the last card has been read). As soon as this occurs, the card reader HOPPER CHECK indicator comes on and the controller END OF FILE bit is set. Note that the END OF FILE can be depressed at any time but the END OF FILE signal is not sent to the controller until the last card has been completely read.

Rear Panel Controls

Control	Type	Function
LAMP TEST switch	pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	Controls automatic operation of the input hopper blower. MAN position—blower operates continuously whether or not cards are in the input hopper. AUTO position—causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when cards are loaded into the hopper and the RESET switch is depressed. Blower activates approximately 3 sec after RESET is depressed.
MODE switch	2-position toggle	Permits selection of either on-line or off-line operation. LOCAL position—removes the READ command input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel. REMOTE position—enables the READ command input from the controller to allow normal on-line operation under program control once RESET is depressed.

REGISTERS

Status and Control Register (CDST) 772 460



Effect of the Initialize (INIT) signal: clear bits 15 to 13, 11 to 9, 6 to 3, 1, and 0.

Read only: bits 15 through 9, 7, 3, and 2
Write only: bits 8 and 0

BIT	NAME	FUNCTION
15	Error (ERR)	Set to indicate an error condition that is the inclusive OR of all error conditions (bits 14-09 in this register). If the error condition is due to bit 11, 10, or 9, the Error bit does not set until the Busy signal from the Card Reader is cleared. This permits the entire card to pass through the read station before an interrupt occurs.
14	Reader Check	Set when an abnormal condition exists in the card reader. Any one of the following four conditions sets this bit: a. **Hopper Check**—input hopper is empty or the output stacker is full. This error indication occurs after column 80 of the last card has been read. b. **Pick Check**—feed mechanism failed to deliver a card to the read station when demanded. This error condition occurs if a card is not delivered within 400 ms after a Read command is initiated. c. **Stack Check**—previous card was not properly seated in the output stacker and, therefore, may be badly damaged.

BIT	NAME	FUNCTION
		d. **Read Check**—read station electronics do not agree with the usual light and dark areas of the card. This could be caused by torn cards or cards with illegal punches (holes in 0 or 81st column positions).
		Error-causing condition should be corrected before clearing this bit.
13	End of File (EOF)	Used with CD11-E only. Associated with the END OF FILE pushbutton on that reader.
		The END OF FILE pushbutton is used as a programming aid to allow the user to insert an END OF FILE flag at the appropriate place in the program.
		When the last group of cards in a specific file has been loaded into the hopper, the user can then depress the END OF FILE switch. When the switch is depressed, the card reader functions in a normal manner until the input hopper is empty and the last card is read. At this time, the card reader HOPPER CHECK indicator light comes on and the controller END OF FILE bit (bit 13) is set. Because a hopper-empty condition is considered an error, the status register Reader Check, Hopper Check, and Error bits are also set.
		When a CD11-A is used, bit 13 is always clear.
12	Off Line	Set when the reader is off-line. When clear, the reader is on-line, under program control, and ready to accept a Read command.
		Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in the REMOTE position.
		The card reader goes off-line (setting bit 12) whenever an error condition is sensed (STOP light on reader is lit), whenever the reader STOP pushbutton is depressed, or whenever the MODE switch is set to the LOCAL position.
11	Data Error	When the controller is in the packing mode of operation (bit 1 set), the normal 12-bit code is compressed into an 8-bit code that allows a column to be transferred as a single byte. When this compressed code is used, card zones 1-7

BIT	NAME	FUNCTION
		are represented by an octal code; therefore, no more than one zone should be at 1 at any given time. Set in the packing mode whenever more than one of zones 1-7 are a 1. When bit 11 sets, it does not inhibit further transfer of data into memory.
10	Data Late	Set when NPR request is not granted during the time that data is guaranteed valid from the Card Reader. This bit prevents further NPR requests from occurring, thereby preventing clocking of the column-count register (CDCC) and current address register (CDBA).
9	Non-Existent Memory	If the controller is engaged in an NPR data transfer and attempts to access a memory address that does not exist, bit 9 sets to provide an NXM error indication. This NXM error occurs if the controller does not receive SSYN within a specified time after it has issued MSYN. When set, this bit inhibits further NPR requests.
8	Power Clear (PWR CLR)	Set to clear the column-count register (CDCC), the current address register (CDBA), and all bits in the status register (CDST) with the exception of bits 12, 7, and 2.
7	Ready (RDY)	Set when the CD11 is ready to receive a new command. This bit is set by one of the following conditions: a. **Error bit set**—an error condition exists and the program should branch to an error-handling routine. b. **Power Clear bit set**—all controller logic has been cleared and the controller can engage in a data transfer. c. **INIT signal occurs**—same as POWER CLEAR. d. **Busy clear and CDCC overflow**—the preset number of data transfers has been performed and the controller is now ready for a new Read command.

BIT	NAME	FUNCTION
6	Interrupt Enable (INT ENB)	Set to allow either Ready or Reader Transition to On Line = 1 to cause an interrupt.
5-4	Extended Bus Address (XBA17, XBA16)	Used to specify bus address lines 17 and 16 in direct memory transfers. Increment with the current address register (CDBA). Bit 5 corresponds to XBA17, bit 4 to XBA16.
3	Reader Transition to On Line (ON LINE TRANS)	Set when the card reader has gone on-line and is under program control. Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in REMOTE. The card reader goes off-line whenever an error condition is sensed or when the STOP switch is depressed. **NOTE** The READER TRANSITION TO ON-LINE bit does not clear when the reader goes off-line.
2	Hopper Check	Set to indicate that either the input hopper is empty or the output stacker is full. The bit will set Reader Check (bit 14). The bit is cleared by correcting the condition that caused the error. Because the bit is controlled by the HOPPER CHECK signal from the card reader, it will not be cleared by Power Clear.
1	Data Packing	Determines whether the data is to be loaded as a 12-bit word or as a 8-bit byte; 0 = 12-bit word, 1 = 8-bit byte. **NOTE** This bit has no effect on data read from the processor.
0	Read	Set to cause the card reader feed mechanism to deliver one card to the read station for reading. When set, the bit clears the following bits in the status register: 15, 14, 11, 10, 9, 7, and 3. The bit also clears Error (bit 15), provided Hopper Check (bit 2) is clear. If the Read bit is set when the Card Reader is busy, it will reset bits 15 and 2. Error is set to indicate that a Read command was issued when the card reader was not available for use.

Column Count Register (CDCC) 772 462

BIT	NAME	FUNCTION
15-0	Column Count	Contains the 2's complement of the number of columns to be transferred to memory when cards are being read.

The column-count register is loaded prior to initiation of the read function. The register is incremented by 1 after each transfer. When the contents of the register equal all 0s, further transfers are inhibited until another READ command occurs.

If an entire 80-column card is read and the column-count register has still not advanced to 0, then the next card is automatically fed to the read station.

All bits may be loaded or read by the program. Cleared by POWER CLEAR (bit 8 in the status register set) or by INIT.

NOTE

The column-count register should not be modified by using byte instructions. Use only word instructions when loading this register. The register is wired in such a manner that the entire word is loaded even if a byte instruction is used. Therefore, if the programmer attempts to load only the low-order byte, for example, the data on the high-order data lines is also loaded. This latter data may be useless and/or unknown to the programmer.

Whenever the column-count register reaches 0, an interrupt is initiated if INT ENB is set to inform the processor that the desired number of columns has been transferred.

Current Address Register (CDBA) 772 464

BIT	NAME	FUNCTION
15-0	Address	These bits specify the bus or memory address into which the next column of data is to be stored.

The current address register is initially set to the memory location of the first column to be read. It then increments by 1 for transfers in the packing mode (byte transfers) and increments by 2 for transfers in the non-packing mode

BIT	NAME	FUNCTION

(word transfers). Incrementation occurs immediately after each data transfer.

The bits in this register are used in conjunction with extended address bits A17 and A16 (bits 5 and 4, respectively, in the status register) so that 18-bit memory addresses may be used.

Note that the extended address bits participate in the incrementation; they are a logical extension to this register.

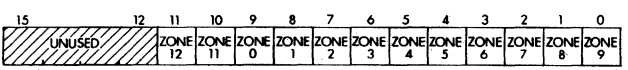
The current address register is loaded prior to issuing a READ command. The register may be loaded or read by the program.

Cleared by POWER CLEAR (bit 08 in the status register set) or by INIT.

NOTE

The current address register should not be modified by using byte instructions. Use only word instructions when loading this register.

Data Buffer Register—Non-Packing Mode (CDDB) 772 466



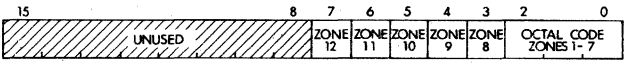
BIT	NAME	FUNCTION
11-0	Zone	These bits represent the output of a 12-bit data buffer register. When the register is in a non-packing mode (bit 01 in the status register is clear), data from a card is loaded into this buffer one column at a time on a word basis. After each column is loaded, the contents of the buffer is placed on the Unibus for transfer to the processor, memory, or other bus device.

The contents of the buffer is coupled to the 12 least-significant bus data lines as shown below:

Bit	Corresponding Card Image
11	ZONE 12
10	ZONE 11
9-0	ZONES 0-9, respectively

Bits 11-0 are read as 1s whenever a card is not being read; bits 15-12 are always read as 0s.

Data Buffer Register—Packing Mode (CDDB) 772 466



BIT	NAME	FUNCTION
7-0	Zone	These bits also represent the output of the data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the UNIBUS as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.

Bits 7 through 3 are encoded as follows:

Bit	Corresponding Card Image
7	ZONE 12
6	ZONE 11
5	ZONE 10
4	ZONE 9
3	ZONE 8

Bits 2 through 0 represent an octal code that defines the card zone as shown below. In the case of multiple zones, these bits are the inclusive OR of the octal codes of the zones.

Bit 02	Bit 01	Bit 00	Card Zone
0	0	0	zero, ZONES 1-7
0	0	1	ZONE 1
0	1	0	ZONE 2
0	1	1	ZONE 3
1	0	0	ZONE 4
1	0	1	ZONE 5
1	1	0	ZONE 6
1	1	1	ZONE 7

All bits are read-only bits with the same conditions as described previously.

SPECIFICATIONS	CD11-A	CD11-E (when different)
Main Specifications		
Input medium:	80-column punched cards, 12 zones (or rows)	
Speed:	1000 cards/minute	1200 cards/min
Hopper capacity:	1000 cards	2300 cards

Register Addresses

Status and Control	(CDST)	772 460
Column Count	(CDCC)	772 462
Current Address	(CDBA)	772 464
Data	(CDDB)	772 466

UNIBUS Interface

Interrupt vector address:	230
Priority level:	BR4
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical		
Mounting:	1 table top unit + 1 system unit (SU)	
Size:	14"H x 24"W x 18"D	38" x 24" x 38"
Weight:	85 lbs.	200 lbs.
Power		
Running current:	4A at 115 VAC	6A
Starting current:	9A at 115 VAC	16A
Current for control:	2.5A at + 5V	
Heat dissipation:	450 W	700 W
Environment		
Operating temperature:	10°C to 50°C	
Relative humidity:	10% to 90%	

Models

CD11-A: Card reader and control, 1000 cards/min, 115 VAC, 60 Hz
CD11-B: " 1000 cards/min, 230 VAC, 50 Hz

CD11-EA: Card reader and control, 1200 cards/min, 115 VAC, 60 Hz
CD11-EB: " 1200 cards/min, 230 VAC, 50 Hz

PUNCHED CARD READER, CR11 AND MARK SENSE CARD READER, CM11-F

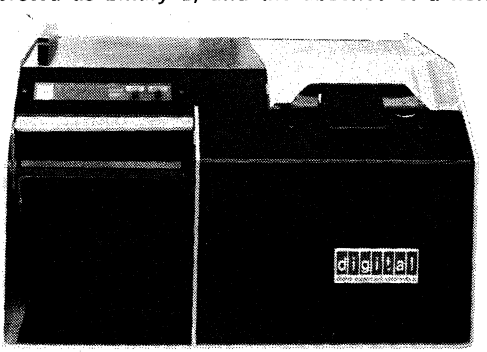
DESCRIPTION

The CR11 Card Reader reads EIA standard 80-column punched data cards at 300 cards per minute; the CM11-F reads 80-column mark-sense cards, which can have punched holes, at 285 cards per minute.

The punched-card reader uses a vacuum picker which works in conjunction with riffle air to make card wear insignificant, card jam virtually impossible, and provide extreme tolerance to damaged cards. The riffling action separates the cards in the input hopper to prevent sticking. The picker uses a strong vacuum to grasp the bottom card and deliver it to the read station on demand. The picker and associated throat block prevent the unit from multiple picking to the extent that taped or stapled cards are not allowed to enter the card track. In such cases the reader stops with pick check alarm. The operator can then separate the cards and enter them into the input hopper for normal reading. The card track is very short, so that only one card is in motion at a time. The combination of tolerance to damaged cards, gentle card handling and short card track provide virtually jam-proof operation.

Operation

Cards are read by column, beginning with Column 1. A read command starts the card moving past the read station. Once a card is in motion, all 80 columns are read. Column information is read in one of two program-selected modes: compressed or image. In the compressed mode, the 12 information bits in one column are automatically decoded and transferred into the least significant half of the Card Reader Data Buffer (CRB2) as 8-bit compressed code. In the image mode, the 12 bits of a column are transferred directly into CRB1 so that Zone 9 is transferred into the CRB bit 0 and Zone 12 is transferred into CRB bit 11. A punched hole is interpreted as binary 1, and the absence of a hole as binary 0.



CARD READER

CONTROLS & INDICATORS

Front Panel

Control or Indicator	Type	Function
POWER switch	alternate-action pushbutton/ indicator switch	Controls application of all power to the card reader. When indicator is off, depressing switch applies power to reader and causes associated indicator to light. When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.
READ CHECK indicator	white light	When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in the 0 or 81st column positions. Because READ CHECK indicates an error condition, whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.
PICK CHECK indicator	white light	When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ COMMAND from the controller. Stops card reader operation and extinguishes RESET indicator.
STACK CHECK indicator	white light	When lit, this light indicates that the previous card was not properly seated in the output stacker and therefore may be badly mutilated. Stops card reader operation and extinguishes RESET indicator.
HOPPER CHECK indicator	white light	When lit, this light indicates that either the input hopper is empty or that the output stacker is full.

		In either case, the operator must manually correct the condition before card reader operation can continue.
STOP switch	momentary pushbutton/ indicator switch (red light)	When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read. This switch has no effect on the system power; it only stops the current operation.
RESET switch	momentary pushbutton/ indicator switch (green light)	When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller. The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).

Rear Panel

Control	Type	Function
LAMP TEST switch	pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	Controls automatic operation of the input hopper blower. MAN position—blower operates continuously whether or not cards are in the input hopper. AUTO position—causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when

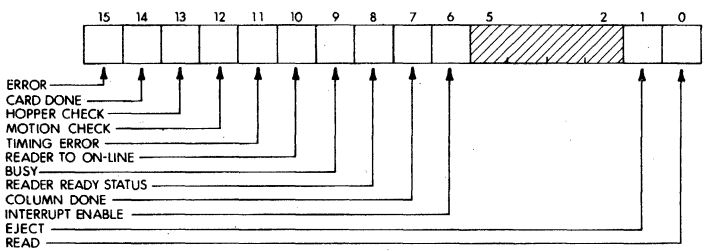
cards are loaded into the hopper and the RESET switch is depressed.

Blower activates approximately three seconds after RESET is depressed.

MODE switch	2-position toggle	Permits selection of either on-line or off-line operation.
		LOCAL position—removes the READ COMMAND input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel.
		REMOTE position—enables the READ COMMAND input from the controller to allow normal on-line operation under program control once RESET is depressed.

REGISTERS

Card Reader Status Register (CRS) 777 160



Effect of the Initialize (INIT) signal: clear bits 15, 14, 11, 10, 7, 6, 1, and 0.

Read only: bits 15 through 7
Write only: bit 0

BIT	NAME	FUNCTION
15	Error	Set when an error occurs.
14	Card Done	Set when one card has passed through the read station and another one may be demanded from the input hopper.

13	Hopper Check	Set when the input hopper is empty or output stack is full. This signal is provided by mark sense card readers and later models of the punched card units.
12	Motion Check	Set to indicate abnormal condition in the card reader. Three conditions can cause this bit to be set: a) Feed error b) Motion error c) Stack Fail These signals are available from the mark sense readers and later models of the punched card units.
11	Timing Error	Set when a new column of data arrived into the CRB before the previously loaded column was attended to by a program.
10	Reader To on Line	Set when the reader is on-line. Sensing an error or operating the stop switch on the card reader panel causes the reader to go off-line. Operating the start switch brings the reader on-line providing no error causing condition exists.
9	Busy	Set when a card is being read.
8	Reader Ready Status	Set when the reader is off line; O indicates on-line and hence ready to accept read commands.
7	Column Done	Set when a column of data is ready in CRB.
6	Interrupt Enable	Set to allow Card Done, Column Done, or Error = 1 to cause an interrupt.
1	Eject	When set, column ready flag is inhibited from setting. However, data transfers between card reader and data buffer do take place.
0	Read	Set to allow the feed mechanism to deliver a card to the read station.

A program can load and read information from the Card Reader Status (CRS) register using appropriate instructions and considering the following limitations:

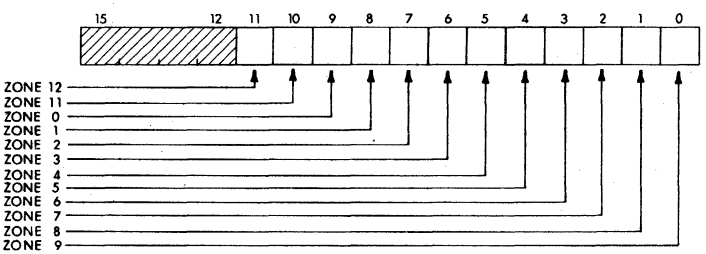
a. Bits 15-7 can only be read on the bus.

b. COLUMN DONE bit is automatically cleared by reading the Data Buffer.

c. Bits 15-8 are automatically cleared when an attempt to load the status register is made. However, if this loading is to read a card, and an error condition requiring manual intervention has not been attended by the operator, appropriate error bit will be set again to cause an interrupt. Commands to READ CARD under these circumstances is not honored.

d. BIT 0 is always read as zero on the bus.

Card Reader Data Buffer Register (CRB1, CRB2) 777 162, 777 164



Read only: all bits

Data from one column at a time of the card is loaded into this register.

BIT	FUNCTION
11	ZONE 12
10	ZONE 11
9	ZONE 0
8	ZONE 1
7	ZONE 2
6	ZONE 3
5	ZONE 4
4	ZONE 5
3	ZONE 6
2	ZONE 7
1	ZONE 8
0	ZONE 9

If the data buffer is addressed at CRB2, the 12-bit content is compressed into an 8-bit character by an encoding network before getting on to the bus as low order byte. The 8-bit code is:

BIT	FUNCTION
7	ZONE 12
6	ZONE 11
5	ZONE 10
4	ZONE 9
3	ZONE 8
2-0	DATA encoded as follows:
	000 = no punches, ZONE 1-7
	001 = ZONE 1 010 = ZONE 2 011 = ZONE 3 100 = ZONE 4 101 = ZONE 5 110 = ZONE 6 111 = ZONE 7

In case of multiple zones twice, bits will be the inclusive OR of the octal codes of the zones.

PROGRAMMING EXAMPLE

The following example shows a typical method of programming the CR11 Card Reader System. In this example, the card reader is used to read a bootstrap loader program from punched cards and load the program into core memory.

```
        CRS=777160          ;CARD READER STATUS REGISTER
        CRB1=777162         ;12-BIT DATA BUFFER
        .=1000              ;STARTING ADDRESS FOR MEMORY

        R1=%1
        R2=%2
        R3=%3
        R4=%4

START:  MOV   #CRS, R1      ;SET UP ADDRESS OF CRS IN R1
        MOV   #CRB1, R3     ;ADD DATA BUFFER ADDRESS IN R3

RTST:   BIT   @R1, #1400    ;IS READER ON-LINE?
        BNE   RTST          ;NO, SO MAY AS WELL WAIT.

RDCD:   INC   @R1           ;O.K., READ A CARD

RCHK:   BIT   @R1, #140000  ;SPECIAL CONDITION OR CARD
                            ;DONE SET?

        BGT   RDCD          ;SPECIAL CONDITION OFF BUT CARD
                            ;DONE ON.

        BEQ   GOGO          ;BOTH OFF
```

```
END:    RESET                   ;SPECIAL CONDITION ON, ASSUME
        JMP     @R2             ;HOPPER EMPTY AND BRANCH TO
                                ;PROGRAM

GOGO:   TSTB    @R1             ;COLUMN READY?
        BPL     RCHK            ;NO, KEEP LOOKING.
        BIT     @R3,    #400    ;ROW 1 IN THIS BYTE?
        BEQ     GO2             ;NO, MUST BE DATA
        MOVB    @R3,    R2      ;YES, IS FIRST ADDRESS BYTE
        SWAB    R2              ;MOVE TO HIGH-ORDER BYTE
        MOV     R1,     R4      ;AND SET SECOND-ADD.-BYTE FLAG
        BR      RCHK            ;AND GET NEXT COLUMN

GO2:    MOV     R4,     R4      ;TEST SECOND-ADD.-BYTE FLAGS
        BNE     GO3             ;IF ON, USE THIS FOR ADD. BYTE
        MOVB    @R3,    (R2)+   ;OTHERWISE, STORE IT IN MEMORY
        BR      RCHK            ;AND GET NEXT BYTE.

GO3:    ADD     @R3,    R2      ;COMPLETE ADDRESS MAKEUP
        CLR     R4              ;RESET SECOND-ADD.-BYTE FLAG
        BR      RCHK            ;AND GO AROUND

        .END
```

SPECIFICATIONS

Main Specifications

Input medium:	80-column punched cards
Speed:	300 cards/minute
Hopper capacity:	600 cards

Register Addresses

Card Reader Status (CRS)	777 160	
Card Reader Buffer (CRB1)	777 162	(12-bit characters)
Card Reader Buffer (CRB2)	777 164	(8-bit char, compressed)

UNIBUS Interface

Interrupt vector address:	230
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	1 table-top unit + 1 SPC slot (quad module)
Size:	11"H x 19"W x 14"D
Weight:	60 lbs
Cable:	15 ft, supplied

Power

Starting current:	9 A at 115 VAC
Running current:	4 A at 115 VAC
Current for Control Unit:	1.5 A at +5 V
Heat dissipation:	400 W

Environmental

Operating temperature:	10°C to 50°C
Relative humidity:	10% to 90%

Models

CR11:	Punched card reader and control, 115 VAC, 60 Hz
CR11-A:	" 230 VAC, 50 Hz
CM11-FA:	Mark-sense card reader and control, 115 VAC, 60 Hz
CM11-FB:	" 230 VAC, 50 Hz

UNIBUS LINK, DA11-B

DESCRIPTION

The DA11-B DMA UNIBUS Link is a high-speed, half-duplex data-transfer channel connecting two PDP-11 computer systems over a distance of up to 100 ft. (30 meters). Using the direct-memory-access (DMA) facilities of each computer, the link transfers either single words or blocks of data from the memory of one machine to the memory of the other. Data blocks up to 32K words in length can be transmitted via the Link in a single operation. The transfer rate can be as high as 500,000 words per second.

The Link consists of a general purpose DMA bus interface attached to each computer plus the interconnecting logic and cables that synchronize both interfaces. The bus link operates in two different modes: Word and Block. In Word Mode, information is passed between computers one word at a time by interrupt-driven program commands. In Block Mode, the link transmits blocks of consecutive locations from the memory of one computer to the memory of the other, using the DMA (NPR) facility in each machine. Each computer controls its own interface to the link. Each has its own Word Count and Bus Address registers that control the number of words in a block transfer and the memory addresses involved. The Link's Word Mode can be used to pass this control information prior to a block transfer.

After the interface registers have been initialized, a command is given to initiate the block transfer. The transmitting interface reads a word from its memory, using the NPR facility of the UNIBUS, and sends that word to the interface on the adjacent computer. The receiving interface gains control of its bus via an NPR request, and then transfers the word from the interface to memory. As each word is transferred, both interfaces automatically increment their Word Count and Bus Address registers. The alternating sequence of cycles continues until the block transfer is complete, whereupon both interfaces generate "transfer-done" interrupts. Each bus interface is constructed as a single system unit that can be installed in any PDP-11 mounting box. The interconnecting cables are shielded and terminated so that the two computers can communicate over distances up to 100 feet (30 meters).

PROGRAMMING

In order to coordinate the channel set-up procedures, the programmable control units in each interface are interconnected to pass interrupt requests and channel-usage parameters between the computers. Once the block transfer is initiated, no further programming operations on the link control units are required until the transfer is completed.

Each of the interfaces of the DA11-B contains the following four addressable registers:

REGISTER	MNEMONIC	PROGRAM OPERATION	BUS ADDRESS
Word Count	DRWC	Read/Write	XXXX00
Bus Address	DRBA	Read/Write	XXXX02
Control & Status	DRST	Read/Write	XXXX04
Data Buffer	DRDB	Read/Write	XXXX06

Data Buffer
The Data Buffer performs two separate functions in the interprocessor channel. In Word Mode, the Data Buffer is used as a 16-bit addressable register to transfer information between computers under program control. It is loaded by the processor transmitting the word, then read by the other processor. The Request-interrupt bit (bit 3) of the Control and Status Register can be used to signal that data has been loaded by the transmitting processor. In Block Mode, the Data Buffer serves as an internal storage register that holds the word being transferred under NPR control.

Word Count Register
The Word Count register is initially loaded with the two's complement of the number of words to be transferred. The register increments toward zero after each bus cycle. When the Word Count overflows (all 1's to all 0's), the Transfer Complete bit in the Control and Status register is set and the transfer halts.

Along with the Extended Address bits (bits 5 and 4) in the Control and Status Register, the Bus Address Register is used to specify the bus address of the location to be transferred during DMA cycles. Because the UNIBUS link is only used to transfer full 16-bit words, bit zero of the Bus Address Register is always zero. The Bus Address Register is incremented after each bus cycle, advancing the address to the next sequential word on the bus. If the Bus Address Register overflows, the ERROR bit in DRST is set. Since Bus Address overflow does not increment the Extended Address bits, the maximum block that can be transmitted in one operation is 32K words.

Control and Status Register
The Control and Status Registers in the two interfaces are interconnected to provide a means of transferring channel status and interrupt requests from one processor to the other. Either processor can set up bits 1, 2, and 3 in its own Control and Status Register to indicate that it wishes to initiate a transfer. Setting these bits causes bits 9, 10, and 11 to be set in the companion processor's Control and Status Register (and an interrupt generated, if enabled) thereby informing the companion processor of the request for transfer. The bits of the Control and Registers are defined as follows:

BIT	NAME	FUNCTION
15	Error	Set to indicate an error.
14	NEX	Set to indicate an attempt to transfer

		data to or from a non-existent address.
13		Unused
12		Maintenance only.
11	Interrupt Requested	Set to indicate that the companion computer has requested an interrupt (by setting bit 3 of its Control and Status Register).
10	Requested Transfer Direction	Set to indicate that the companion computer wishes to receive data. Cleared to indicate that the companion computer wishes to transmit data.
9	Requested Transfer Mode	Set to indicate that the companion computer wishes to initiate a single-word transfer. Cleared to indicate that it wishes to transfer a block of data.
8	Cycle	Set to initiate the first transmit cycle from the requesting computer. Used in conjunction with the Go bit.
7	Transfer Done	Set at the completion of a transfer to indicate that the Link is ready to accept a new command. Forces the interface to release control of the UNIBUS and inhibits further DMA cycles.
6	Interrupt Enabled	Set to force a program interrupt whenever an Error (bit 15), an Interrupt-Requested (bit 11), or a Transfer-Complete (bit 7) condition occurs.
5	XBA17	Extended-Bus Address bits. Set to 00 for a transfer in the area 0-32K, 01 for 32K-64K, 10 for 64K-96K, 11 for 96K-128K.
4	XBA16	
3	Request Interrupt	Set to request an interrupt in the companion processor. Sets Interrupt Requested (bit 11) and Transfer Complete (bit 7) in the companion computer and causes an interrupt in the other computer if its Interrupt Enable bit (bit 6) has been set.
2	Request Transfer Direction	Set to request a transfer of data from the companion processor. Clear to request a transfer to it.
1	Request Transfer Mode	Set to request a single-word transfer. Cleared to request a block transfer.
0	GO	Set to initiate a transfer.

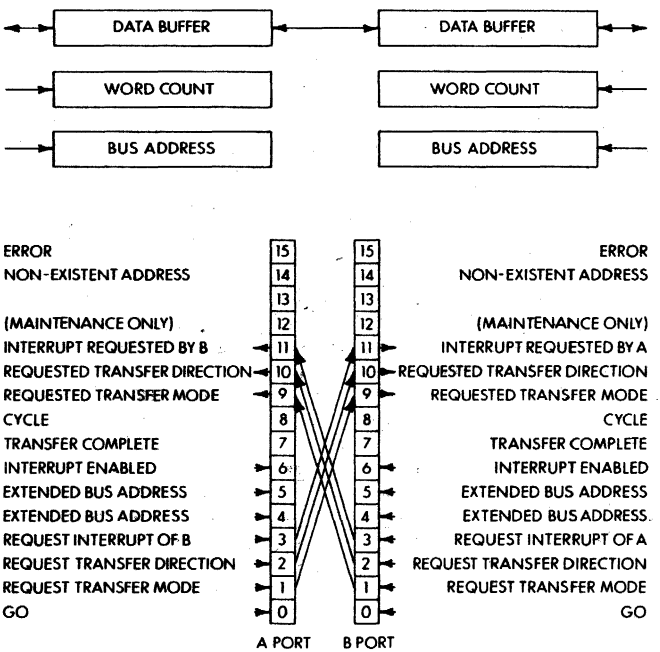
SPECIFICATIONS

Option Designations

DA11-BP DMA Bus Link—25 ft. (7.5 meter) cables

DA11-BE DMA Bus Link—50 ft. (15 meter) cables

	DA11-BF DMA Bus Link—100 ft. (30 meter) cables
Addressable Registers	Four in each interface: Word Count Bus Address Control and Status Data Buffer
Interrupt Vector	Requires one vector at location 124 (or assigned to floating vector field, location 300 and above)
Priority Level	BR5
Modes	Word or Block Transfer
Direction	Send or Receive
Word Size	16-bits parallel data
Maximum Block Length	32K words
Bus Loading	Each interface places a one-unit bus load on its UNIBUS.
DC Power	Each interface draws 4A (max.) from + 5V dc supply.
Installation	Each interface occupies one system unit and can be installed in any PDP-11 mounting box.
UNIBUS Compatibility	Can be used with any PDP-11 Family processor.



Control and Data Transfer Between the A Port and B Port of A UNIBUS Link

UNIBUS WINDOW, DA11-F

DESCRIPTION

The DA11-F UNIBUS Window is a high-speed interbus channel that connects two PDP-11 systems. Since it is a bus-to-bus connection, the DA11-F permits communications between any two devices on the two busses. And, since it operates on a cycle-by-cycle basis, it permits interbus DMA transfers as well as single-word accesses.

The UNIBUS window allows a PDP-11 system to access addresses on a companion system's UNIBUS as though they (the addresses) were on its own. It does so by automatically translating requests to a designated part of the bus-address space into requests on the other bus. Since all synchronization is done internally by the window hardware, the operation is completely transparent to the operating software.

Any unused block of addresses on the UNIBUS, from 512 to 32K words in size, may be designated as the window. Normally, it is placed directly above the last memory module. Thus, on a system with 64K words of memory, an 8K window would be placed from 64K to 72K. Once this window is initialized, any access to a location between 64K and 72K will be translated automatically into an access to an 8K address area on the companion system's UNIBUS. (The 8K area to be accessed on the companion's UNIBUS is selected as part of the window initialization process.) Thus, a window operation involves both the UNIBUS on which the access was requested, referred to as the originator bus, and the bus on which the access is actually performed, referred to as the target bus. Any type of address access (instruction fetch, data fetch, data write, or DMA-type block transfer) may be performed through the UNIBUS window. Once the window is set up, the interbus transfer is completely transparent.

Any device capable of being bus master may originate an access through the window. A processor on one side, for example, can execute code that is contained in the other computer's memory. Or a mass-storage device can transfer data to memory on the opposite bus. An individual processor is not limited to a single UNIBUS window; multiple windows allow inter-communication between several processors.

The window channel appears as a field of UNIBUS addresses on the originator bus. When the DA11-F recognizes a bus cycle addressed to a location within that field, it gains control of the target bus via an NPR request. The DA11-F then executes the same bus cycle but addresses it to the desired physical location on the target bus. A "through-the-window" transaction, therefore, is composed of a data transfer cycle on each bus. UNIBUS cycles operate as master-slave handshaking sequences. As a result, the DA11-F appears as a slave on the originator bus and as a master on the target bus.

The window field on the originator bus is fixed in size and in its location in the total bus-address space. The target space that the DA11-F can ad-

dress on the target bus is the same size as the window field but may be relocated, under program control, throughout the full UNIBUS addressing range (128K). A device on the originator bus could address its data transfer to the window field between 64K and 72K, but would actually gain access to target-bus locations between 32K and 40K. The relocation factor may, of course, be changed to point the window to any set of locations (starting on an even 4K boundary) on the target bus.

The DA11-F is a completely symmetrical unit and contains two of the window channels described above. Transactions may, therefore, originate on either bus and data may flow in either direction. To distinguish the two sides of the bus window, the UNIBUS interfaces are designated as the A Port and the B Port.

Each processor is given complete control over accesses to locations on its own bus. A programmable control unit within each port governs the use of the channel that originates on the opposite bus. The processor on the target bus can disable transfers through the window, restrict them to read only, and decide which addresses on its bus the window may have access to.

PROGRAMMING

Since each processor controls window operations directed at its own bus, the two computers must cooperate in establishing the access parameters for the window channels. Both cross-interrupt and cross-parameter transfer facilities are provided in the port-control units for interprocessor communication. Information can be passed via the control units without disturbing any on-going window-channel operations. Typical messages would request that a channel be opened, indicate whether it is to be read/write or read only, and set up the relocation factor to be used in calculating the target address. Once a channel has been opened, programs on the originator side can make random accesses through the window at any time with no further programming operations on the DA11-F control unit itself.

Each port of the DA11-F contains the addressable registers explained below:

	MNEMONIC		PROGRAM	
REGISTER	A PORT	B PORT	OPERATION	ADDRESS
Control and Status Word	ACSR	BCSR	Read/Write	XXXX00
Output Data Buffer	ADB	BDB	Read/Write	XXXX02
Input Data Buffer	BDB	ADB	Read Only	XXXX04
Displacement Address (Internal)	ADA	BDA	Read Only	XXXX06
Relocation Address	ARA	BRA	Read/Write	XXXX10
Starting Address	ASA	BSA	Read Only	XXXX12
Vector Address	AVA	BVA	Read Only	XXXX14

Control and Status Register

The Control and Status Registers on each port are interconnected to provide a means of transferring information, channel status, and interrupt

requests from one processor to the other. They also report error conditions due to illegal access by an originator bus or due to the inability of the window channel to complete a target bus cycle.

The bits of the Control and Status Registers are defined as follows:

BIT	NAME	FUNCTION
15	Error	Set if an access request from the originating bus fails. When the error bit is set, further window transactions originating on this bus are inhibited. If the Interrupt Enable bit (bit 6) is set, the error will cause an interrupt.
14	Timeout	Set on this port if a bus timeout occurs while the window is attempting to access a location on the opposite bus. Generally, the timeout is the result of attempting to access a non-existent target location in memory.
13	Power Failure	Set to indicate a power failure on the target bus.
12	New Data Loaded by Other Bus	When set, indicates that the opposite processor has loaded new information into its CSR (bits 11:9) or its Data Buffer. If Interrupt Enable (bit 6) is set, then loading new data causes an interrupt on this bus. The new-data bit can be set and cleared to signal successful passing of data. For example, if bit 0 (New Data for A) is set on the B port, a 1 appears at bit 12 of the A port. If Interrupt Enable (bit 6) on the A port is set, an interrupt request will be generated on the A bus. When the A processor has serviced the interrupt, it can clear the New-Data bit by writing a 0 into bit 12 of its own CSR. This action clears bit 0 of the B port CSR, thereby indicating that the message has been received.
11	Data 3 from Other Bus	Readout of contents of bits 5, 4, and 3 from the opposite port. Used to pass information bits and flags between computers.
10	Data 2 from Other Bus	
9	Data 1 from Other Bus	
8	Enable Transfer from Other Bus	Set to allow this port to be used as a target for transactions originating on the opposite bus. (Transfer Enable should only be set after Write Enable (bit 1) and

		the Relocation Address Register on this port are loaded correctly.)
7	Transfer to Other Bus Enabled	When set, indicates that an originator on this bus may perform a window transaction to the opposite bus, i.e., the target bus has set its Enable Transfer bit (bit 8). If this bit is clear, an attempt to originate a window transaction from this bus will cause an error.
6	Interrupt Enabled (IE)	Set to generate a program interrupt when an error occurs (bit 15) or when the companion processor loads new data (bit 12).
5	Data 3 for Other Bus	Loaded to pass information to the companion computer.
4	Data 2 for Other Bus	
3	Data 1 for Other Bus	
2	Writing to Other Bus Enabled	When set, indicates that the companion processor has allowed write access to its UNIBUS locations (i.e., the companion processor has set its bit 1).
1	Enable Writing from Other Bus	Set to allow the companion processor to change locations on the UNIBUS.
0	New Data	Set to indicate to the companion processor that either the Data bits (bits 11:9) or the Data Buffer on this port are loaded with new information.

Output Data Buffer

The 16-bit Output Data Buffer operates in two modes—either as an internal data-storage register during window transactions or as a cross-communication register during interprocessor program transfers. When the window is not enabled for transfers (bit 8 of the status register is cleared) the Output Data Buffer can be used to pass information to the opposite processor. Since data transfers can only be enabled by the target bus, the output data buffer provides a convenient way for the originator bus to request that a window be enabled.

Input Data Buffer

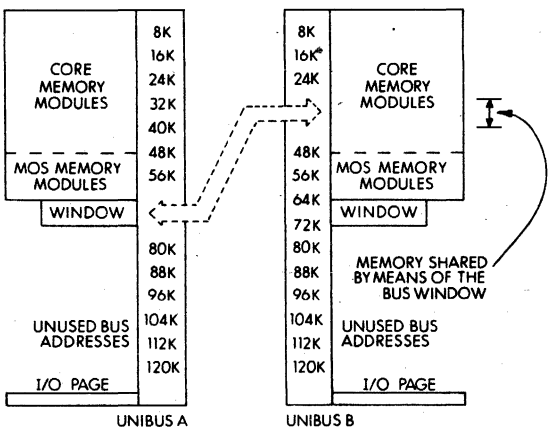
The 16-bit Input Data Buffer holds the contents of the Output Data Buffer from the opposite port. It permits the target bus to read data loaded by the originator bus.

Relocation Address Register

The Relocation Address Register specifies the high-order bits of a relocated target address, i.e., the area on the target bus to which the window points. It is loaded by the processor on the target bus. During a window transaction, the contents of the Relocation Address Register, shifted left by two bits, are added to the low order bits of the address

on the originator bus (that indicate the address within the window) to form an 18-bit target address.

Operation of the UNIBUS Window
(Simplified examples using identical processors and only one window port)



a. Example: A is the originating bus; B is the target bus. An 8K Window on UNIBUS A is located at 64K. It has been initialized to connect to locations 32-40K of UNIBUS B. System A executes a MOV X, R0 instruction where X is defined to be a location between 64K and 72K.

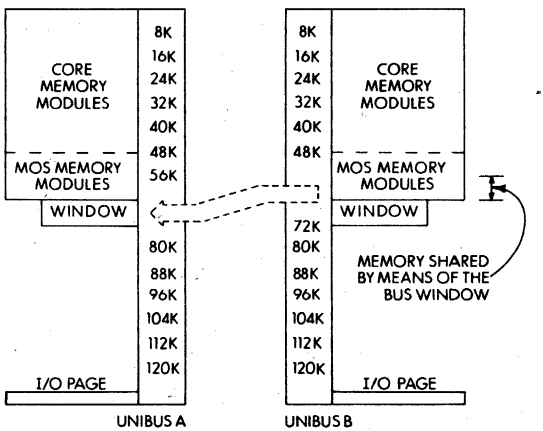
1. Processor A issues a request on UNIBUS A to fetch location X.

2. The window recognizes this as an address within its address boundaries (64K-72K). It therefore translates it into the appropriate address on UNIBUS B (an address between 32K and 40K) and issues a request on UNIBUS B to fetch that location.

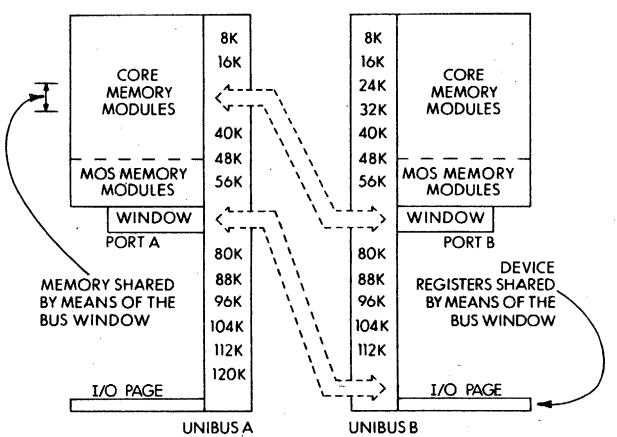
3. The data is fetched from UNIBUS B and passed to the window.

4. The data from UNIBUS B is transmitted to Processor A in response to the original fetch cycle on UNIBUS A.

5. The data is loaded into Processor A's R0, thereby completing execution of the MOV X, R0. The fact that the data actually came from System B's memory is transparent to Processor A.



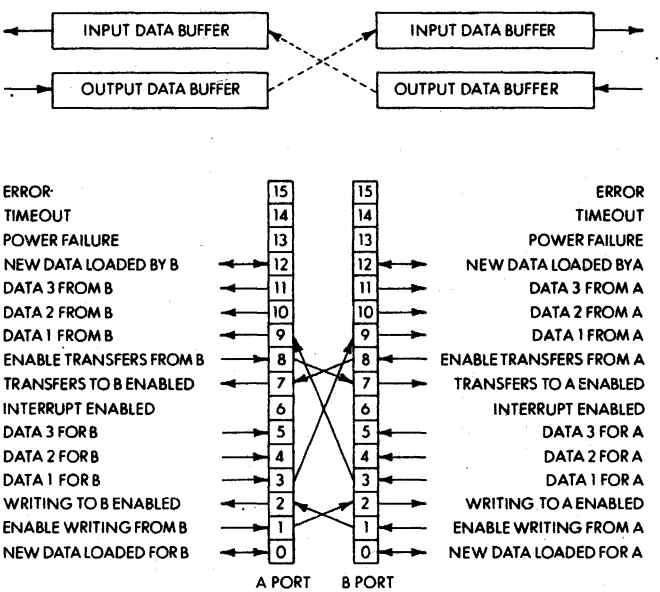
b. In this second example, the window has been reinitialized to point to locations 56K-64K on UNIBUS B. If the same MOV X, R0 instruction were repeated, the value of X would be fetched from System B's MOS memory instead of from its core memory.
Also, in this example, access to UNIBUS B has been initialized as read-only. An attempt to execute a MOV R0, X instruction would, therefore, result in a protection-violation trap.



UNIBUS Window Operation Utilizing Both Window Ports

In previous examples, only one direction of window transfer was diagrammed. The window actually implements two independent paths between busses. Having both windows enabled for reading and writing

allows each system to have shared access to part of the other system's memory. In this special case example, System A's window allows it to access device registers and hence initiate transfers on one or more of System B's peripherals. By doing writes to the appropriate locations between 68K-72K on its own UNIBUS (automatically translated by the window to actually load disk controller registers in System B's I/O page), System A may initiate an 8K transfer to locations 64K-72K on System B's UNIBUS. But this data would, in turn, pass through System B's window to locations 24K-32K of System A's memory. Thus, the window permits System A to initiate a transfer from System B's disk directly into its own memory on a completely transparent, DMA, basis.



Control and Data Transfer Between the A Port and the B Port of a UNIBUS Window

SPECIFICATIONS

Option Designation	DA11-F UNIBUS Window
Addressable Registers	Seven in each port: Control and Status Output Data Buffer Input Data Buffer Displacement Address (internal use only) Relocation Address

	Starting Address (maintenance)
	Vector Address (maintenance)
Interrupt Vector	Requires one vector assigned to floating vector field (location 300 and above)
Priority Level	BR7
Bus Loading	Each port places a one-unit bus load on its UNIBUS
Bus Latency	300-ns internal address-translation time plus time of the bus cycle on the target bus.
DC Power	Draws 5 amperes from + 5 V dc supply
Installation	Occupies one system unit and can be installed in any mounting box that accepts hex-height modules
UNIBUS Compatibility	Can be used with any PDP-11 Family Processor

BUS REPEATER, DB11-A

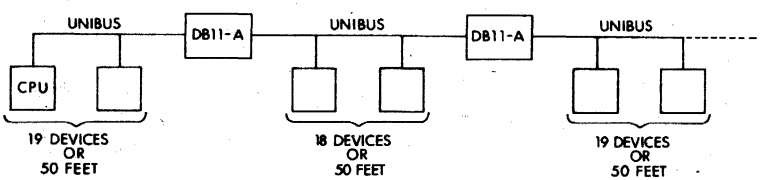
DESCRIPTION

The DB11-A Bus Repeater allows physical and electrical extension of the UNIBUS. Each DB11-A allows a 50-foot extension in bus length, and will drive 19 extra bus loads. Most PDP-11 options that interface to the UNIBUS are one bus load.

All UNIBUS signals are carried through from one side to the other by the DB11-A. Inclusion of a Bus Repeater in a PDP-11 system imposes no operational changes, and no timing restrictions. The operation is transparent to programming, and there are no addressable registers. The bus cycle time is unaffected for devices on the same side of the Repeater, and increase by only a maximum of 375 nsec for devices on the opposite sides.

Bus Loading

Each section of the UNIBUS is rated for 20 bus loads and a length of 50 feet. The DB11-A represents 2 bus loads, 1 on the input (CPU) side, and 1 on the output side. Therefore, the addition of one DB11-A allows a total of up to 38 devices (excluding the DB11-A), for a net gain of 18 bus loads.



DB11 Bus Repeater

SPECIFICATIONS

Increase in Bus Timing

Master and slave on same side:	0
Master and slave on opposite sides:	375 nsec, max

UNIBUS Interface

Bus loading:	2 bus loads (1 on each side)
Drive capability:	19 bus loads and 50 feet
Mounting:	1 System Unit (SU)
Input current:	3.2 A at + 5 V

Environment

Operating temperature:	5°C to 50°C
Relative humidity:	10% to 95%

PROGRAMMABLE ASYNCHRONOUS SERIAL LINE INTERFACE, DC11

DESCRIPTION

The DC11 series of character-buffered interfaces are used between the PDP-11 and a serial asynchronous line. They can be used to connect the PDP-11 to a variety of asynchronous terminals or to another computer through a common carrier communications facility. Also the communications facility can be bypassed and asynchronous terminal devices and other computers can be connected locally to the PDP-11. The DC11 has the flexibility to handle many different types of terminals. The line speed, character size, stop-code length, and the data set of control lines may be set under program control. Input and output line speeds can be varied independently.

The DC11 provides the necessary control signals and levels to interface to BELL 103 and 202 type modems or equivalent. The levels are EIA RS-232-C and CCITT compatible.

The PDP-11 UNIBUS serves as a multiplexer for adding multiple DC11s. Each two interfaces require one PDP-11 system unit's worth of mounting space. The pre-wired system unit and clock module are designated as the DC11-AA, DC11-AB, DC11-AC, DC11-AD, DC11-AE, DC11-AG, DC11-AH, or DC11-AX depending on the baud rates desired. The DC11-DA is the module set that interfaces the PDP-11 to a serial asynchronous line. Two DC11-DA's will mount in each DC11-A type unit. The DC11-A unit contains the clock for both DC11-DA module sets.

Operation

The DC11 is a character-buffered communications interface designed to translate asynchronous serial-bit stream data to parallel-character data. The units contain two independent character buffers (transmit and receive) capable of simultaneous two-way communication. Proper programming of each unit will allow it to operate in a half-duplex or full-duplex mode.

The receiver section offers serial to parallel conversion of 5-, 6-, 7-, or 8-level codes. The code size is under control of the program and appears right-justified in the data buffer without start or stop bits. Four different crystal-controlled clocking rates are available. When the character has been received, its parity is available to the programmer for testing. An interrupt request is generated in the middle of the last data bit of a character being received. If the program does not remove the character from the data buffer before the middle of the next start bit, a data overrun error is set in the device. Both the receiver and transmitter character length and stop-code size are simultaneously controlled by the program (i.e., they are always the same). The receiver interprets a break as a series of nulls.

The transmitter section offers parallel-to-serial conversion of 5-, 6-, 7-, or 8-level code. The transmission rate can be set by program control to one

of four rates independent of the receive rate. An interrupt request is generated in the middle of the last data bit being set. Also included is the ability to transmit a continuous space (break).

The control section provides connection to all the leads from Bell 103 and 202 type data sets, with the exception of data set ready. Control of the data set is done by the program. Interrupt requests are generated when rings appears or at the transition of carrier detect.

The control leads are fail-safe; i.e., they will appear off if the data set loses power.

Programming

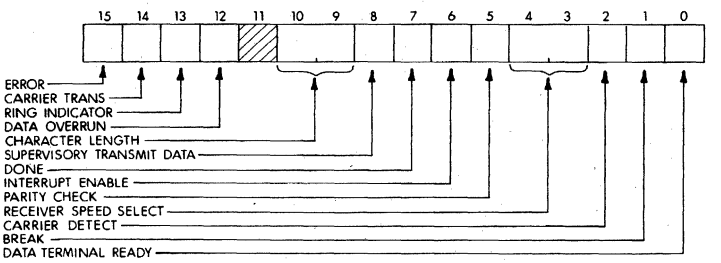
Each line unit contains four registers and, hence, requires four addresses. Address space has been assigned for 32 line unit. Line unit number 1 starts at 774 000, line unit 2 is at address 774 010, up to line unit 32 at addresses 774 370. The four registers and their address for line unit xx are:

REGISTER	ADDRESS
Receiver Status Register (RCSR)	774XX0
Receiver Buffer Register (RBUF)	774XX2
Transmitter Status Register (TSCR)	774XX4
Transmitter Buffer Register (TBUF)	774XX6

Each asynchronous modem interface requires one interrupt vector. The vector addresses are assigned from 300 to 777. (See Appendix A.)

Each DC11 has a bus request level assignment. All units will be shipped with the bus request line set to BR5. These levels are field changeable with a priority jumper plug.

Receiver Status Register (RCSR) 774XX0

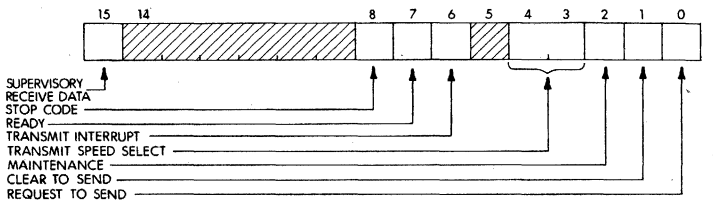


Effect of the Initialize (INIT) signal: clear bits 15 to 12, 10 to 3, and 1.

BIT	NAME	FUNCTION
15	Error	The logical OR of bits 12, 13, 14, causes an interrupt and is read only.
14	Carrier Transition	Set when carrier detect changes state. Cleared on read of receiver CSR. Read only.
13	Ring Indicator	Set when data set rings. Cleared on read of receiver CSR. Read only.
12	Data Overrun	Signals an error condition. Set when start pulse is received and done flag is still set. Cleared on read of receiver CSR. Read only.
10,9	Character Length	Specify the number of bits per character: BIT 10 / BIT 9 0 / 0 — 8 bits/char. 0 / 1 — 7 bits/char. 1 / 0 — 6 bits/char. 1 / 1 — 5 bits/char. Read and Write.
8	Superv. Transmit Data	Provides signalling capability on reverse channel of 202C/D modems. Read and Write.
7	Done	Indicates character available, and is cleared by reading the receiver buffer. Read only.
6	Interrupt Enable	Enables the receiver interrupt facility. Read and Write.
5	Parity Check	Provides a parity check to incoming data: Bit 5 = 1 Odd parity checks Bit 5 = 0 Odd parity fault Bit 5 = 0 Even parity checks Bit 5 = 1 Even parity fault Bit is read only and is valid until next character start pulse is received.
3,4	Receiver Speed Select	Specify the Baud rate of the receiver: BIT 4 / BIT 3 0 / 0 — Lowest 0 / 1 1 / 0 1 / 1 — Highest These bits are both read and write.

2	Carrier Detect	Control lead from modem. Indicates status of carrier and is asserted when channel is established. This bit is read only.
1	Break	When asserted, pulls the output data line to a space. This bit is read and write.
0	Data Terminal Ready	Control lead to modem. This bit conditions automatic answer and is both read and write. Must be set for register to assemble characters.

Transmitter Status Register (TSCR) 774XX4



Effect of the Initialize (INIT) signal: clear bits 8 to 6, 4 to 2, and 0.

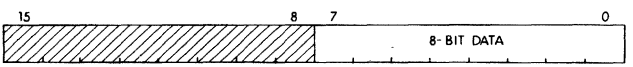
BIT	NAME	FUNCTION
15	Supervisory Receive Data	Provides receive capability on reverse channel of 202 C/D modems. Read only.
8	Stop Code	Sets the stop code sent by the transmitter: 0—Set stop code to 2 bits 1—Set stop code to 1 bit Read and write.
7	Ready	Indicates transmitter ready to output data. Cleared by loading transmitter buffer, set by having transmitter buffer zero'd. Read only.
6	Transmit Interrupt	Enables the transmitter interrupt facility. Read and Write.
4,3	Transmitter Speed Select	Specify the Baud rate of the transmitter

BIT 4	BIT 3	
0	0	Lowest
0	1	
1	0	
1	1	Highest

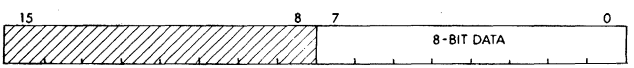
Read and Write.

2	Maintenance	Maintenance function which connects transmitter serial output to receiver serial input. Read and Write.
1	Clear to Send	Control lead from modem; required that this bit must be asserted for transmit interrupt. Read only.
0	Request to Send	Control lead to modem; required for transmission of data. Read and Write.

Receiver Buffer Register (RBUF) 774XX2



Transmitter Buffer Register (TBUF) 774XX6



SPECIFICATIONS

Operating mode:	Full- or half-duplex selected under software control.
Data Rates:	110, 134.5, 150, 300, 600, 1200, 1800 Baud or one user specified Baud rate between 600 and 10,000. Four speeds are available to the user under program control. Transmitting and receiving rates are independent. See DC11 models for specific combinations available.
Data Format:	One start bit. Character size is variable under program control to 5, 6, 7, or 8 data bits. Stop code is programmable to one or two bits.
Order of Bit Transmission:	Low order bit first.
Parity:	Computed on incoming data.
Distortion Input:	Can tolerate up to 40% per character.

Output:	Less than 3% per character.
Data Signals:	Conforms to EIA RS-232-C and CCITT specifications.
Control Signals:	All control leads from the Bell 103, 202 or equivalent modems are brought into the unit with the exception of data set ready. All leads are EIA RS-232-C and CCITT compatible.
Program Interrupts:	Receive done, transmit done, receive overrun, ring, and carrier transition. (If appropriate enable bits are set.)
Bus Load:	One line unit represents a one unit load to the PDP-11 UNIBUS. The UNIBUS can handle 18 unit loads. For more than 18 unit loads a bus extender, DB11-A, must be used.
Physical Connection:	25-foot cable with EIA RS-232-C-Compatible 25-Pin male connector.
Space Required:	1 systems unit for either one or two line interfaces.
Power Required:	2.2 amps of + 5 Volts for the first interface in a systems unit.
	2.0 amps of + 5 Volts for the second interface in a systems unit.
Temperature/Humidity:	10° -50° C with 20 to 90% noncondensing humidity.

Models

DC11-AA	Dual Serial Asynchronous Line System Unit and Clock. Provides space for mounting two DC11-DA Line Units. Clock gives 110, 134.5, 150 and 300 baud signals.
DC11-AB	Same as DC11-AA except Clock gives 110, 300, 1200, 1800 Baud signals.
DC11-AC	Same as DC11-AA except Clock gives 110, 150, 600, 1200 Baud signals.
DC11-AD	Same as DC11-AA except Clock gives 50, 110, 134.5, 150 baud signals.
DC11-AE	Same as DC11-AA except Clock gives 75, 110, 134.5, 150 baud signals.
DC11-AG	Same as DC11-AA except Clock gives 134.5, 150, 300, 1200 baud signals.
DC11-AH	Same as DC11-AA except Clock gives 110, 134.5, 600, 1200.

DC11-AX — Same as DC11-AA except Clock gives 110, 134.5, 150 plus one non-standard baud rate above 600 Baud and below 10,000 Baud.

DC11-DA — Full duplex serial asynchronous line unit with modem control features. Allows programmable variation of line speed character size, stop code length and data set control lines.

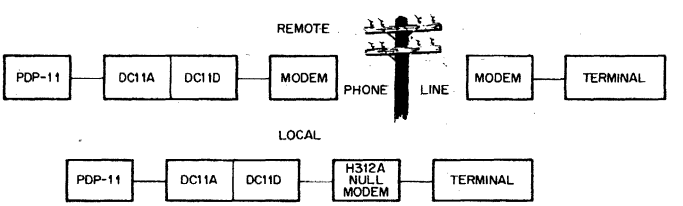
Transmitting and receiving speeds are independent. Data-set lines conform to EIA RS-232-C and CCITT specifications. Compatible with Bell 103, 202, or equivalent modems. Includes 25-foot modem cable.

H312-A — Asynchronous null modem jumper box. Allows direct connection of a PDP-11 to any peripheral with a data-set type interface which conforms to EIA RS-232-C and CCITT specifications. Also allows direct serial asynchronous computer-to-computer data transfers between two PDP-11's. Each PDP-11 must have a DC11-DA and the maximum separation must not exceed 50 feet.

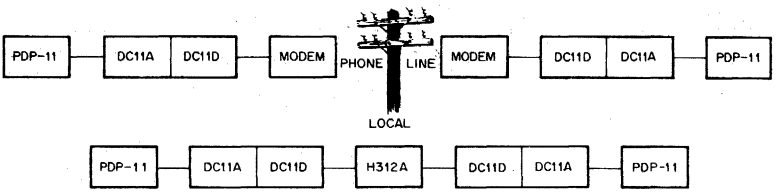
Applications

The DC11 is ideally suited for interfacing a moderate number of serial asynchronous lines to PDP-11 Systems. Applications of the PDP-11 such as numerical control, data acquisition, physics, biomedical and data processing often require several asynchronous serial line interfaces to be connected to either terminals or other computers. The DC11 is also a very flexible asynchronous interface for use in small time-sharing systems. Terminal manufacturers can easily interface the DC11 to their terminals provided they conform to EIA RS-232-C and CCITT Specifications.

The DC11 can connect a wide variety of terminals to the PDP-11 either remotely or locally. These configurations would be:



The DC11 also can connect two PDP-11's together. These connections which could be either remote or local would appear as:



PERIPHERAL MOUNTING PANEL, DD11

GENERAL

The DD11 Peripheral Mounting Panel is a pre-wired System Unit designed for mounting up to 4 Small Peripheral Controller (SPC) interfaces. It is pre-wired for logic and UNIBUS signals, and for power. The physical construction of the DD11 is similar to the BB11 Blank Mounting Panel.

Use of the DD11 requires specialized logic modules for the actual interface, since the pin assignments are fixed for the various control and data signals. Customers may design interfaces to go into a DD11 by using modules which have the same pin assignments for the signals.

There are two versions of the DD11, differing in only one functional aspect. The DD11-B is pre-wired for 2 DF11 interfaces, while the DD11-A is not.

DIFFERENCES

	DD11-A	DD11-B
1. Pre-wired area.	4 SPC slots.	4 SPC slots + 2 DF11 slots
2. Use with BA11-ES Mounting Box.	Must be used.	Cannot be used. (for power connection reasons)
3. Power Connections.	Module for power plugs into slot A3.	Tabs are used on the wire-wrap pin side.
4. Pin numbers CA1 to CV1.	Interconnected between slots 1 & 2, also 3 & 4.	Assigned to UNIBUS signals.

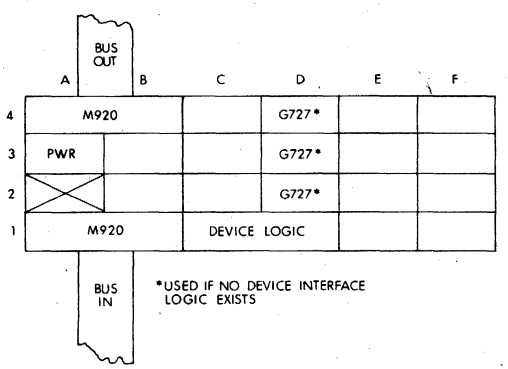
DD11-A

The following figure illustrates module allocation within a DD11-A unit. Slot A2 must be empty because of power cable overhang; slots B2 and B3 are unused. The DD11-A is wired to permit the installation of four M7821 modules in column F, four M105 modules in column E, and four double-height device interface modules in columns C and D or 4 quad module Small Peripheral Controllers (SPC's), which contain the equivalent of the M105 and M7821 plus the device interface logic. The unidirectional grant lines are wired to column D, and each device interface module must include jumper arrangements to allow selection of the device priority level at the time of installation. Only BR<7:4> levels are wired to this column; devices mounted in a DD11-A unit cannot be assigned to the NPR priority level without rewiring the panel. An additional constraint imposed on the interface is that each device may be on only one request level, since both interrupts available through one M7821 module are wired in series and must be at the same priority level.

If the device requires interface logic that occupies more than one full row of space in the DD11-A, columns C and D of the second row can be used by using wiring provided between rows 1 and 2 and rows 3 and 4. If this is done, it is no longer necessary to add another M105 and M7821 module to slots E and F of the second row.

UNIBUS—The UNIBUS enters through slots A1-B1 of the DD11-A. This connection can be made with either an M920 UNIBUS connector or a BC11A UNIBUS cable. All bus signals (except grants) are wired directly to corresponding pins in slots A4-B4. Connection can be made with either an M920 connector or BC11A cable to continue the UNIBUS to the next unit. If the DD11-A is the last unit on the bus, an M930 Bus Terminator must be placed in slots A4-B4.

Power—The G772 Power Connector plugs into slot A3. This connector distributes +5V power to all A2 pins and −15V power to all B2 pins except in slots A1, B1, A4, B4, A2, and A3. Ground is maintained through the frame and power connector on pins C2 and T1 of all slots.



DD11-A Module Layout

Note that a G727 Grant Continuity module must always be installed in column D if there is no interface logic in that row. The following figure shows the wiring assignments that must be adhered to when using the DD11-A.

Extended Usage—Additional wiring provides 10 signal lines between slots C1-D1 and C2-D2 as well as between slots C3-D3 and C4-D4. This permits use of multiple board device controls. Thus, if device logic can be divided into two sections with 10 or less interconnections between sections, then one section can be mounted in slots C1-D1 and the other section in slots C2-D2.

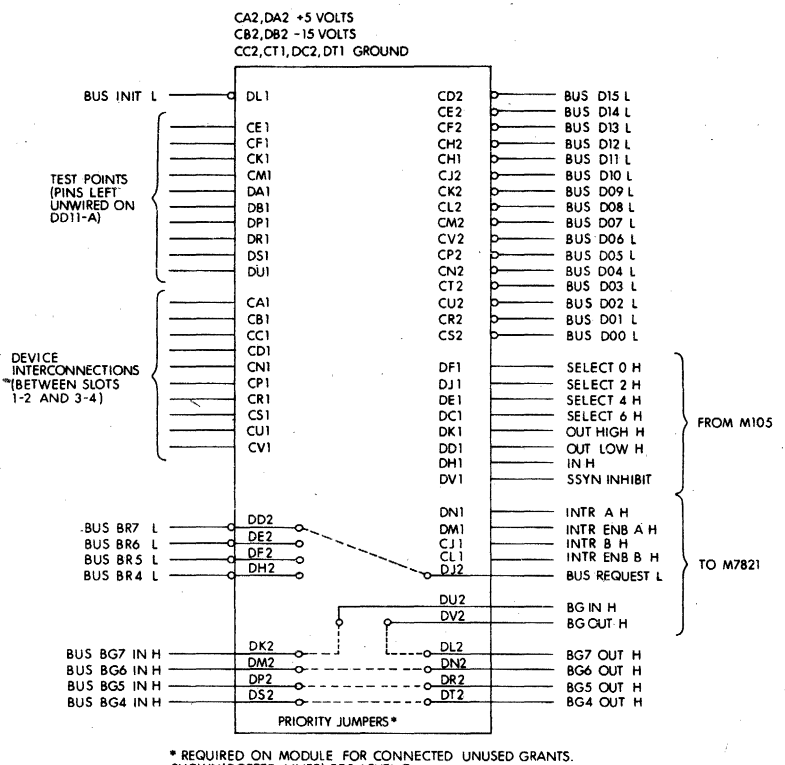
NOTE

Interconnections can be made only between rows 1 and 2 or between rows 3 and 4. No connections can be made between 1 and 3, for example.

Other sections of divided logic can also be placed into slots E and F with the interconnections provided by the normal M105 and M7821 module- to-device control signals.

CAUTION

When designing special logic, it is necessary to prevent interference with bus signals prewired to the pins of a particular slot.



* REQUIRED ON MODULE FOR CONNECTED UNUSED GRANTS. SHOWN(DOTTED LINES) FOR LEVEL 7

Device Control as Wired in the DD11-A

Grant Continuity—The device control module mounted in slots C1-D1 receives the bus grant signal from the UNIBUS. As a function of its interrupt priority level, this device control must switch the grant signal into its interrupt control (BG IN). After passing through both stages of the interrupt control, if not the interrupting device, the signal (BG OUT) must be returned to the grant chain and passed on to the next device control (mounted in slots C2-D2). In addition, the device control must maintain the continuity of unused grant signals. The BG OUT signals of C1-D1 are wired to the BG IN lines of the next device control. This grant chain must be continued through each device until the BG OUT signals of the last device control are wired to the outgoing UNIBUS in slots A4-B4.

Whenever slot D is not used by a device control, a G727 Grant Continuity module must be inserted in this slot. This module provides jumpers between pins K2 and L2, M2 and N2, P2 and R2, and S2 and T2. Three G727 modules and one M920 module are provided with the DD11-A unit.

External Device Cables—An edge connector mounted on the device control module permits connection to external devices. An H807 36-pin module socket may be mounted on the device control module and an M927 cable connector or M925 ribbon connector may be used. The M927 is used for coaxial cables or twisted pairs and is electrically equivalent to the M904 connector; however, the cable is mounted at the edge of the module card rather than at the end. The M925 is similar to M903 and is used for ribbon cable connectors.

DD11-B

The DD11-B can hold:

4 SPC's plus 2 DF11's

	A	B	C	D	E	F
4	UNIBUS CONNECTION		SPC			
3	DF11		SPC			
2	DF11		SPC			
1	UNIBUS CONNECTION		SPC			

ACOUSTIC TELEPHONE COUPLER, DF01-A

DESCRIPTION

The DF01-A Acoustic Coupler can be used to connect DIGITAL and other terminals to remote computing systems via ordinary telephone sets and the public switched telephone network.

Both 20 milliampere teletype current loop and EIA RS232C interfaces are standard in the DF01-A. The output from the interfaces can be used simultaneously, allowing the user to drive a plotter or other device requiring EIA interfacing while using a teleprinter for data input or output.

The DF01-A has built-in terminations for tying to the telephone company's Data Access Arrangement (Bell CDT Manual DAA) in the rare instances where a hard-wired connection is necessary to overcome interference or switchboard losses. Through pushbutton switches, the user may choose either acoustic or hard-wire and full- or half-duplex operation.

"Sound-seal" cushions on the DF01-A hold the telephone handset firmly in position and provide excellent acoustic shielding. Good durability is provided by an injection-molded case made of a special impact-resistant material. All electronic circuitry, switches, connectors and the sound-seal cushions are mounted on a single printed circuit board.

SPECIFICATIONS

Operating Modes: Originate-only, in half- or full-duplex.

Data Rate: Up to 300 Baud.

Receiver Sensitivity:—48 dBm in acoustic mode; —60 dBm hard-wire (DAA)

Frequencies:

	Send	Receive
Mark	1270 Hz	2225 Hz
Space	1070 Hz	2025 Hz

Frequency Stability: 0.3%

Modulation Technique: Audio Frequency—Shift Keyed (AFSK)

Transmit Power Level: —10 dBm

Line Coupling: Acoustic or hard-wire (Bell CDT Data Access Arrangement) coupling to telephone line.

Interface: 0 to 20 milliampere teletype levels or EIA RS232C (both available on the same unit; both outputs can be used simultaneously if desired).

Compatibility:
Used with remote terminals (teleprinter, typewriter, CRT display, plotter, card reader) to provide information transfer to/from a Bell 103A2 (or equivalent) dataset. Cannot be used with 230V, 50 Hz, nor is it compatible with European modems.

Power Requirement:	115V, 60 Hz (approximately 30W)
Operating Temperature:	32° to 140°F (0° to 60°C)
Size:	Width 6.5" (16.5 cm) Height 6" (15.2 cm) Length 12" (30.4 cm)
Weight:	6 lbs. (2.72 Kg)
Mounting:	Tabletop case

Controls and Indicators:
Power ON/OFF (pilot light integral with switch)
Acoustic/Hard-Wire Mode (pushbutton switch)
Full-Duplex/Half-Duplex (pushbutton switch)
Carrier ON indicator light

Cables: Supplied with 7.5 ft. (2.27 m) cable for connection to Model 33 ASR or KSR teletypewriter

A cable may be ordered (DEC No. BC05D-25) to connect the DF01-A to EIA terminals not already supplied with a cable.

Applications:
The DF01-A may be used to operate a standard DIGITAL LT33-B, D, E or H Teletype over the switched network. In the case of the LT33-D and E, connection to the DF01-A will disable the paper tape punch/reader. The reader may be enabled by DIGITAL field service personnel.

SERIAL LINE INTERFACE SIGNAL CONDITIONING, DF11

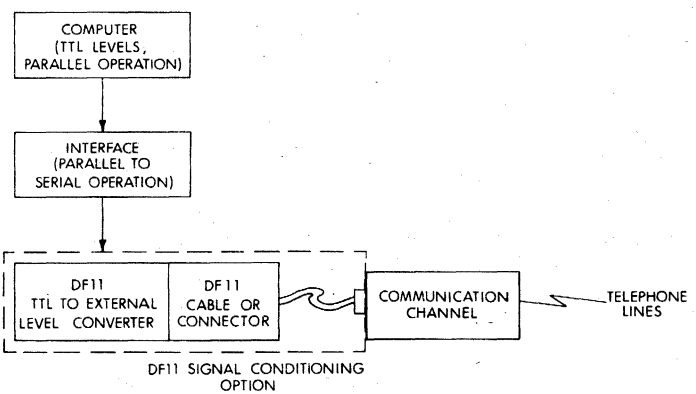
DESCRIPTION

The DF11 furnishes flexible, low-cost electrical and physical signal conditioning between most Digital-supplied serial line interface equipment and terminals, and commonly used serial communications channels. DF11 units are used with the following Digital serial line interface equipment: DC11, DP11, DL11, DH11, and LA30.

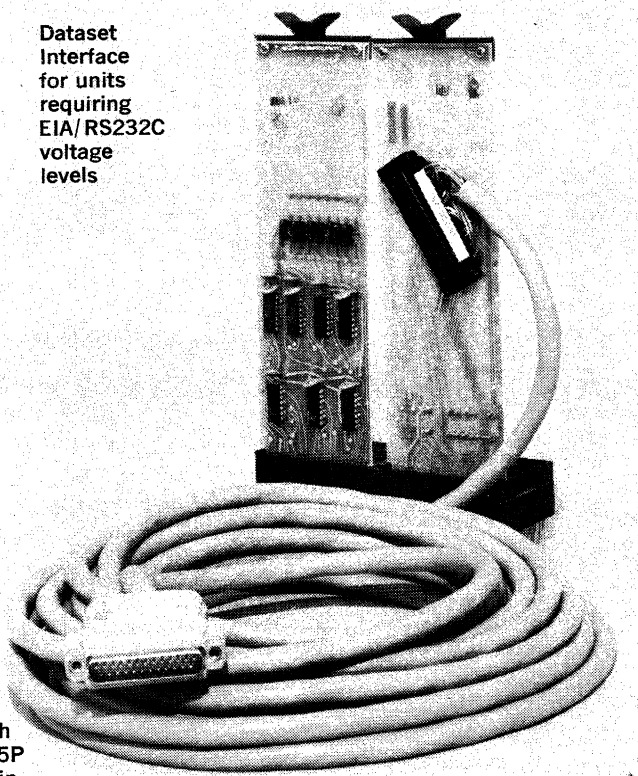
Most modern digital computers handle data signals as Transistor-Transistor Logic (TTL) levels. These levels must then be converted to other voltage levels or current values to prepare them for application to communications media so that they may be transmitted to a distant processor or terminal. In addition to the need for level conversion, there is a requirement to have cables of various lengths equipped with a variety of specialized fittings for each communications medium serviced.

CONSTRUCTION

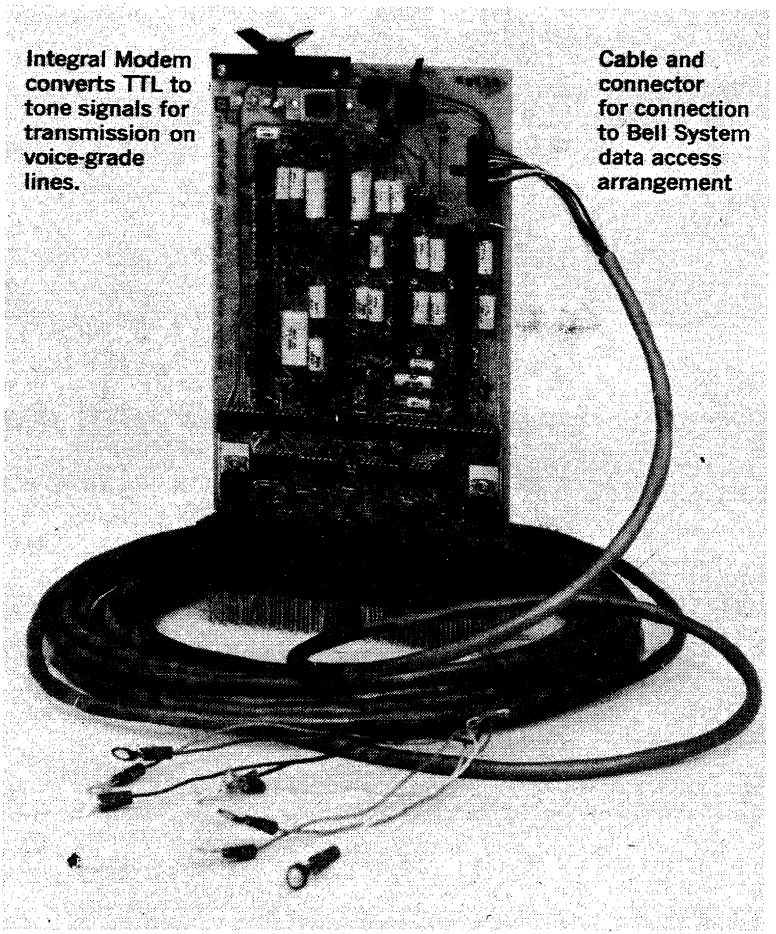
A DF11 unit will normally consist of two single-height modules. One module performs the electrical signal conditioning function of converting from the TTL signal levels internal to the computer logic to the external signal discipline required (e.g., EIA RS-232C, 20 mA Teletypes, Bell System CBS or CDT Data Access Arrangements, etc.). The second module performs the physical interface conditioning required; i.e., furnishes a cable to connect the level-converted signals produced by the first module to the desired device or channel (e.g., a dataset). In the case of the DF11-F 20 mA Teletype Interface, this second module provides a Mate-n-Lok connector for a customer-furnished cable. In the case of the DF11-A EIA Interface, the second module provides the 25-conductor cable and plug to connect the level-converted signals on the back panel wires to the dataset.



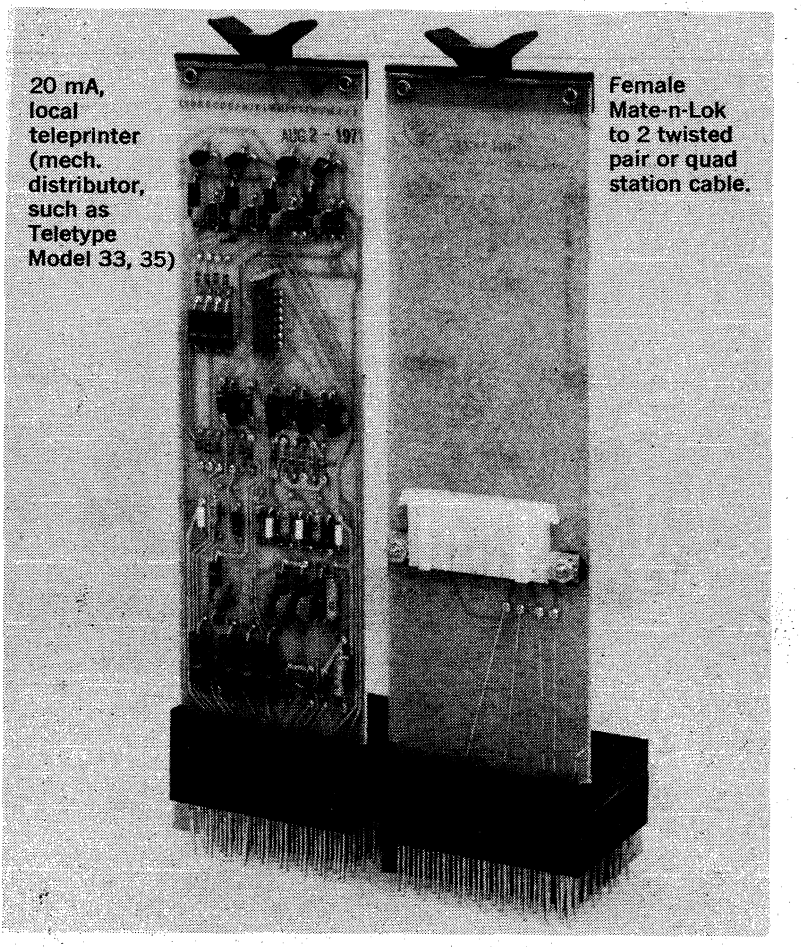
TYPICAL CONFIGURATIONS:



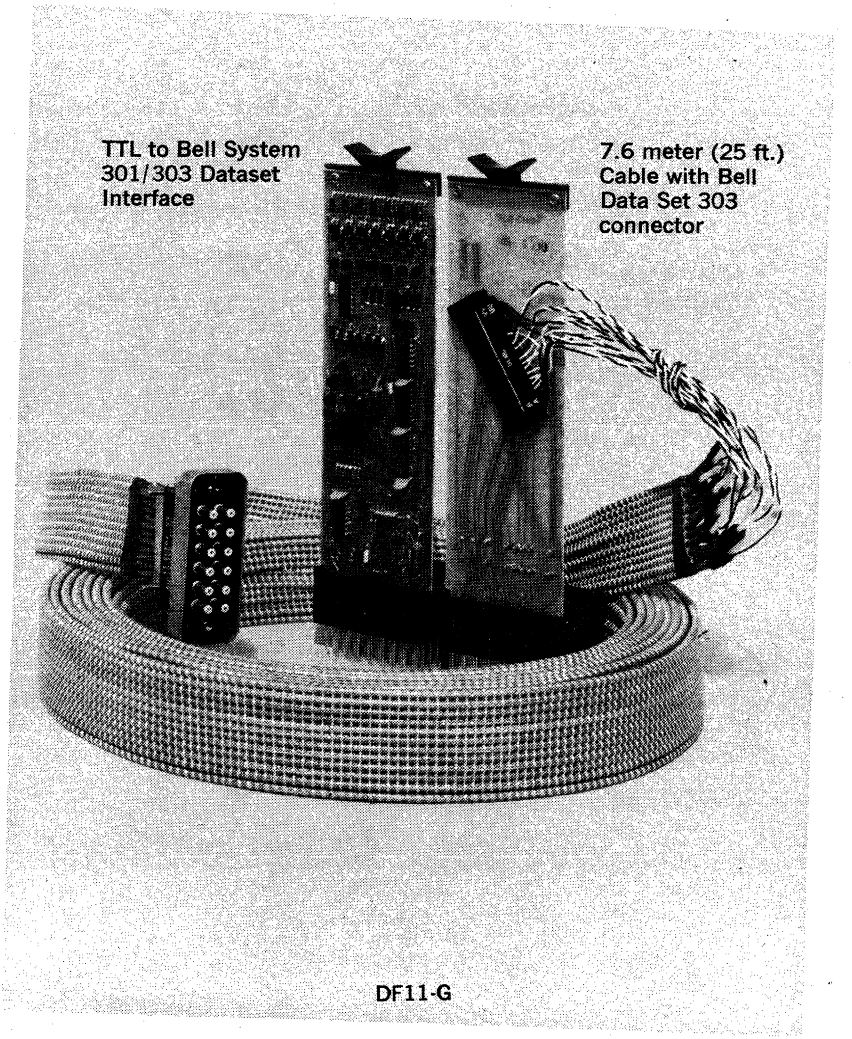
DF11-A

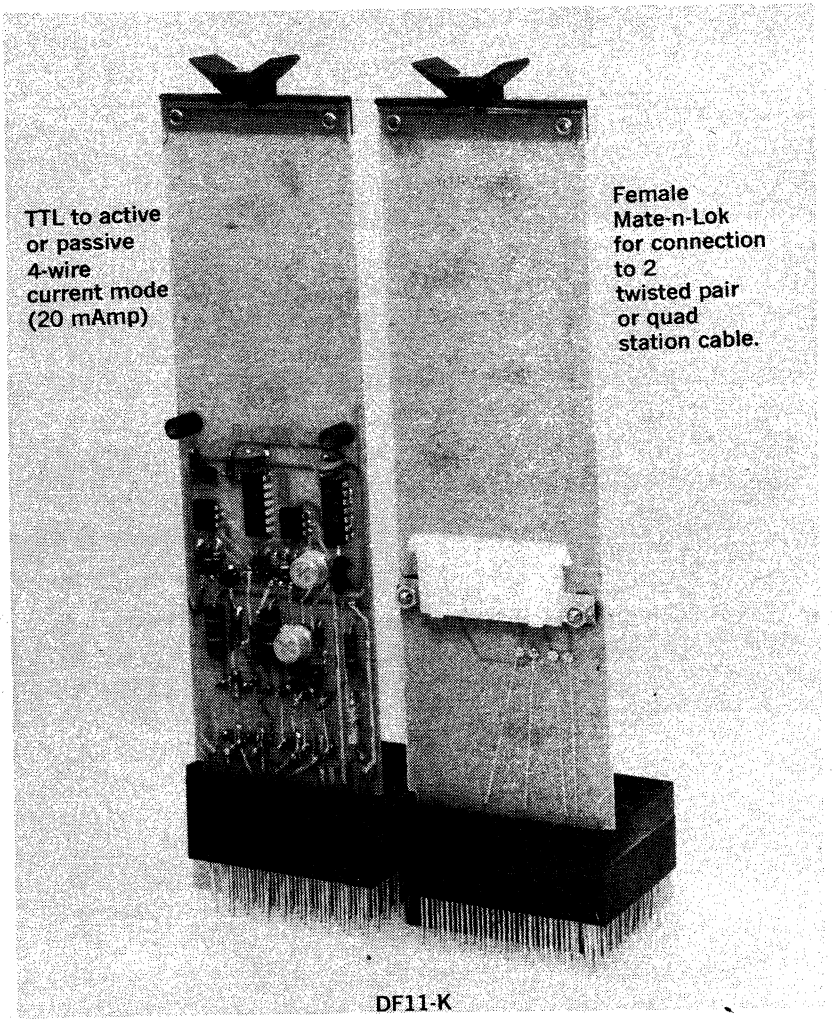

Integral Modem converts TTL to tone signals for transmission on voice-grade lines.
Cable and connector for connection to Bell System data access arrangement

DF11-B


20 mA, local teleprinter (mech. distributor, such as Teletype Model 33, 35)
Female Mate-n-Lok to 2 twisted pair or quad station cable.

DF11-F


TTL to Bell System
301/303 Dataset
Interface
7.6 meter (25 ft.)
Cable with Bell
Data Set 303
connector
DF11-G


TTL to active
or passive
4-wire
current mode
(20 mAmp)
Female
Mate-n-Lok
for connection
to 2
twisted pair
or quad
station cable.

DF11-K

MODELS

DF11-A—EIA ADAPTER
TTL to EIA/CCITT voltage levels. Connects to EIA circuits AA, AB, BA, BB, CA, CB, CE, CF, SBA, SBB, DA, CD, DB, DD, and C. Twenty-five foot cable with DB25P 25-pin male Dataset plug. Signaling rates up to 9600 Baud.

DF11-BA—INTEGRAL MODEM
Integral 103-type modem converts TTL to audio frequency shift keyed tone signals in the Originate-Only mode. Twenty-five foot cable and connector provided for connection with Bell System data access arrangement CDT or to private wireline channels. Signaling rate up to 300 Baud.

DF11-BB—INTERNAL MODEM
As above (DF11-BA) except unit operates in Answer-Only mode, and interfaces to Bell System data access arrangements CBS or CDT.

Note: The DF11-BA and BB may be used without data access arrangements on customer-owned lines, at distances up to 5000 ft.

DF11-F—TELETYPE ADAPTER
TTL to 20 mA active local Teletype loop. Connector is Amp Mate-n-Lok for connection with customer-supplied 22AWG, 2 twisted pair cable to local or remote (up to 1500 ft.) Model 33 or 35 Teletype. Signaling rates to 300 Baud.

DF11-G—303 DATASET ADAPTER
TTL to Bell System 301/303 Dataset Interface, Signal levels, cable connector, and signal pinning compatible with the Bell 301/303 Datasets. Supplied with 25-foot cable. Signaling rates to 250K Baud.

DF11-K—OPTICAL COUPLER
TTL to active or passive 4-wire current mode (20 mA) loop. Connector is Amp Mate-n-Lok for connection with customer-supplied cable. Signaling rates up to 2400 Baud, at distances up to 1500 ft.

Note: The data rates and distances cited above are recommended by DIGITAL. They are applicable in electrically quiet environments and do not necessarily represent limiting values.

APPLICATION

The DF11 series is applicable in most DECcomm-11 communications line interface equipment. The following is a partial list of line interfaces and mating DF11 signal conditioning options:

DL11*	DF11-BA, DF11-BB, DF11-K
DC11	DF11-A, DF11-F, DF11-K
DP11	DF11-A, DF11-G
DH11	DF11-A, DF11-BA, DF11-BB, DF11-F, DF11-K

* Available only when the DL11 is used in a DD11-B system unit, or in the top small peripheral controller slot of a PDP-11/10.

Related Options

H312-A	Null Modem—for connection of DF11-A directly to local EIA-compatible terminals.
959-A	Bag of 8 Male Mate-n-Lok connectors, with pins. For connection of customer-supplied cable with female Mate-n-Lok connectors supplied with DF11-F and DF11-K options.

16 LINE PROGRAMMABLE ASYNCHRONOUS SERIAL LINE MULTIPLEXER, DH11

DESCRIPTION

The DH11 multiplexer connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:

Character length:	5, 6, 7, or 8 bits
Number of stop bits:	1 or 2 for 6-, 7-, 8-bit characters 1 or 1.5 for 5-bit characters
Parity generation and detection:	Odd, Even, or None
Operating mode:	Half Duplex or Full Duplex
Transmitter speed (Baud):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.
Receiver speed (Baud):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.

Breaks may be detected and generated on each line.

The DH11 Multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the "silo." The bottom of the silo is a register which is addressable from the UNIBUS.

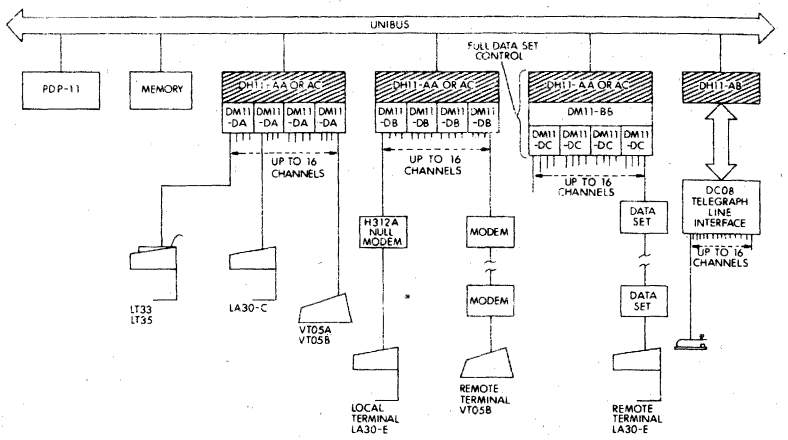
The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single cycle direct memory transfers (NPR). The current addresses and data byte counts for each line's message table are stored in semi-conductor memories located in the DH11. This reduces the UNIBUS time required for NPR transfers to one NPR cycle per character transmitted.

As many as 16 DH11's may be placed on a single PDP-11 processor, creating a total capacity of 256 lines.

Models Available

The DH11 Multiplexer is available in three variations:
The DH11-AA consists of a double system unit, all modules necessary to implement a 16 line asynchronous multiplexer, an externally mounted 14 cm (5¼ inch) level conversion and distribution panel with its own power supply that can be mounted on the rear of the rack, and a data cable between the logic in the double system unit and the level conversion/distribution panel.

The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements.



The DH11-AB is the same as the DH11-AA, but does not include the level conversion/distribution panel or its associated power supply. A data cable suitable for connecting the DH11-AB to the DC08CS telegraph converter panel is supplied instead of a cable to a distribution panel.

The DH11-AC is the same as the DH11-AA, except that the power supply for the level conversion/distribution panel is arranged for 240 V, 50 Hz operation. (There is no need for a 50 Hz version of the DH11-AB because it is a processor-powered option).

All versions of the DH11 include pre-wired slots in the double system unit for the insertion of the DM11-BB modem control (not included in the basic DH11).

Operation-Receiver

Reception on each line is effected by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40-pin MOS/LSI circuits which perform all the necessary functions for double buffered asynchronous character assembly.

The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a Mark-to-Space transition, the UART counts 8 clock pulses and checks the line. This sampling will occur in the center of a normal start bit. If the sample is a Mark, the receiver returns to its idling state, ready to detect another Mark-to-Space transition. If the sample is a Space, the receiver samples the line at subsequent sample points spaced 16 clock ticks from the center of the start bit. The number of samples taken is determined by

the "character length" information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver logic computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit will be set.

The character length, parity sense, number of stop bits, etc. that will be used by the UART to perform the above operations are stored within each UART in a Control Bits Holding Register. The Control Bits Holding Registers are addressable on a write-only basis from the UNIBUS, by first setting the "line selection bits" of the System Control Register and then loading the desired line parameters into the Line Parameter Register. Then they will automatically be transferred to the Control Bits Holding Register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.

The Silo

The silo is a MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16-bit word is entered at the top, and automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the Next Received Character Register.

There are three registers associated with the silo. The Next Received Character Register is a read-once register and is the bottom of the silo. Reading it extracts a character from the silo and causes all other entries to shift down one more position.

The other two registers are byte-size registers and are contained within the Silo Status Register. The high byte is read only and contains the status of an up-down counter giving the actual fill level of the silo. The low byte (bits 7-0) is read/write, and contains the number of characters which must be loaded into the silo before an interrupt request will be generated. Details of these registers can be found in the Section on Programming under the heading "Silo."

Received Character Distortion

Received characters may contain up to 43.75% distortion on any bit, due to the sampling rate. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark (if not, it's a "framing error") the error accumulated by that time must not exceed 43.75% of a bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error x number of data bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8% speed distortion would be permissible. Speed distortion (clock error, bit rate error) of any amount poses severe problems in an echo situation, however. If a terminal sends to the DH11 at a slightly fast rate and the DH11 sends the exact same characters back to the terminal at the correct rate, the DH11 silo will eventually fill with un-echoed characters. This problem would not occur with keyboard terminals, but high speed tape senders should have their

transmission speeds carefully checked before use with the DH11 or any other asynchronous communications interface. The acceptable tolerance is + 0, — 4%. In computing speeds, one may assume the DH11 receiver clock to be accurate within .05%.

Operation-Transmitter

Transmission on each line is also effected by means of UARTs. These 40-pin MOS/LSI chips perform all the necessary functions for double-buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a Marking state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART will generate a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by 5, 6, 7, or 8 data bits, as determined by the control bits holding register. (See Receiver Hardware for a description of the UART control bits holding registers and how they are loaded from the Line Parameter Register). The data bits are presented to the lines least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks.

The number of stop bits depends upon the setting of the control word. If the transmission of 6, 7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission is in 5-bit code, the program may select either one or one and a half stop bits.

If the transmitter's holding register has been loaded while a character was being transmitted, that second character will have its start bit commence immediately at the end of the preceding character's stop bit(s).

The transmitter timing circuit is driven by the same crystal clock as the receiver, and is accurate to .05%.

The Auto-Echo Feature

The DH11 hardware is capable of echoing received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register.

The auto-echo hardware is part of the receiver scanner and operates as follows:

1) If the receiver scanner finds a received character for a line on which auto-echo is NOT enabled, it loads that character into the silo and resumes scanning.

2) If the receiver scanner finds a received character for a line on which auto-echo IS enabled, it examines the error flags associated with that character.

   a) If a framing error is detected, the remote terminal may be trying to gain the attention of the processor by sending a "Break." In

this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software will be alerted. The Break is not echoed to the remote terminal.

b) If an overrun error is detected, this may mean that the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to 2a, above.

3) If the receiver scanner finds a received character from a line upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic will attempt to echo the character. First, however, certain tests of internal logic conditions will be made.

a) The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process will be tried again on the scanner's next rotation.

b) If the above test indicates no problem, the one remaining check is to see if the Transmitter Holding Register for the line on which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences.

It should be noted that it is not advisable to transmit messages on a line and auto-echo characters received on that line simultaneously. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, a data overrun will occur and characters will be lost. In short, auto-echo and software-driven transmission should not be attempted on the same line simultaneously if input from that line is expected.

Channel Interfaces

Multiplexer Distribution Panel and Power Supply:

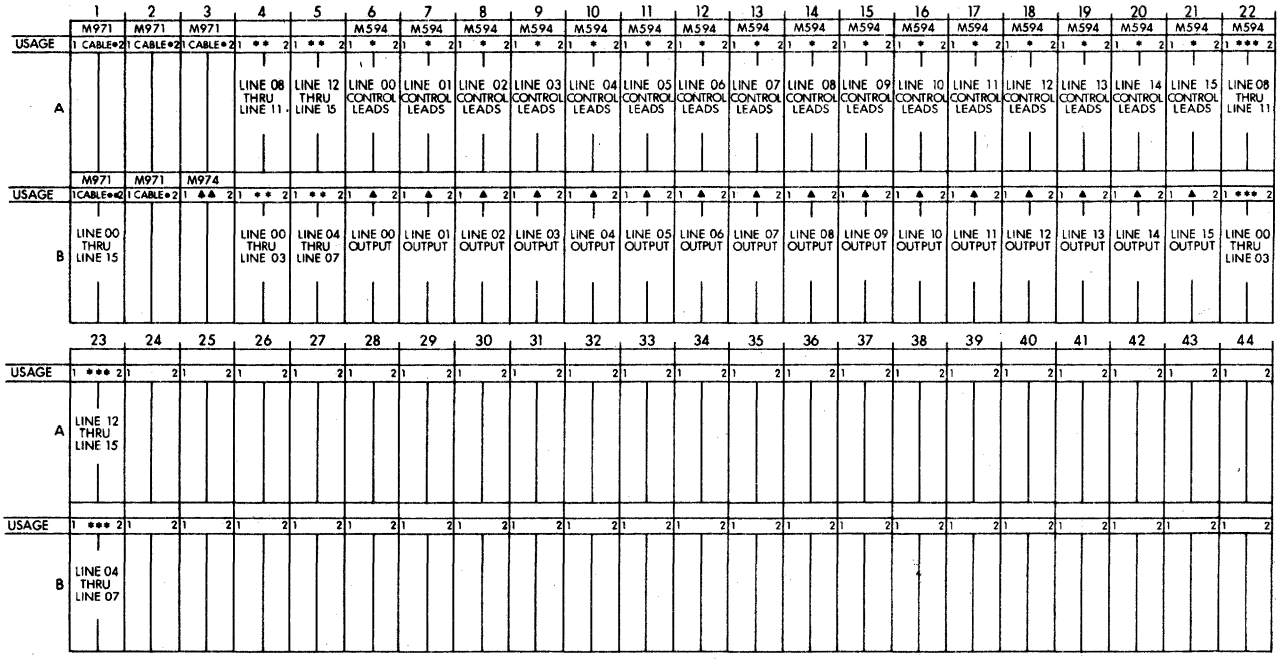
The DH11 provides a panel for level conversion and cabling of the individual line. The panel uses a standard H911 style rack, with 6 connector blocks:

Note that the slot assignments follow the DF11 (standard level conversion and cable slot for all PDP-11 communications products) format. Slot A6 through A21 is used for level conversion and slot B6 through B21 is used for cabling out. Other slots provide inputs or special purpose outputs. The unit mounts on the standard 48.3 cm (19 in.) cabinet and connects to the PDP-11 via the BC08-S data cable.

Power for the distribution panel is provided by the H751-C power supply mounted on the rear door of the cabinet.

The H751-C provides the following voltages:

+ 5 V at 4 A
+ 15 V at 2 A
— 15 V at 2 A



*LEVEL CONVERSION OF CONTROL LEADS. ONE SLOT PER LINE. USE M594 ONLY WHEN DM11-BB IS IMPLEMENTED. IF DM11-DB IS USED REPLACE M594 WITH W404-A (SUPPLIED WITH DM11-DB). IF DM11-DA IS USED LEAVE BLANK.

**USE M594 FOR DM11-DB

***USE M596 FOR DM11-DA

•USE ONLY IF DM11-BB IS IMPLEMENTED

••DATA CABLE FROM DH11-AA CONTROL LOGIC

▲16 CABLE SLOTS ONE PER LINE FOR DM11-DA USE M973, FOR DM11-DB USE BC01R-25

▲▲JUMPER CARD USED FOR DIAGNOSTIC PROGRAMS ONLY, REMOVE FOR NORMAL OPERATION.

Power drain of the distribution panel depends on the type of level conversion used. The maximum draw occurs when EIA levels are used with modem control (DM11-BB is implemented).

For this configuration the following power is used:

+ 15 V at 1.4 A
− 15 V at 1.4 A
+ 5 V at 1.7 A

Note that level converter types can be mixed on a 4-line basis by using different converters in slots A4, A5, B4 and B5. Also level converter types can be mixed on a single line basis by using slots A6 through A21 for level conversion on a single-line basis.

Programming

Double-Buffered Receivers—General

Double-buffered receivers contain two registers, one of which is a Shift Register. The character being received from the communications line is shifted into this register a bit at a time. The second register is a Holding Register. When the Shift Register has assembled a complete character, that character is transferred in a parallel fashion into the Holding Register. At that time a flag is set and the hardware or software using the double-buffered receiver can access the Holding Register and remove or copy the data stored there. When th Shift Register has assembled another character, that character will be transferred into the Holding Register, obliterating the character previously stored there. If this action takes place before the data in the Holding Register has been accessed, a Data Overrun flag will be set, indicating that data was lost.

Double-Buffered Receivers—DH11

The UARTs used in the DH11 are MOS/LSI units, each containing a double-buffered receiver and a double-buffered transmitter. In the DH11, the flags indicating presence of data in the receiver's Holding Registers are scanned by a automatic hardware scanner which copies data from the Holding Registers into the silo if storage space is available. (If that space is not available, and the scanner finds a flag indicating a holding register with data in it, the Storage Overflow bit (System Control Register, bit 14) is set, and an interrupt is generated. The setting of this bit does not necessarily mean that data has been lost. Rather, it indicates that data will be lost if the hardware scanner is unable to service (i.e. dump into the silo) the data in one or more Holding Registers before additional characters arrive on those lines. Actual data loss will become evident to the program when characters are received with the Data Overrun bit set. (See the description of the Next Received Character Register.)

Silo

The silo, actually more similar in operation to a granary, is a first-in first-out buffer store. A parallel-loaded 16-bit word (see Next Received Character Register for the format) automatically propagates downward into

the first location not already containing a word. In the case where the silo is empty, this means that the word would propagate directly into the Next Received Character Register.

The propagation time from the top of the silo to the bottom may be as much as 32 microseconds. For this reason, the hardware is arranged such that the Receiver Interrupt is not generated until the number of characters in the silo exceeds the silo alarm level AND there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo counts both those resting in the bottom and those propagating downward. While the hardware arrangement protects the case where the silo is empty and the alarm level is zero, the fact still remains that the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. For this reason, character handling programs should not assume there is some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the Valid Data Present bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as "1." At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another Receiver Interrupt is received.

On very fast processors, such as the PDP-11/45, the program should avoid reading the Next Received Character Register more often than once per microsecond, as it takes one microsecond for characters in the silo to shift downward one position. Since the typical program will be checking bit 15 and moving the character to some location in memory, it is not anticipated that this speed restriction will present a problem.

Zero Bauds
A speed selecton of zero bauds is provided so that the program may turn off any line. This is useful if excessive circuit noise on an unused line causes annoying quantities of bogus characters.

BREAK Signals
When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the SPACE (0) condition. The duration of this signal may be timed as described below.

The generation of a Transmitter Interrupt occurs when the last character of a message is loaded into a UART transmitter from a message table in PDP-11 core. At that time the program sets up a new message in core and loads the appropriate current address and byte count so that the new message can begin when the old one is finished.

It is important to note that the former message is not finished when the Transmitter Interrupt is given. Rather, the use of the core table is finished. In terms of the serial communications line, there are two more

characters left. One of these characters is in the UART transmitter's Shift Register; the other is in the UART transmitter's Holding Register.

Therefore, sending a Break signal requires loading two nulls and waiting for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a Break will not interrupt the transmission of any valid characters. In like manner, nulls should be used to time the transmission of a Break signal so that when the Break condition is terminated, no valid characters will be produced from the UART Shift and Holding Registers.

Interrupts
There are two kinds of receiver interrupts:

Receiver Interrupt (System Control Register, bit 7)

This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the silo status alarm level. (The program can determine the actual silo fill at any time by examining the high byte of the Silo Status Register.

Storage Overflow Interrupt (System Control Register, bit 14)

This interrupt, when enabled, occurs whenever the character storage silo is full and the DH11 hardware needs to store an additional character. This does not necessarily mean that data has been lost. (See the section on "Programming.")

There are two kinds of transmitter interrupts; both are enabled by bit 13 of the System Control Register:

Transmitter Interrupt (System Control Register, bit 15)

This interrupt, if enabled, occurs when one or more lines finish the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loads the last character to be transmitted (and hence that increments the byte count to zero).

Non-Existent Memory Interrupt (System Control Register bit 10).

This interrupt, when enabled, occurs whenever the DH11 addresses nonexistent memory; specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus, and fails to receive a slave sync response for that request within 20 microseconds.

Address and Vector Assignment
The DH11 uses floating addresses and is located after DJ11's in the floating address space that begins at location 760 010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11's in a system should have consecutive addresses.

Example #1: A system with no DJ11's but two DH11's:

760 010 Cannot use for DH11's because not multiple of 20.

760 020 First DH11
760 240 Second DH11
760 060 DH11 Gap (Indicates that there are no more DH11's).

Example #2: A system with one DJ11, two DH11's:

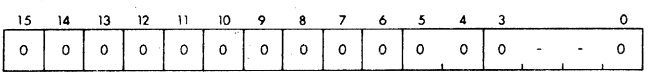
760 010 First DJ11
760 020 DJ11 Gap (Indicates that there are no more DJ11's).
760 030 Cannot use for DH11's because not multiple of 20.
760 040 First DH11
760 060 Second DH11
760 100 DH11 Gap (Indicates that there are no more DH11's).

The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C, D, E; DJ11; DH11.

The receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP11 priority jumper plugs. BR level 5 is standard.

Register Definition
The following chart presents the bit assignments within each register: Bits marked Unused and Write Only are always read as zero. Attempting to write into Unused or Read Only bits has no effect on those bits. INIT refers to the Initialize signal generated by the processor (e.g. upon execution of a RESET instruction.) Transmit and Receive are with respect to the DH11. All bits in the accompanying diagrams are shown in the state they assume on POWER CLEAR or INIT.

The System Control Register—Address X00



The System Control Register is a byte-addressable register. The bit assignment is as follows;

BITS DESCRIPTION

00-03 Line Selection

Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routing is accomplished by setting the Line Selection bits to the binary address (0000-1111) of the desired line. These bits are read/write.

04, 05 Memory Extension
The information stored in these bits becomes bits 16 and 17 respectively of any current address loaded by the program into the Current Address Register. These bits are read/write but, when read, represent only the status of bits 4 and 5 of the System Control Register, NOT the status of address bits 16 and 17 of the selected line. See the Silo Status Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

06 Receiver Interrupt Enable
This bit, when set, enables receiver interrupts (bit 7)

07 Receiver Interrupt
This bit, when set, indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the Silo Status Register. This bit is read only, except in maintenance mode, where it is read/write. Setting of this bit will generate an interrupt request if bit 6 (above) is also set.

08 Clear Non-Existent Memory Interrupt
This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write.

09 Maintenance
This bit, when set, places the DH11 in maintenance mode.

10 Non-Existent Memory
This bit is set whenever the NPR hardware places the addresses of a memory location on the UNIBUS and no slave sync is received in 20 μs. This indicates that the addressed location or device does not exist. This bit causes an interrupt request if set while Transmitter and Non-Existent Memory Interrupt Enable is set. This bit is read only, except in maintenance mode, where it is read/write.

11 Master Clear
This bit, when set, generates "Initialize" within the DH11, clearing the silo, the UARTs, and the registers. The exact bits cleared are discussed in the section on initialization. Read/Write.

12 Storage Interrupt Enable
This bit, when set, permits the setting of bit 14 to generate an interrupt request. This bit is read/write.

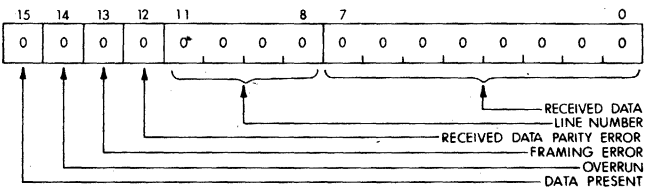
13 Transmitter and Non-Ex-Mem Interrupt Enable
This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt request. This bit is read/write.

14 Storage Interrupt
This bit is set when the receiver scanner finds a receiver holding buffer with a character in it, tries to store that character in the silo, and cannot do so because of a lack of space. When set this

bit will cause an interrupt request if bit 12 is set. This bit is read only, except in Maintenance Mode, where it is read/write.

15 Transmitter Interrupt
This bit is set when the DH11 concludes an NPR cycle that incremented a byte count to zero, indicating the last character in a message buffer was loaded into a UART transmitter Holding Register. This bit will cause an interrupt request if bit 13 is set. This bit is read/write. (It is set during an NPR cycle.)

Next Received Character Register Address X02



BITS DESCRIPTION

00-07 Next Received Character
These bits contain the next received character, right justified. The least significant bit is bit 00.

08-11 Line Number
These bits indicate the line number on which the next received character was received. Bit 8 is the least significant bit.

12 Parity Error
This bit is set if the parity of the received character does not agree with that designated for that line.

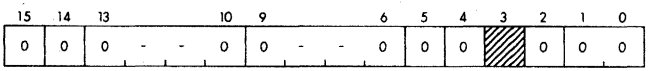
13 Framing Error
This bit is set if the receiver samples a line for the first stop bit, and finds the line in a spacing condition (logical 0). This condition usually indicates the reception of a Break.

14 Data Overrun
This bit is set when the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer. Refer to the section on Programming for further details on double-buffered reception.

15 Valid Data Present
This bit indicates that the data presented in bits 14-00 is valid. It permits a character handling program to take characters from the silo until it is empty. This is done by reading this register and checking bit 15 until a word is obtained for which bit 15 is a zero.

The entire Next Received Character Register is read-only and is addressable only on a word basis.

Line Parameter Register Address X04



This register should be loaded only after the line selection bits of the System Control Register have been set to select the line to which these parameters apply. This register is write only.

BITS DESCRIPTION

00-01 Character Length

These bits should be set as shown to receive and transmit characters of the length (excluding parity) shown:

bit 01	00	
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

02 Two Stop Bits

This bit, when set, conditions a line transmitting with 6-, 7-, or 8-bit code to transmit characters having two stop marks. If the line is transmitting 5-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.

03 Not Used.

04 Parity Enabled

If this bit is set, characters transmitted on this line will have an appropriate parity bit affixed, and characters received on this line will have their parity checked.

05 Even Parity

If this bit and bit 4 are set, characters of even parity will be generated on this line and incoming characters will be expected to have even parity. If this bit is not set, but bit 4 is set, characters of odd parity will be generated on this line and incoming characters will be expected to have odd parity. If bit 4 is not set, the setting of this bit is immaterial.

06-09 Receiver Speed

The state of these bits determines the operating speed for this line's receiver. The speed table below is applicable.

10-13 Transmitter Speed

The state of these bits determines the operating speed for this line's transmitter. The speed table below is applicable.

Speed Table for Receiver and Transmitter Speeds:

	Bit				
Transmitter	13	12	11	10	
Receiver	9	8	7	6	
	0	0	0	0	Zero Baud
	0	0	0	1	50 Bauds
	0	0	1	0	75 Bauds
	0	0	1	1	110 Bauds
	0	1	0	0	134.5 Bauds
	0	1	0	1	150 Bauds
	0	1	1	0	200 Bauds
	0	1	1	1	300 Bauds
	1	0	0	0	600 Bauds
	1	0	0	1	1200 Bauds
	1	0	1	0	1800 Bauds
	1	0	1	1	2400 Bauds
	1	1	0	0	4800 Bauds
	1	1	0	1	9600 Bauds
	1	1	1	0	External Input A
	1	1	1	1	External Input B

14 Half Duplex/Full Duplex

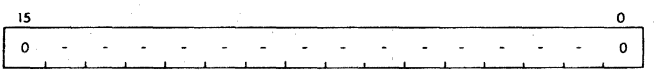
If this bit is set, this line will operate in half-duplex mode. If not set, this line will operate in full-duplex mode.

In this application half-duplex means that the DH11 receiver is blinded during transmission of a character.

15 Auto-Echo Enable

When this bit is set, characters received on this line will be hardware echoed. See the discussion of Auto-Echo for further details.

Current Address Register Address X06



This register should be loaded only after the System Control Register (SCR) has had the appropriate bits set to select the desired line number. When this register is loaded, address bits 00-15 are transferred into semiconductor memories in the DH11 from bits 00-15 of this register. Address bits 16-17 are transferred into semiconductor memories in the DH11 from bits 4-5 of the System Control Register.

Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Current Address Register.

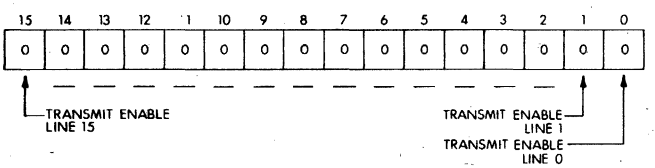
When this register is read, it will indicate the current address of the line selected by the System Control Register. Bits 16 and 17 will appear in the Silo Status Register, bits 6 and 7.

Byte Count Register Address X10

In the same fashion as the Line Parameter and Current Address registers, this register should not be loaded or read without first selecting a line number by means of the lower-order four bits of the System Control Register. This register should be loaded with the two's complement of the number of characters (bytes) to be transmitted on that line. The byte count register is read/write.

Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Byte Count Register.

Buffer Active Register (BAR) Address X12

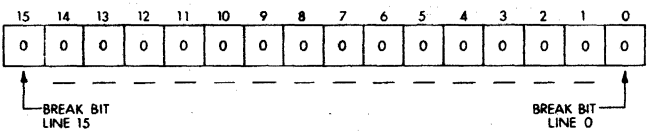


This register contains one bit for each line. The bits are individually set using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted is loaded into the transmitter Data Holding Register of the UART for that line. It should be noted that while the clearing of a BAR does indicate that a message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters will be sent after the BAR bit clears. These are the last two characters of the message; one of them was just starting when the BAR was cleared and one was that final character that was loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request to Send. Request to Send (RTS) should not be dropped until at least two character times after the BAR bit for a given line clears.

This timing may be effected by sending two extra (null) characters in a message and dropping RTS when BAR clears.

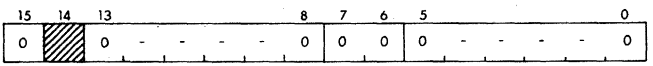
Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be set to zero. The Buffer Active Register bits are read/write.

Break Control Register Address X14



This register contains one bit for each line. Setting a bit in this register will immediately generate a Break condition on the line corresponding to that bit number. Clearing the bit will terminate the Break condition. The Break condition may be timed by sending characters during the Break interval, since these characters will never actually reach the line. Further comments concerning the transmission of Break signals may be found in the Break Signals Section.

Silo Status Register Address X16



This register is actually two byte-sized registers. The bit assignments are:

Bit Description and Operation

00-05 Silo Alarm Level

The program may load an integral power of 2 between 0 and 63 into this location (e.g., 0, 1, 2, 4, 8, 16, or 32). When the number of characters stored in the silo exceeds that number, an interrupt request (System Control Register bit 7) is generated, if System Control Register bit 6 is set. These bits are read/write.

06-07 Read Extended Memory

These bits are read only and contain the A16 and A17 bits of the current line address to which the line selection bits of the System Control Register are pointing.

08-13 Silo Fill Level

These bits are an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six bits, hence numbers between 0 and 63 can be represented. A full silo has 64 entries and the fill level appears as 00000, but one may easily tell the difference between an empty silo (00000) and a full silo (00000) by checking the Storage Overflow bit (bit 14 of System Control). These bits are read only.

14 Unused

15 Reserved for Maintenance

MODEM CONTROL MULTIPLEXER DM11-BB

In cases where the DH11 is used in public switched networks such as DDD, or TWX, the modem control multiplexer DM11-BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT electrical specifications.

DM11-BB Modem Control Option

Each DM11-BB modem control multiplexer contains two registers and requires two addresses. Address space has been assigned for 16 DM11-BB modem control multiplexers. The first DM11-BB is at 770500. The second starts at 770510, etc. to the 16th at 770670. The two registers and their addresses are listed below for DM11-BB unit xx.

Register	Address
Control and Status Register	770xx0
Line Status Register	770xx2

Each DM11-BB requires one interrupt vector. The vector addresses are assigned from 300 to 777.

All units are shipped with the bus request line set to BR4.

Control and Status Register (770XX0)

BIT	NAME	DESCRIPTION
15	Ring Flag	When DONE is set, this flag indicates that a Ring OFF to ON transition has been detected at line #--. This bit is read only and is cleared by Initialize and Clear Scan.
14	Carrier Flag	When DONE is set, this flag indicates that a Carrier Flag transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
13	Clear to Send	When DONE is set, this flag indicates that a Clear to Send transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
12	Secondary Receive Flag	When DONE is set, this flag indicates that a Secondary Receive transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
11	Clear Scan	Clears all Read/Write functions. Additionally, the Scan Decoder is set to 0 and the Scan Memory Logic is cleared. This function is useful for having

BIT	NAME	DESCRIPTION
		the Hardware Test and Interrupt on all lines that have an On condition (CO, CS, Sec T). Clear occurs when a ONE is written into this bit position.
10	Clear Multiplexer	Clear Multiplexer clears the request to Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops when a ONE is written into this bit position.
9	Maintenance Mode	The Scan Input (Ring, Clear to Send, Carrier, and Sec Rx) to a ONE or ON state Utilizing Step or SCAN EN with MAINT MODE will exercise 100% of the Scan Logic (not the data multiplexers). This includes the Interrupt Circuits (M7820) and the Address Selector (M105). This mode provides a diagnostic feature, as well as an on line test facility for the DM11-BB's interaction with the Unibus. This bit is Read/Write and cleared by Initialize and by Clear Scan.
8	Step	STEP, when set to a ONE, causes the Scan to increment the Line Number and test that line for interrupts causing transitions. Step may be used in place of Scan Enable but care should be exercised that the Scan rate is great enough (milliseconds) such that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1 μsec $\pm$ 10% to execute. This bit is Write One's only.
7	Done	The DONE flag set to a ONE indicates that the hardware SCAN has detected a transition requiring an Interrupt to the program. An Interrupt will occur if Interrupt Enable is on (a ONE). Additionally, DONE set to a ONE inhibits the SCAN clock and makes available to the programmer: (a) the Line Number that caused the Interrupt; (b) the status of the flags (4 bits); (c) modem status (8 bits). The SCAN will be released again when DONE is reset. This bit is Read/Write and cleared by Initialize and Clear Scan.
6	Interrupt Enable	Allow Interrupts on Priority four if set to a ONE. This bit is Read/Write and cleared by Initialize and Clear Scan.
5	Scan Enable	A ONE allows the scan to test all lines for Ring, Carrier, Clear to Send, and Sec. Receive Interrupts. If the SCAN EN flip flop is negated while the Ring Counter is cycling (i.e. DONE not set), the Ring Counter will come to rest in 1 μsec

BIT	NAME	DESCRIPTION
		± 10% (max). The LINE register must not be changed until BUSY (Bit 4) is cleared, or line number transitions may be lost. This bit is Read/Write and cleared by Initialize and Clear Scan.
4	BUSY	Set when Scan is cycling, Reset at end of Clear Scan or Init. Read Only. Must be tested for 0 before changing the registers.
3-0	Line Number	The LINE NUMBER bits are the Binary Addresses for the DM11-BB's 16 lines (0-15) as follows:

Bit 3210	Line #
0000	0
0001	1
etc	etc
1111	15

If the Scan is cleared by Initialize or Clear Scan, the Line Number Register will settle in 16 μsec 10%. When settled, the Line Number Register will be set to Line #0 (0000). NOTE: When the Scan is Enabled (or STEP) the next line to be tested will always be Line #1. These bits are Read/Write and cleared by Initialize and Clear Scan.

Line Status (770XX2)

7	Ring	Modem status of the Ring lead. This bit is Read Only.
6	Carrier	Modem status of the Carrier lead. This bit is Read Only.
5	Clear to Send	Modem status of the Clear to Send lead. This bit is Read Only.
4	Secondary Receive	Modem status of the Secondary Receive lead. This bit is Read Only.
3	Secondary Transmit	When set, presents a MARK to the modem's Secondary Transmit lead. This lead is Read/Write and is cleared by Initialize and Clear Mux.
2	Request to Send	This lead is used to condition the modem to transmit if all other conditions are met. This bit is Read/Write and cleared by Initialize and Clear Mux.
1	Data Terminal Ready	This lead allows the modem to enter and maintain data mode. This bit is Read/Write and cleared by Initialize and Clear Mux.

0	Line Enable	This bit enables the state of Ring, Carrier, Clear to Send and Sec Rx to be sampled by the program and to be tested for transitions. This bit is Read/ Write and cleared by Initialize and Clear Mux.

Maintenance Bits and Their Function

Setting of SCR 09 (Maintenance) does the following:

1.) It enables the program to write SCR07 (Receiver Interrupt). SCR 10 (Non-Ex-Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done.

2.) It loops the Transmitted Data leads (Serial Out, line 00-15) to the Received Data leads (Serial In, line 00-15).

Setting of Silo Status Register 15 (Silo Maintenance):

The setting of bit 15 in SSR causes the inputs of the silo to be set to a 1010101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 will repeat this procedure. All receiver speeds should be set to 0 and the silo emptied before this is done, so that no data from the incoming serial lines will be placed in the silo while it is under test.

Specifications

Function: The DH11 is a program-controlled interface between the PDP-11 UNIBUS and 16 asynchronous bit serial communications channels. The DH11 receiver section provides conversion of binary serial asynchronous (start-stop) signals to parallel binary data, and temporary buffering of that data. The DH11 transmitter section provides retrieval of parallel binary data from PDP-11 memory and conversion of that data to binary serial asynchronous (start-stop) signals for transmission over data communications channels.

Operating Modes: Each individual channel may be set to operate in half- or full-duplex mode, under program control. In half-duplex, the receiver for a channel is disabled during transmission of a character on that channel.

Any individual channel may be set, under program control, to echo (retransmit) received characters automatically.

Individual receivers may be continuously disabled under program control.

Data Format:

Asynchronous, serial-by-bit to/from the communications channel. Parallel-by-character to/from the UNIBUS. The serial data format is one start bit; 5, 6, 7, or 8 data bits; none or 1 parity bit (odd or even): and 1, 1½ (5 level codes only), or 2 stop bits per character. All data format parameters are individually program selectable for each channel. The data format for the receiver and transmitter on a given channel, however, is the same.

A one in any bit of a character presented by the program to the DH11 for transmission will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one in the Next Received Character Register, and a Spacing condition will be presented as a zero.

Order of Bit Transmission and Reception:

Low order bit first

Data Rates:

The operating data rate (Baud rate) of the receiver and transmitter on each channel is independently program selectable from among the following 14 rates:

0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600 Baud. In addition, any two other speeds between 40 and 110 Baud, and between 312.5 and 9600 Baud may be added as options, by ordering an M405 or M401 clock module at the proper frequency (desired bit rate x 16).

Distortion:

The DH11 receiver will operate properly in the presence of up to 43% distortion between any two code elements (intersymbol distortion). The long term (within any one character) speed variation of the received data may not exceed ± 4.3%, provided that the auto-echo feature is not used. If auto-echo is used, the long term (greater than one character time) speed variation of the received data may not exceed 0 to — 4%. The DH11 receiver clock is accurate to within ± .05% of the nominal data rate. The DH11 transmitter will introduce less than 2% intersymbol distortion, with a long term stability of ± .05%.

Physical Arrangement:	The DH11-AA and DH11-AC are comprised of a pre-wired, double PDP-11 system unit suitable for mounting in a PDP-11/40 or PDP-11/45 or equivalent cabinet; and all logic cards necessary to implement a 16-line multiplexer. Also included is an externally mounted distribution panel, 14 cm by 48.3 cm (5½ x 19 in.), with separate power supply for individual channel termination. The DH11-AA and -AC system unit and distribution panel are pre-wired for plug-in installation of the DM11-BB 16-line Data set Control Multiplexer. The DH11-AB is supplied without distribution panel, but with cables for connection to the DIGITAL DC08 Telegraph Line Subsystem Option.
Environmental Information:	The DH11 will operate at temperatures between + 5° and + 45° C, and at relative humidities between 0% and 95%, noncondensing.
Bus Loading:	Each DH11 presents 2 unit loads to the PDP-11 UNIBUS. The DM11-BB Data set Control Multiplexer, if present, represents one additional unit load.
Power Consumption:	The DH11 logic draws 8.4 A of + 5 Vdc, and 240 mA of — 15 Vdc. If the DM11-BB Data set Control Multiplexer is added, the total current drain is 11.2 A at + 5 Vdc.
Heat Dissipation:	56.4 kg cal/hr—DH11 alone 120 kg cal/hr—DH11 plus DM11-BB
Electrical Interface:	Connection between the DH11 logic and the distribution panel is via a cable containing 16 input and 16 output data lines at Transistor-Transistor Logic levels (0, + 5 Vdc). The logic levels are: Mark (logical 1) = 0V, Space (logical 0) = + 3 V. Input leads from the distribution panel are equipped with pull up resistors which clamp open input lines in a logical 0 (space) condition. However, logic in the DH11 receiver section prevents this from assembling continuous all-zero characters. The electrical and physical interface to the external channels is provided by optional level conversion module sets (DM11-DA, -DB, -DC) that plug into the distribution panel. These options are described in the next section.

Models

Connection to Switched Network (DDD Net) Data sets

DEC No.	PREREQUISITE	DESCRIPTION
DH11-AA	PDP-11	Programmable 16-line asynchronous serial line multiplexer and distribution

		panel, includes space for mounting up to four line adapters (16 line interfaces). Power requirement is 115 Vac, 60 Hz, 600 W.
DH11-AC	PDP-11	Same as DH11-AA except 230 V, 50 Hz, 600 W.
DM11-BB	DH11-AA or DH11-AC	16-line modem control multiplexer provides program operation of control leads for 103, 202 or equivalent data sets. Mounts in DH11-AA or DH11-AC.
DM11-DC	DM11-BB	Line adapter which implements four EIA/CCITT-compatible lines equipped with data set control features. Includes 25-foot data set cables.

Private Line Modems (No Control) or Local EIA Terminals

DH11-AA	PDP-11	See above -AA
DH11-AC	PDP-11	See above -AC
DM11-DB	DH11-AA or DH11-AC	Line adapter which implements four EIA/CCITT lines (data only). Includes four 25-foot modem cables. Note that the -DB can be used on a switched network system. This requires that the data set have Auto Answer strapped on. The data set will answer a call automatically. Not provided in this type of operation is the ability to not answer a call, the ability to initiate a disconnect by the computer, and the ability to sense an intermittent carrier.

Local Teletypes

DH11-AA	PDP-11	See above DH11-AA
DH11-AC	PDP-11	See above DH11-AC
DM11-DA	DH11-AA or DH11-AC	Line adapter for four 20 mA Teletype lines (data only).
DEC No.	Prerequisite	Description
DH11-AB	PDP-11	Programmable 16-line asynchronous serial line multiplexer and connecting cable to DC08CS mounting panel. (Does not include DC08CS.) Up to 2 DH11-AB's plug into one DC08CS.

DC08CS	DH11-AB	Telegraph or Telex line adapter distribution panel. Mounts line adapters for interfacing between the DH11-AB and telegraph or Telex lines. Accommodates up to 16 dual, solid-state telegraph line adapters, type DC08CM (Each DC08CM provides two telegraph line interfaces).
DC08CM	DC08CS	Dual solid-state telegraph line adapter; provides transmit and receive switching of two lines, in half duplex or duplex, neutral or polar operation. This unit is used with either externally supplied neutral or polar transmit and receive line power or internally supplied transmit line power (793 or 793A).
DC08EB	DC08CS	Line current adjusting option. Provides rheostats on each send and receive line for adjusting send and receive line current. Meter is provided for current monitoring.
DC08D	DC08CS	Line terminator panel. Provides screw terminal connection points for interfacing the DC08CM telegraph line adapters to telegraph lines. Can accommodate up to 32 lines with four connections provided for each.
793	DC08CM	Line power supply for driving a maximum of 32 telegraph lines (transmit only). Can drive unipolar or bipolar lines, ± 45 V to ± 80 V and 80 mA per line. For operation with 115 V, 60 Hz, 700 W.
793A	DC08CM	Same as 793 except 230 V, 50 Hz, 700 W.
893	DC08CS, DC08CM.	Fuse panel for up to 32 lines. Fusing for both transmit and receive lines.

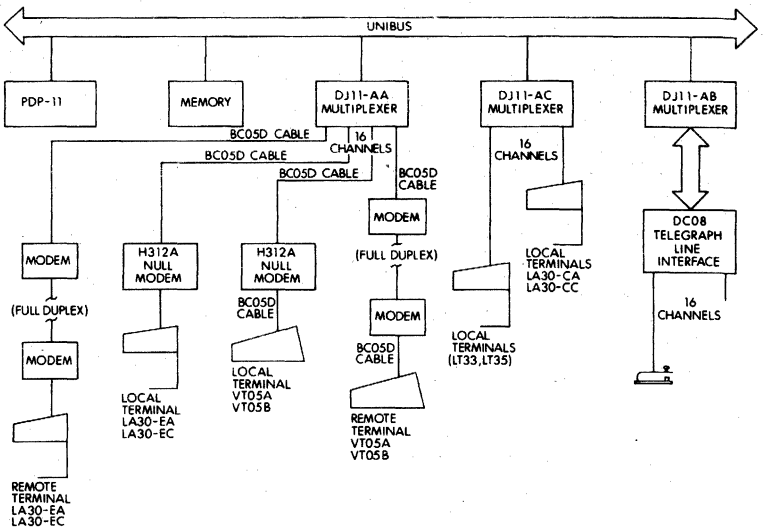
Related Options

The following options are useful in connecting various terminals and channels to the DH11.

Option No.	Prerequisite	Description
H312-A	None	Null modem. Required for local connection of terminals with EIA-compatible interfaces such as the DIGITAL

		VT05B, LA30EA, the Hazeltine 2000, etc., to the standard DM11-DB or DM11-DC modem interface.
BC05D-15	None	Modem cable. 7.6 m, 25-conductor cable terminated in Cinch DB25S socket at one end and Cinch DB25P plug at the other. Used to extend standard DM11DB or DM11DC modem cable.
DF11-BB	DH11-AA, DH11-AC	Integral Modem. Single line, answer-only, integral modem which plugs into the DH11-AA distribution panel. It is compatible with Bell 103A and 113A datasets. The DF11-BB connects to a Bell System type CBS or CDT Data Access Arrangement.
DF11-K	DH11-AA DH11-AC	Current mode interface. This is a TTL to active or passive 4-wire current mode (20 mA) loop converter. Connector provided is Amp Mate-n-Lok for connection with customer-supplied cable. Signalling rates up to 2400 Bauds, at distances up to 1500 feet.
M405		Clock Card. Required to provide non-standard speed (Ext. A or Ext. B) for DH11. M405 frequency ordered should be 16 x desired Baud rate. Minimum rate is 312.5 Bauds, maximum is 9600 Bauds.
M401		Clock Card—as above except minimum rate is 40 Bauds, maximum is 110 Bauds.

16-LINE ASYNCHRONOUS SERIAL LINE MULTIPLEXER, DJ11

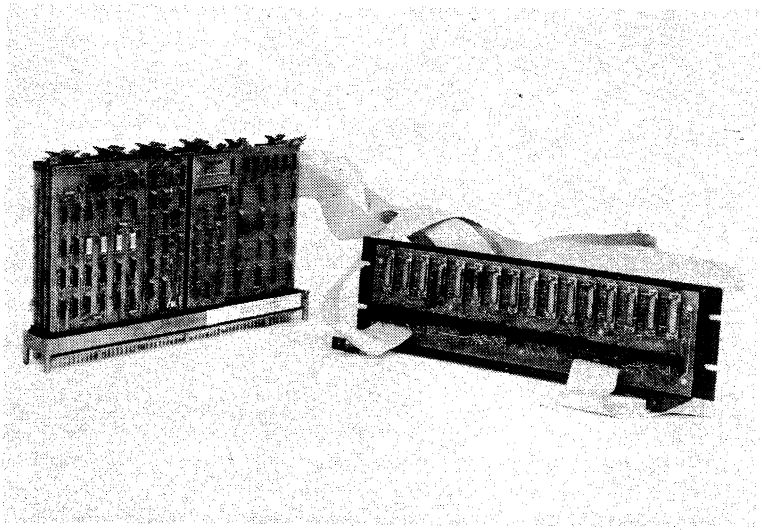


The DJ11 is a multiplexed interface between 16 asynchronous serial data-communications channels and the PDP-11 UNIBUS. The DJ11 is a low-cost, high-performance unit whose character formats and operating speeds are jumper or switch selectable in groups of four lines. The customer may select from 11 standard speeds (75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, or 9600 Bauds); four character sizes (5, 6, 7, or 8 data bits); three parity configurations generated and checked by the hardware (odd, even, or none); and three stop code lengths (1 and 1½ stop bits for 5 data bits. 1 and 2 stop bits for 6, 7, or 8 data bits), also generated and stripped by the hardware.

MODELS AVAILABLE

Three models of the DJ11 are available, differing only in the type of input/output level conversion they provide.

The DJ11-AA furnishes level conversion conforming to the Electronic Industries Association (EIA) Standard RS232C, and to CCITT Recommendation V.24, supporting Transmitted and Received Data leads only. The Data Terminal Ready and Request To Send leads are permanently asserted (ON). The DJ11-AA is suitable for connection to local terminals with EIA interfaces, to private-line modems, and to dial network data sets, where computer control of the data set is not required. An externally mounted interface panel with 16 Cinch DB25P EIA connectors is provided for attachment of data set cables (not supplied).



The DJ11-AB is supplied without level conversion, but with cables which bring the TTL signals out of the mounting cabinet. This allows connection to external signal-conditioning equipment, such as the DIGITAL-supplied DC08 Telegraph Line Interface Options, and customer-supplied special interface equipment.

The DJ11-AC furnishes 20-milliampere active neutral current-loop level conversion, suitable for operating DIGITAL-supplied terminals, such as the LA30-CA and LA30-CD DECwriters, VT05A and VT05B Display Terminals, LT33 and LT35 Teletypewriters, and RT01 or RT02 Data Entry terminals. An externally mounted distribution panel with 16 four-screw terminal strips is provided for connection of customer terminals.

OPERATION:

General

The DJ11 is a buffered, multiplexed interface between 16 asynchronous serial communications channels and the PDP-11 UNIBUS. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with double character buffered MOS/LSI circuits called UART's (Universal Asynchronous Receiver Transmitters). These circuits provide the logic necessary to double buffer characters in and out, to serialize-deserialize data, to provide selection of character length and stop code configuration, and to present status information about the UART and each character. A 64-character, first-in/first-out buffer is provided in the hardware to hold characters as they are received.

Receiver

The receiver section performs serial-to-parallel conversion of 5-, 6-, 7-, or 8-level codes. The desired character length is switch selectable in four-line groups. That is, all lines within each group of four lines (lines 0-3, 4-7, etc.) will expect the same character format, i.e., number of data bits, duration of stop element (stop code) and parity sense. For any line, the character format is the same for both the received and the transmitted data. The receiver data rate (Baud rate) is jumper selectable from among 11 standard speeds, also in four-line groups. These speeds are 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. The receiver data rate for any four-line group may be different from the transmitter data rate for that group. Each receiver samples the line at 16 times the data rate.

The duration of the stop element is switch selectable, again in four-line groups. Values available are 1 or 1½ bit times for characters with 5 data bits, and 1 or 2 bit times for characters with 6, 7, or 8 data bits.

As each character is received, it, along with the four-bit number of the line it came from and four bits of status information, is stored in a 16-bit wide by 64-word deep first-in/first-out hardware buffer, called a 'Silo.' This storage occurs at the time the center of the first stop bit of the character is sampled. Each complete character is loaded into the top of the silo and propagates (falls) automatically toward the 'bottom' of the silo, until it comes to rest against the bottom, or against the last previous character stored in the silo. The bottom of the silo is actually the Receiver Buffer Register (RBUF) and is seen, by the program, as a device register on the UNIBUS. Thus, there are no accesses to the UNIBUS at all until a complete character is received, stripped of start and stop bits, checked for proper parity (if required), and stored in a hardware buffer.

Indications of character words available from the silo and of device status are provided to the program by the Control Status Register (CSR).

The exact definition of each bit in CSR is given in the section on Programming, but the functions of the bits related to the DJ11 receiver section are discussed in the following paragraphs.

At the time a received character word appears in RBUF the Receiver Done bit (bit 7) is set in the CSR. If the Receiver Interrupt Enable bit (bit 7) is also set in CSR, an interrupt request is generated. The BR level is set by a priority jumper plug, and is the same for receive and transmit. BR 5 is standard.

In order to operate on received characters, the program tests bit 15 of RBUF for a 1 (data present). If bit 15 is set, the program moves the word from RBUF. This causes the silo to shift, automatically, all other characters it may contain 'down' one position, with the next received character appearing in RBUF not more than 1.4 μs later. Thus the program may disable received character interrupts, entering the receiver service routine on a timed basis and 'clearing out' the silo each time, or it may respond to an interrupt on each character.

The parity sense for received data is switch selectable in four-line groups. The DJ11 offers a choice of odd, even, or no parity. If odd or even parity is selected, the receiver assumes that the bit received after the nth data bit (where n is the number of data bits selected) is the parity bit, and compares that bit with the parity of the n received data bits. If the parity is correct, the parity bit is discarded, and the n data bits are retained and placed in the received character buffer (silo). If the parity is incorrect, the hardware will set the Parity Error bit (PE, bit 12) of the received character word before storing it in the silo. If no parity is selected for a particular line group, parity is not checked and bit 12 will never be set.

Note that if odd or even parity is selected, the total character length is the sum of the start bit, plus the number of data bits selected, plus the parity bit, plus the number of stop bits selected.

If, at the time the center of the first stop bit should appear on a particular received data line, that line is found to be in a spacing (0) state, the Framing Error bit (FE, bit 13) will be set in the received character word. Such a condition may occur, for instance, if the data line goes open, or if the terminal connected to that line transmits a Break signal. In these cases all bits of the data character will be zero. Succeeding all-zero or Break characters, however, will not be assembled by the UART on that line or put into the silo. The received data line must return to a marking condition for 1/16 of a bit time before character assembly is resumed.

The Overrun bit (OR, bit 14) is an indication that the DJ11 receiver scanner has failed to remove a completed character from the UART before the next character was moved in on top of it. This only occurs if the silo has completely filled, and the program fails to respond to a FIFO Full flag. Since each UART is double buffered (32 complete characters), in addition to the 64-character silo buffer, this condition is unlikely to occur unless the program servicing the DJ11 is faulty. By means of a split-lug jumper, the DJ11 can be wired to give a Receiver Interrupt after having stored 5, 9, or 17 characters in the silo instead of interrupting on each character.

A Receiver Enable bit (CSR Bit 0) is provided which, when cleared, prevents the DJ11 from depositing characters in the silo.

The program can set the DJ11 for half-duplex operation (all channels simultaneously) by asserting bit 1 (Half-Duplex Select) in the CSR. Half-duplex, for the DJ11, means that if a character is in the process of being transmitted on a given line, the receiver associated with that line is disabled.

The entire silo and all 16 UART's may be cleared by assertion of CSR bit 3 (MOS Clear). Since more than one instruction time is required to clear the LSI circuits, CSR bit 4 (Busy Clear) is provided as a flag. Bit 4 is asserted any time the MOS Clear is in process. No load operations to the DJ11 or reads, of other than bit 4 of the CSR, should be attempted while bit 4 is set. MOS Clear causes all transmit lines to assume a marking (logical 1) state.

It should be noted that 'clearing' the silo only clears the Data Present bit (bit 15) in the Receiver Buffer Register (RBUF) and does not affect the state of any RBUF bits. These RBUF bits may contain anything, and will be updated each time a new character is presented to the program.

The DJ11 hardware asserts CSR bit 13 (FIFO Full) anytime the receiver scanner finds a line with a character available, but cannot load the new character into the silo. If CSR bit 12 (Status Interrupt Enable) is also set, an interrupt request is generated. The assertion of FIFO Full does not necessarily mean data has been lost. On any given line, there will be one character time between the time the character is presented to the receiver scanner, and the time Overrun actually occurs. In the worst case (9600 Bauds, 7 bit characters) the program has approximately 700 μs to respond to the FIFO Full Interrupt and remove characters from the silo before any data is actually lost. The receiver scanner runs at about a 1 MHz rate, and so scans each UART many times during one character time.

Transmitter

The transmitter section of the DJ11 performs parallel-to-serial conversion of data supplied to it from the UNIBUS. The character length and stop code for any given line are the same as for the receiver on that line. The transmitter data rate, however, is jumper selectable in four-line groups, independent of the receiver data rate.

The transmitter for each line is fully double buffered. That is, the program has a full character time to respond to the Transmit Ready (bit 15) flag from any line, and still transmit data on that line at its maximum character rate.

The transmitter section of the DJ11 is operated by the program through four registers on the UNIBUS: The Control Status Register (CSR) previously mentioned, the Transmitter Control Register (TCR), the Transmitter Buffer Register (TBUF), and the Break Control Register (BCR).

To initiate transmission, the program sets CSR bit 8 (MASTER TRANS SCAN ENB). If it is desired to have the transmitter section give an interrupt when a character is requested, the program also sets CSR bit 14 (TRANS INT ENB). The Transmitter Control Register (TCR) is used to select an individual line for transmission. In order to set and clear bits in TCR, it is required that CSR bit 10 (BREAK REG SEL) be cleared (0). If the line-select bit in TCR associated with a particular line is set, and the transmit character buffer (TBMT) in the UART for that line is empty, the DJ11 transmitter scanner stops when it reaches the selected line. CSR bit 15 (TRANS RDY) will be set, and, if CSR bit 14 (TRANS INT ENB) is set, an interrupt request is generated. The BR level is the same as for the receiver. BR 5 is standard. When the transmitter scanner stops, the line number to which it is pointing will be contained in the Transmitter Buffer Register (TBUF) in bits 8-11. These bits are read only.

The program may then read the line number and furnish a new character to be transmitted on that line, by loading the character in TBUF, or the

program may clear the line select bit in TCR. Either action clears CSR bit 15 (TRANS RDY) and allows the transmitter scanner to continue.

It should be noted that the so-called 'transmitter scanner' is not really a scanner, but is, instead, a 16-level priority encoder. The practical effect of this is that when any line is serviced as described above, the next line requiring service will be found and the TRANS RDY bit (CSR bit 15) set in 1.3 μs or less, independent of the line number. Thus, the hardware allows the program to perform transmit service in a very efficient manner on all active lines on one entry to the transmit service routine. The transmit character buffers in the UART's are sampled every 400 ns. Line 15 has the highest priority, and line 0 the lowest. For mixed-speed configurations, the highest-speed line should be connected to DJ11 lines 15-12, the next highest to lines 11-8, etc.

The normal rest condition of the Transmitted Data lead for any line is Marking (1). A continuous Spacing (0) signal may be applied to a line by means of the Break Control Register (BCR). The program addresses the BCR by setting CSR bit 10 (BREAK REG SEL). The program may then cause a continuous Spacing condition on a particular line by setting the Break Bit in BCR for that line. The Spacing condition remains on the Transmitted Data lead as long as the Break Bit is set for that line. If characters are supplied to the transmitter for that line, however, it continues to appear to the program as if they are being sent normally. This provides the facility for sending precisely timed spacing signals, by asserting the Break Bit and using the Transmit Ready Interrupts as a timer.

It should be remembered in this context that each line in the DJ11 is double buffered internally. This means that when the transmitter section gives a TRANS RDY and an interrupt, it has just **started** sending the last character loaded into TBUF (not finished). When the transmitter is used as a timer for sending Breaks, the program should ensure that the characters sent, or at least the final one, are all ones (Marks), else the line may remain in a spacing condition longer than desired.

Line Interfaces

The Line-Distribution Panels supplied with the DJ11-AA and DJ11-AC are used to fan out the lines to the outside world.

The DJ11-AA is supplied with an electrical interface and connectors which meet the specifications of Electronic Industries Association Standard RS232C, and CCITT Recommendation V.24, for the Transmitted Data (Circuit BA, pin 2) and Received Data (Circuit BB, pin 3) leads.

The DJ11-AC is supplied with an active electrical interface which furnishes a nominal 20 mA at 20 V dc, for operation of local neutral Teletype terminals and other terminals operating on 20 mA neutral current loops.

The DJ11-AB is supplied without level conversion (TTL input-output levels) and without a Line Distribution Panel, for control of DIGITAL-supplied DC08 Telegraph Line Interface equipment.

The DJ11-AA and DJ11-AC Panels do not require that power be supplied to them, that is, they are completely passive. These panels can be mounted across a 19-in. rack or flat against a wall. Level conversion of the TTL signals is performed within the DJ11. The level-converted data are sent from the DJ11 to the Distribution Panel by two flat cables which terminate in Berg connectors. The Distribution Panel fans out the lines to Individual Cinch DB25P connectors (DJ11-AA) or four-wire screw terminal strips (DJ11-AC) for each line. The TTY Distribution Panel (DJ11-AC) contains several components of the TTY circuit.

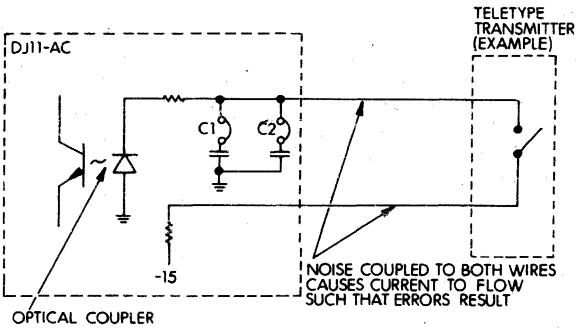
Several jumper selections are available on the Distribution Panels. In the EIA case, the Data Terminal Ready lead (Circuit CD, pin 20) and the Request To Send lead (Circuit CA, pin 4) normally are strapped to a positive or 'ON' voltage. This strapping can be removed individually (on a per-line basis). The DJ11-AA Distribution Panel also contains a Jumper that connects together the Protective Ground (Circuit AA) and Signal Ground (Circuit AB) leads from each channel. The jumper can be cut to separate the two grounds.

Two jumpers for each line exist on the DJ11-AC Panel (20-mA TTY). With these jumpers the receiver portion of the TTY circuit can be shifted from an active receiver (one that supplies the current source) to a passive one (where the remote equipment must supply the current). The active receiver is required for Teletypes and similar devices that provide a switch opening or closing for a binary one or zero. The disadvantage of this mode is that the signalling is single-ended and noise introduced on the line can cause errors. When wired as a passive receiver, the device has common-mode rejection, since any noise introduced on the wires appears on both wires and hence causes no net change in the current through the diode.

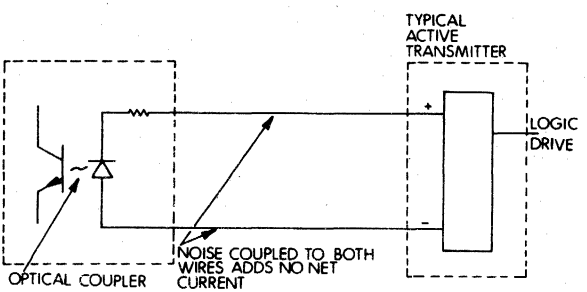
The DJ11-AC Panel also contains two other jumpers for each line. These are used to insert capacitors to filter out high frequency noise in the circuit. There are three speed ranges. The low-speed range is used for 300 Bauds and below; both capacitors are left in for this range. The filtering adds 10% distortion, maximum, to a 300-Baud signalling rate. The medium range is used for 2400 Bauds and below; capacitor C1 is removed, and the filtering causes 10% distortion, maximum, to a 2400-Baud signal. The high range is obtained when both capacitors are removed and should be used above 2400 Bauds. For the higher speed ranges it is preferable that the remote device be the current source so that the DJ11-AC receiver can be strapped as a passive receiver with common-mode rejection.

Maintenance Provisions

The DJ11 has a maintenance bit (CSR bit 2) which will, when set, loop back all 16 lines internally. Also, if split speed was selected on any or all of the groups, the transmitter speed will be forced to that of the receiver so that loop-back can occur.



TTY RECEIVER WIRED AS ACTIVE



TTY RECEIVER WIRED AS PASSIVE

PROGRAMMING

General

The Interface between a program running in the PDP-11 processor and the DJ11 is via five device registers, two of which share a common address on the UNIBUS.

These registers are:

Control Status Register (CSR), address 76XXX0
Receiver Buffer Register (RBUF), address 76XXX2
Transmitter Control Register (TCR), address 76XXX4
Break Control Register (BCR), address 76XXX4
Transmitter Buffer Register (TBUF), address 76XXX6

The functions of the bits provided in each register are defined below. Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction that references these addresses, with the exceptions noted. Selection of BCR or TCR (BREAK REG SEL) is accomplished by setting or clearing CSR bit 10. If bit 10 is

cleared (0) references to address 76XXX4 will reference TCR. If bit 10 is set (1), references to address 76XXX4 will reference BCR.

Interrupts

The DJ11 uses two interrupt vectors; vector address XX0 for the interrupt caused by Receiver Done (CSR bit 7) and FIFO Full (CSR bit 13), and vector address XX4 for Transmit Ready (CSR bit 15). Both interrupts operate independently, except that the receiver takes priority on simultaneous interrupt requests (is closer to the processor on the UNIBUS). Since the interrupt through vector address XX0 can come from two sources (Receiver Done and FIFO Full), it is necessary for the program to check both bits 15 and 13 each time the service routine for this interrupt is entered. The program must clear the bit which caused the interrupt request when exiting the service routine, else the occurrence of another interrupt-causing condition, while the first is being serviced, may fail to give an interrupt.

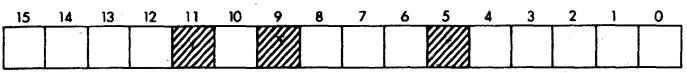
Address and Vector Assignment

The address assigned to the DJ11 is in the floating address space reserved for PDP-11 peripherals. The DJ11's for a system are assigned contiguous addresses in the range from $760\,010_8$ to $764\,000_8$. Each DJ11 requires 10_8 locations. Each unit uses two interrupt vectors, one for Receiver Done and FIFO Full (address XX0), and one for Transmit Ready (address XX4).

Register Definition

Bits marked 'Not Used' and 'Write Only' are always read as zero. Attempting to write into 'Not Used' or 'Read Only' bits has no effect on those bits. INIT' refers to the initialize signal generated by the processor (e.g., upon execution of a RESET instruction). 'Transmit' and 'Receive' are with respect to the DJ11.

Control Status Register (CSR) 76XXX0



BIT DESCRIPTION AND OPERATION

15 Transmitter Ready. Read only. This bit is set whenever the transmitter scanner finds that the transmit-character buffer in the UART for line n (TBMTn) is able to accept a character for transmission and the line-select bit in the Transmitter Control Register (see below) for that line (TCRn) is set. The logical condition is then CSR15←CSR8* TMBTn* TCRn (*implies 'AND'). This bit is cleared by the hardware within 1μs after a character is loaded into the Transmitter Buffer Register (see below), negating TBMTn, or when TCRn is cleared. The transmitter scanner stops when Transmitter Ready is set, and resumes when it is cleared. If another line needs transmit service at the time bit 15 is cleared, bit 15 will be set

again within 1.4 μs of the completion of the bus cycle that loads TBUF or clears TCRn. This bit is cleared by INIT or by the actions described above.

14 Transmitter Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated whenever CSR bit 15 is set. This bit is cleared by INIT or by the program.

13 FIFO Full. Read only. This bit is set if the DJ11 receiver hardware attempts to load a character into the FIFO buffer and finds the buffer full. The receiver scanner continues to scan. This bit is cleared when the Receiver Buffer Register (see below) is read from, or by INIT.

12 FIFO Buffer Status Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated whenever CSR bit 13 is set. This bit is cleared by INIT or by the program. The program servicing this interrupt should clear bit 12 upon entering the service routine, and should reset it upon exit, to make sure the hardware picks up all transitions of bit 13.

10 Break Register Select. Read/Write. This bit, when set, causes processor references to address 76XXX4, to access the Break Control Register (see below). When clear, this bit causes processor references to address 76XXX4 to access the Transmitter Control Register (see below). This bit is cleared by INIT or by the program.

8 Master Transmit Scanner Enable. Read/Write. This bit, when set, enables the transmitter hardware to scan the UART's for lines requiring transmit service. When clear, this bit prevents CSR bit 15 from being set. This bit is cleared by INIT or by the program.

7 Receiver Done. Read Only. This bit is set when a received character word appears in the Receiver Buffer Register (RBUF, see below). If CSR bit 6 is also set, an interrupt request is generated. This bit is cleared by an instruction which references RBUF. However, if another received character word is in the silo, this bit is reasserted and the new data appears in RBUF within 1.4 μs. This bit is cleared by INIT or by the actions described above.

6 Receiver Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time CSR bit 7 is set. This bit is cleared by INIT or by the program.

4 Busy Clear. Read only. This bit is set by the hardware whenever the MOS Clear process, initiated by CSR bit 3, is in progress. It is a flag to the program indicating that other bits in CSR and other registers of the DJ11 should not be accessed. This bit is set, then cleared, by the setting of CSR bit 3.

3 MOS Clear. Write only. This bit, when set, causes a 2μs clear pulse to be issued to the silo and all 16 UART's. During the clear pulse,

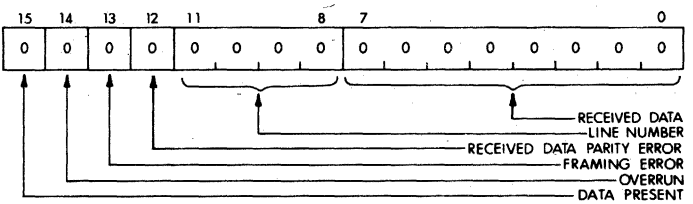
CSR bit 4 is also set. This bit is set by the program and cleared by the DJ11 hardware.

2 Maintenance Mode. Read/Write. This bit, when set, causes all the Transmitted Data leads to be connected to their respective Received Data leads at the TTL outputs. The Transmitter data rate of each four line group is also forced to that of the receivers for that group. This bit is cleared by INIT or by the program.

1 Half-Duplex Select. Read/Write. This bit, when set, disables the receiver section of any line during the time the transmitter section of that line is active. This bit applies to all 16 lines. It is cleared by INIT or by the program.

0 Receiver Enable. Read/Write. This bit, when set, enables the receiver scanner to operate and enables received character words to be loaded into the silo. It is cleared by INIT or by the program.

Receiver Buffer Register (RBUF), 76XXX2



BIT DESCRIPTION AND OPERATION

15 Data Present. Read only. This bit, when set, indicates the presence of a received character and its associated line number and status bits in RBUF. This bit is cleared by the hardware when data is read from RBUF, but is set again within 1.4μs if more data is present in the silo. It is cleared by INIT or by setting CSR bit 3.

14 Overrun. Read only. This bit is set if data from the line specified in bits 11-8 of RBUF has been lost. This may occur if the silo fills up. The character in this received character word is the first good character after the data loss (rather than the last good character before the data loss). This bit is valid only for this character. All bits in RBUF are updated as each new received character word appears in RBUF.

13 Framing Error. Read only. This bit is set if the UART, at the time it samples the Received Data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, a 'Break' signal, or excessive distortion of the Received Data character.

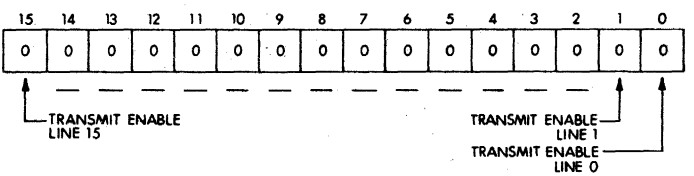
12 Received Data Parity Error. Read only. This bit is set by the UART

if the parity of the received data character does not agree with the parity specified for this group of lines (odd or even). This bit is always zero if the 'no parity check' option is specified. Bits 14, 13, and 12 are updated for each new character.

11-8 Line Number. Read only. These bits are the binary number of the line from which the character in bits 7-0 of RBUF was received.

7-0 Received Data. Read only. These bits contain the complete character assembled by the UART. If the character length specified for this group of four lines is less than 8 bits, the character appears right justified (low-order bit in bit 0). The unused high-order bits will contain 0's.

Transmitter Control Register (TCR) 76XXX4

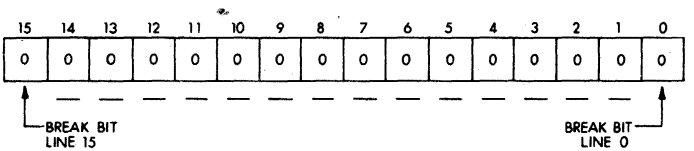


BIT DESCRIPTION AND OPERATION

15-0 Transmit Enable. Read/Write. Each bit in TCR enables the DJ11 transmitter scanner to flag that a character is required for transmission on one line. If the Transmit Enable bit in TCR is set for a particular line, CSR bit 8 is set, and the transmitted data buffer in the UART (TMBT) for that line is empty, then the scanner stops, CSR bit 15 is set, and, if CSR bit 14 is set, an interrupt request is generated. The line number at which the transmitter scanner is stopped appears in bits 11-8 of the Transmitter Buffer Register (TBUF, see below). The scanner restarts when TBUF is written into or when the TCR bit for the line whose number appears in bits 11-8 of TBUF is cleared. The bits in TCR are cleared by INIT or by the program.

Note that TCR may be accessed from the UNIBUS only if CSR bit 10 is cleared.

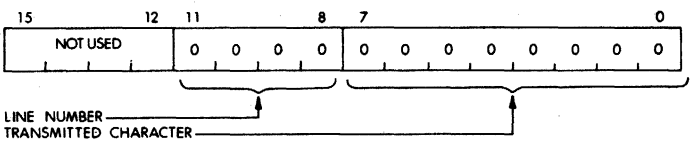
Break Control Register (BCR) 76XXX4



BIT DESCRIPTION AND OPERATION

15-0 Break Bit. Read/Write. Each bit in BCR controls the state of one Transmitted Data line. If the Break Bit in BCR is set for a particular line, that line is clamped in a Spacing (logical 0) state. This condition remains until the bit is cleared. The transmitter for that line appears to the program to function normally, however. This register may be accessed from the UNIBUS only if CSR bit 10 is set. BCR may be cleared by INIT or by the program.

Transmitter Buffer Register (TBUF) 76XXX6



BIT DESCRIPTION AND OPERATION

11-8 Line Number. Read only. If CSR bit 15 and the bit in TCR associated with the indicated line are set, these bits contain the four-bit number of the line requiring a character for transmission. Cleared by INIT. Note that bits 11-8 are valid only if CSR bit 15 is set.

7-0 Transmitted Character. Write only. The data character to be transmitted on the line whose number is contained in bits 11-8 of TBUF is loaded into these bits. If the data character contains fewer than 8 bits, the character must be right justified when loaded into TBUF. The bits of the data character are presented to the serial line low-order bit (bit 0) first. A bit set to a one in TBUF causes a marking condition to appear on the Transmitted-Data lead for the line whose number is in bits 11-8 of TBUF for one bit time. These bits are cleared by INIT. Note that bits 7-0 should only be loaded when CSR bit 15 is set. Loading TBUF with CSR bit 15 cleared results in the transmission of the character on line 0.

SPECIFICATIONS

Function:	The DJ11 provides an interface between the PDP-11 UNIBUS and 16 asynchronous bit serial communications channels.
Connectability:	A maximum of 16 DJ11's may be connected to a single PDP-11.
Operating Mode:	Half or Full duplex, under program control.
Data Format:	Asynchronous, serial by bit. One start and 1, 1½ (5-level codes only), or 2 stop bits supplied by the hardware. The DJ11 will accommodate characters of 5, 6, 7, or 8 bits, with or without even or odd parity.

The data format is the same for transmitted and received data on any line. The data format is switch selectable in four-line groups.

A one (1) presented by the program to any bit in the Transmitter Buffer Register causes a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program causes a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data-bit sampling interval is presented to the program as a one (1) in the Receiver Buffer Register, and a Spacing condition is presented as a zero (0).

Order of Bit Transmission and Reception: Low-order bit first

Data Rate: The DJ11 is supplied with 11 standard data rates: 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. The data rate is jumper selectable in four-line groups. The data rate for the receivers in a group may be different from that of the transmitters in that group.

Signalling Performance: DJ11-AA: 15.2 m (50 ft) at up to 9600 Bauds with BC05D cable, or equivalent.

DJ11 Distribution Panel-to-Terminal Distances: DJ11-AB: 3.7 m (12 ft) with supplied cable.
DJ11-AC: 5.5 m (18 ft) with DIGITAL BC04R-18 cable. With cable made with shielded twisted pairs, such as Belden no. 8777 or equivalent, the following rate/distance table may be used as a guide. This chart is for informational purposes only, and is not to be construed as a warranty by Digital Equipment Corp. of error-free operation of DJ11 at these speeds and distances under all circumstances.

150 m at 9600 Bauds
150 m at 4800 Bauds
450 m at 2400 Bauds
450 m at 1800 Bauds
450 m at 1200 Bauds
450 m at 600 Bauds
600 m at 300 Bauds and below

Distortion: The DJ11 receiver operates properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received-data bits, and up to

± 4.5% long-term speed distortion, provided the data format contains a least 1½ stop units. If the data format contains only one stop unit, the speed tolerance is ± 4%. The DJ11 transmitter operates with less than 3% bit-to-bit or long-term distortion.

Bus Loading: One DJ11 presents one unit load to the PDP-11 UNIBUS.

Physical Layout: The DJ11 consists of a single prewired PDP-11 system unit, suitable for mounting in a PDP-11/40, PDP-11/45, or equivalent cabinet, and all logic modules and cables necessary to implement a 16-line multiplexer. The DJ11-AA and DJ11-AC are supplied with an externally mounted, 14-cm high (5½ in.) Line Distribution Panel with connectors appropriate to type of channel to be connected. Cables to connect the Distribution Panel to data sets are not supplied but are available separately (see below).

The DJ11-AB is supplied with cables and connector cards that plug into the DC08 Telegraph Line Interface Option or into a standard DM11 Line Distribution Panel.

Note that the DJ11 cannot be mounted in a PDP-11/15 or PDP-11/20 processor box, or in a BA11ES extender box. See below for recommended mounting cabinet.

Electrical Interface: DJ11-AA: Provides a voltage-level interface for 16 lines whose signal levels and connector pinnings conform to Electronic Industries Association Standard RS232C and CCITT Recommendation V. 24. The leads supported by the DJ11-AA are:

Protective Ground, Circuit AA (CCITT 101) pin 1.

Transmitted Data, Circuit BA (CCITT 103) pin 2.

Received Data, Circuit BB (CCITT 104) pin 3.

Signal Ground, Circuit AB (CCITT 102) pin 7.

Signal Ground and Protective Ground are connected together by a removable jumper on the DJ11-AA Distribution Panel:

In addition, the Data Terminal Ready lead, Circuit CD (CCIT 108.2) pin 20, and the Request to Send lead, Circuit CA (CCIT 105) pin 4, are clamped ON (logical 1). This condition may be removed on a per-line basis by removal of jumpers on the DJ11-AA Distribution Panel. If the jumpers are removed, how-

ever, these leads are left floating (0 V dc). These circuits are terminated in 16 Cinch DB25P connectors mounted on a 14-cm-high by 48.3-cm-wide (5½ x 19 in.) Distribution Panel supplied with the DJ11-AA.

Cables with the proper connectors for connecting the Distribution Panel to modems or local terminals with EIA interfaces are available from DIGITAL as No. BC05D—25 (7.6m, 25 ft).

DJ11-AB: Provides standard Transistor-Transistor-Logic (TTL) Levels for 16 receive and transmit data leads on two cables 3m (10 ft) long, terminated in M971 cards. The pinning of these cards is such that they may be plugged into the DIGITAL-supplied DC08 Telegraph-Line Interface Option, or into the Distribution Panel supplied with the DM11 16-line Asynchronous Serial Line Multiplexer.

DJ11-AC: Provides 20-mA neutral active or passive (jumper option) current-loop circuits for 16 transmit and receive data leads. These circuits are terminated in 16 four-screw-terminal barrier strips mounted on a 14 cm-by-48.3 cm (5½ x 19 in.) Distribution Panel that can be mounted on the back door of a standard 48.3-cm (19 in.) rack, or mounted on any flat surface no farther than 3 m (10 ft) from the DJ11 logic.

Power Requirements:

DJ11-AA:	4.7 A at + 5 V dc 0.25 A at — 15 V dc 0.25 A at + 15 V dc
DJ11-AB:	4.7 A at + 5 V dc 0 A at + 15 V dc 0.25 A at — 15 V dc
DJ11-AC:	5.3 A at + 5 V dc 0 A at + 15 V dc 1.0 A at — 15 V dc

Heat Dissipation: 35 kg-cal/hr maximum

Environmental: The DJ11 operates at an ambient temperature of 5 to 50° C with relatively humidity of 10 to 95%, non-condensing.

Models

DJ11-AA: 16-line Asynchronous Serial Line Multiplexer, Full- or Half-Duplex operation. Electrical Interface meets Standards EIA RS232C and CCITT V.24. Supports Transmitted and Received-Supports Transmitted and Received-Data leads only.

Request To Send and Data Terminal Ready leads clamped ON. Speed and character format strap selectable in four-line groups. Provides 5, 6, 7, or 8 data bits: 1, 1½, or 2 stop bits; even, odd or no parity. Provides standard data rates of 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. Split-speed operation. Supplied with externally mounted Distribution Panel, but without modem cables. See Related Options for recommended cable.

DJ11-AB: As DJ11-AA above, except electrical interface is TTL levels (0,+5V) for Transmitted and Received Data leads only. Supplied without external Distribution Panel, but with cables and cards for connection to DC08 Telegraph Line Interface Options, or to the DIGITAL DM11-AA/AC Line Distribution Panel.

DJ11-AC: As DJ11-AA above, except electrical interface is 20-mA neutral active or passive current loop, for operation of local devices with 20-mA current-loop interfaces (Teletypes, LA30-CA and -CD, VT05-A and -B etc). Externally mounted Distribution Panel has screw-terminal strips to connect Transmitted and Received Data Leads from devices.

Related Equipment

BC05-D-25 Cable — Modem Cable, 7.6 m (25 ft), 25-conductor cable terminated in Cinch DB25S socket at one end, and DB25P plug at the other end. For connection of one line from DJ11-AA Distribution Panel to modem, data set, or Null Modem listed below.

H312A — Null Modem. Required for local connection of terminals with EIA interfaces, such as LA30-EA or -EC, Hazeltine 2000, etc. to BC05D cable from DJ11 Distribution Panel.

BC04R-XX Cable — Four spade lugs to male Mate-N-Lok cable. For local connection of DIGITAL RT01 etc to DJ11-AC Distribution Panel. This cable is supplied in standard lengths of 3.7 m (12 ft, BC04R-12) and 5.5 m (18 ft, BC04R-18).

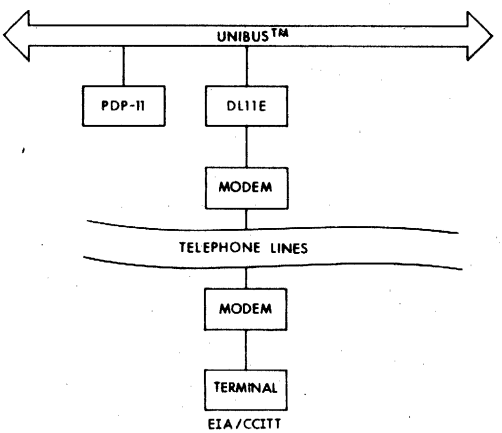
H960-DA — Cabinet with single PDP-11/40 or PDP-11/45 Extension Mounting Box. Provides mounting space for nine system units (9 DJ11's). Includes power supply for 115-V, 60-Hz power.

H960-DB — As above, except for 230-V, 50-Hz power.

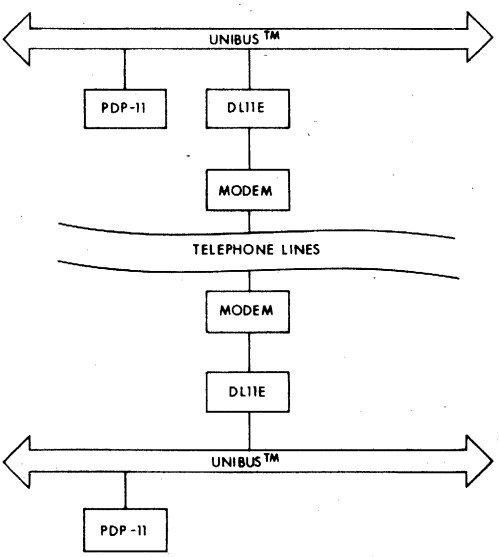
H960-EA — As H960-DA, except two boxes and two power supplies, providing space for 18 system units. For 115-V, 60-Hz power.

H960-EB — As H960-DC above, except for 230-V, 50-Hz power.

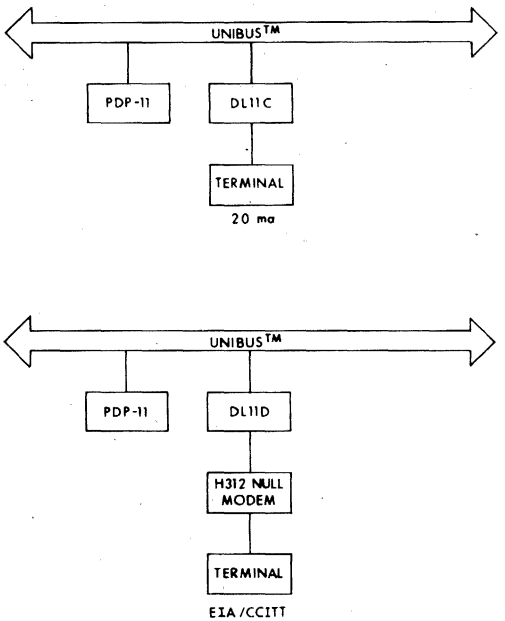
SINGLE ASYNCHRONOUS SERIAL LINE INTERFACES, DL11



Interfacing a Remote Terminal



Interfacing a Remote PDP-11



Interfacing a Local Terminal

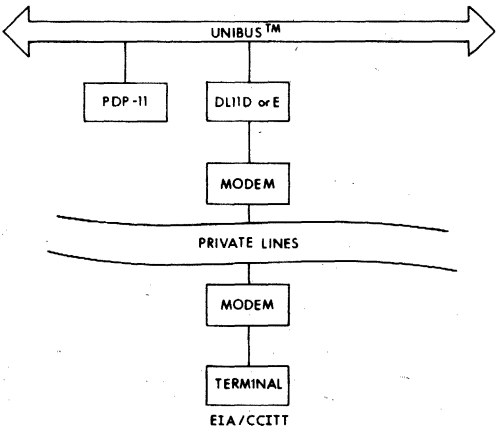
DESCRIPTION

The DL11 series of asynchronous single line interfaces handle full or half duplex communication between a wide variety of serial communication channels and a PDP-11 computer.

With a DL11 interface, a PDP-11 computer can communicate with a local terminal such as a console teleprinter, with a remote terminal via data sets and private line or public switched telephone facilities, or with another local or remote PDP-11 computer.

DL11 systems provide wide flexibility. The user can specify data rate from a selection of 13 standard rates between 40 and 9600 Baud, or he can order a non-standard rate device. With most of the standard rates, the interface can offer split-speed operation for faster, more efficient handling of computer output.

For additional flexibility, character size is strap selectable for 5, 6, 7, or 8-level codes. Also strap selectable are parity checking (even, odd, or none) and stop code length 1, 1.5, or 2 bits).



Remote Communication via Private Lines

There are five DL11 models.

Model DL11-A replaces and is compatible with DIGITAL's KL11 interface, handling 20 mA neutral current loop devices (such as console teleprinters) which use 8-level code and two stop bits.

The DL11-C handles the same current levels but provides the flexibility of a wide choice of speeds and stop bit configurations. This model is recommended for direct interfacing of DIGITAL-supplied teleprinters, the VT05 alphanumeric display, and the LA30-C DECwriter—a DIGITAL-designed electronic keyboard printer.

Model DL11-B meets the interface specifications of Electronic Industries Association Standard RS232C and CCITT Recommendation V.24 and handles either local or remote (data only) communication for 8-level code devices. With local devices, this model requires a null modem; in private line communication, modems are required.

Model DL11-D meets the specifications of and is applied in the same manner as Model DL11-B. However, like the C model, it gives the user a choice of operating speeds and stop bit configurations, so that it is easily adaptable to a wide range of terminals. With a null modem, this model may be used for local interfacing of a terminal or another PDP-11.

Model DL11-E meets the EIA and CCITT interface specifications cited for Models B and D. This interface provides the user with the full range of data rates as well as with complete dataset control for remote communication with either a terminal or another PDP-11 computer.

Using the PDP-11's versatile UNIBUS as a multiplexer, a PDP-11 can handle multiple DL11 interfaces. Assigned addressing space allows a single system to support up to 16 DL11-A and/or B models and up to 31 DL11-C, D, or E models. Each DL11 module represents one unit load to the UNIBUS and plugs into a standard small peripheral controller slot in a PDP-11 system unit.

With its exceptional versatility, the DL11 is ideally suited for such applications as numerical control and data acquisition and reduction, especially in such fields as biomedicine and physics where input and processing often require multiple asynchronous lines.

OPERATION

General

The DL11 is an interface between a single Asynchronous Serial Communication Channel and the PDP-11. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with a double character buffered MOS/LSI circuit called a UART (for Universal Asynchronous Receiver-Transmitter). This 40-pin dual-in-line package includes all of the circuitry necessary to double buffer characters in and out, serialize-deserialize data, provide selection of character length and stop code configuration, and present status information about the unit and each character.

Receiver

The receiver section performs serial to parallel conversion of 5, 6, 7 or 8-level codes. The character length is selectable by split-lug jumpers on the circuit card, and is specified by the customer at the time of the order. Each character appears right justified in the Receiver Data Buffer Register (RBUF), stripped of start, stop, and parity bits.

The data rate may lie anywhere in the range between 40 baud and 10,000 baud, and in many cases need not necessarily be the same for the receiver as for the transmitter. (See section on DATA RATES). The receiver samples the line at 16 times the data rate.

A complete character is formed in the UART and is transferred to the Receiver Data Buffer Register (RBUF) at the time the center of the first stop bit is sampled. At that time, the Receiver Done Bit (Bit 7) is set in the Receiver Status Register (RCSR). If the Receiver Interrupt Enable Bit (Bit 6) is also set in RCSR, an interrupt request is generated. The BR level is set by jumper plug. BR4 is standard.

The program then reads the RBUF. The character appears right justified in bits 7-0 of RBUF, stripped of start, stop, and parity (if odd or even is selected) bits. Unused high order bits (6 and 7 in the case of a 6-level code) are zero-filled. Bits 8-11 are always zero and bits 12-15 contain status information about the character supplied by the UART*. (See section on PROGRAMMING.)

* All references to the character status and error bits (12-15) apply to the DL11-C, D, and E models only. The DL11-A and B are KL11 compatible, and therefore have no such status bits.

MODEL	ELECTRICAL INTERFACE	LEVEL CODE	STOP BITS	PARITY CHECKING	BAUD RATE GROUPS*	APPLICATIONS
DL11-A	20 ma neutral current	8	2	None	1, 3	Models LT33 & LT35 teletypewriters with or without paper tape.
DL11-B	EIA/CCITT	8	2	None	1, 3	Local (needs null modem) Remote (private wire) via modems.
DL11-C	20 ma neutral current	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Used as A, but choice of code etc. VT05, LA30-C, . . .
DL11-D	EIA/CCITT	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Used as B, but choice of code etc. Can be used for local interfacing of a PDP-11 with a null modem.
DL11-E	EIA/CCITT	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Bell 103, 202, 113 modems

* See data rate table later in this section.

Note that the program has a full character time to remove the completed character from RBUF before the next character is put there by the UART. Should the program fail to remove a character before the next is available, the old one(s) will be lost, and the Overrun Bit and Error Bit (bits 14 and 15) are set in RBUF.

The customer may specify, at the time of ordering, that the DL11 will check received data characters for even parity (an even number of data bits are ones), odd parity, or no parity check. If even or odd parity is selected, the DL11 will compute the parity of the incoming character and set bits 12 and 15 in RBUF if an error is found. (Bit 15 is the logical OR of bits 12, 13 and 14.) Note that if odd or even parity is selected, the total character length is the sum of the start bit, plus the number of data bits selected, **plus** the **parity bit,** plus the number of stop bits selected.

If, at the time the center of the first stop bit should appear on the received data line, the line is found to be in a spacing condition, the Framing Error Bit (Bit 13) and Error Bit (Bit 15) are set in RBUF. Such a condition may occur, for instance, if the data line goes open, or if the terminal to which the DL11 is connected transmits a Break signal. Should this occur, RBUF will contain a character all of whose bits will be zero. Succeeding all-zero or Break characters, however, will not be assembled by the UART and presented to the program. The received data line must return to a marking condition before character assembly will be resumed.

Transmitter

The transmitter section performs parallel to serial conversion of data supplied to it from the UNIBUS. The character length and stop code (number of units of mark at the end of each character) are the same as for the receiver section. The transmitter section is also fully double buffered. Any time the Transmitter Ready Bit (bit 7) is set in the Transmitter Status Register (XCSR), the program may load the low-order eight bits of the Transmitted Data Buffer Register (XBUF) with a right justified data character. The Transmitter Ready Bit will be set any time the XBUF is available, whether or not a character is currently being transmitted. This is a natural result of the double buffering and means that if a character is not currently being transmitted and XBUF is empty, the program may provide two characters in succession (within less than one character time) to the transmitter.

As the first character is loaded, it is immediately transferred to the serializer register internal to the UART, and the Transmitter Ready Bit (bit 7) in XCSR is set again. If the Transmitter Interrupt Enable Bit (bit 6) is set in XCSR, an interrupt request will be generated any time the Transmitter Ready Bit (bit 7) is set. The BR level for the transmitter is the same as for the receiver.

The transmitter supplies the start bit, odd, even, or no parity bit, and the proper number of stop bits as specified by the customer at the time of order.** The code configuration (number of data bits, odd, even, or

no parity, and number of stop bits) is the same for the transmitter as for the receiver section.

The normal rest condition of the transmitted data lead is marking. A continuous spacing signal may be applied to this lead by setting bit 0 or XCSR (the "BREAK" bit) to a one.** The Transmitted Data lead will remain in a spacing condition as long as this bit is asserted. If characters are supplied to the transmitter, it will, however, continue to appear to the program as if they were being sent normally. This provides the facility for sending precisely timed spacing signals, by asserting the "BREAK" bit and using the transmitter interrupts as a timer.

** Note that references to parity generation and "BREAK" bits are not applicable to the DL11-A and B, since these two are functionally and program compatible with the KL11.

Paper Tape Reader Control

The DL11-A and DL11-C have a 20 mA current loop electrical interface and are equipped to control the paper tape Reader Run Relay with which some DIGITAL-supplied teleprinters are equipped. If bit 0 of RCSR is set to a one, the lead controlling the Reader Run Relay is asserted, and a character will be read from paper tape. This bit is reset upon detection of a valid start bit by the UART receiver. The DL11-A is supplied with a 2¼ ft. cable (DIGITAL part #7008360) terminated in a female MATE-N-LOC connector which connects to the teleprinter supplied with a PDP-11, or to the cable supplied with the DIGITAL VT05 terminal, or DIGITAL LA30-C DECwriter.

Dataset Interface

The DL11-B and DL11-D are supplied with an electrical interface and connector whose signal levels and connector pinning conform to Electronic Industries Association Specification RS232C, and to CCITT Recommendation V.24. Their cables are terminated in a Cinch DB25P plug with protective hood. The DL11-B and DL11-D connect to the Protective Ground (EIA circuit AA, connector pin 1), Signal Ground (Circuit AB, pin 7), Transmitted Data (Circuit BA, pin 2), Received Data (Circuit BB, pin 3), Request to Send (Circuit CA, pin 4), and Data Terminal Ready (Circuit CD, pin 20) leads. The Data Terminal Ready lead (Circuit CD, pin 20) and Request to Send lead (Circuit CA, pin 4) are held asserted (ON, logical 1). It is therefore possible to connect the DL11-B and DL11-D to datasets such as the Bell 103A2, which will automatically answer incoming calls. It is not possible, however, to terminate the call, determine the presence of Data Carrier (Circuit CF), detect a Ring signal (Circuit CE), or operate the Secondary Transmitted and Received Data leads (Circuit SBA and SBB) with the DL11-B and DL11-D, under program control. These functions are provided by the DL11-E.

Dataset Control

The DL11-E is supplied with an electrical and physical interface as described above for the DL11-B and D, except as noted. However, the DL11-E is equipped for full dataset control, and supports the following dataset leads:

Signal Name	EIA Circuit Designation	Connector Pin No.
Protective Ground	AA	1
Transmitted Data	BA	2
Received Data	BB	3
Request to Send	CA	4
Clear to Send	CB	5
Signal Ground	AB	7
Received Line Signal Detector (Carrier)	CF	8
*Secondary Transmitted Data	SBA	11
*Secondary Received Data	SBB	12
Data Terminal Ready	CD	20
Ring Indicator	CE	22

* The pinning convention for Secondary Transmitted and Secondary Received Data leads does NOT conform to the cited EIA and CCITT specifications, but rather to the Bell 202C, D Dataset Interface pinning. In order to make the connector pinning conform to the EIA/CCITT specifications for these two leads, it is necessary to move the wire connected to pin 11 in the Cinch DB25P connector to pin 14, and the wire connected to pin 12 to pin 16.

These leads are sensed (for signals from the dataset) and set/reset (for signals to the dataset) by the program via bits in RCSR. The operation and meaning of these bits is explained in the section on "Programming."

Note that it is not possible to convert one DL11 model to another in the field.

Data Rates

The DL11 is available with a wide range of standard data rates. The customer must specify on his order one of four groups of data rates for both the transmitter and receiver, in bits per second. The following table lists the standard rates available, and whether or not it is possible to operate the transmitter at a different speed from the receiver (split speed).

Speed Group	Speeds (Bits Per Sec)		Split Speed	Applicable Terminals
	Transmit	Receive		
1	110	110	No	Teletype Models 33, 35
2*	134.5	134.5	No	IBM 2740, 2741, Datel, etc.
3	50 75 150 300 600 1200 1800 2400	50 75 150 300 600 1200 1800 2400	Yes	DIGITAL LA30, VT05, M37 TTY Most CRT Terminals

4*	200 300 600 1200 2400 4800 7200 9600	200 300 600 1200 2400 4800 7200 9600	Yes	DIGITAL LA30-C, VT05, GE Terminet 300, Most CRT Terminals

* Not available on DL11-A and DL11-B.

It is possible to field change speeds within groups 3 and 4 to other speeds within the same group, but it is not possible to field change from one group to another group. Where the data rate specified by the customer may be either group 3 or 4 (e.g. 300 baud), the unit will be supplied with group 3 speeds.

PROGRAMMING

General

The interface between a program running in the PDP-11 processor and the DL11 is via four device registers. They are the 1) Receiver Status Register (RCSR); 2) Receiver Data Buffer Register (RBUF); 3) Transmitter Status Register (XCSR); and 4) Transmitter Data Buffer Register (XBUF). The functions of the bits provided in each register are described below. Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction which references these addresses, with the exceptions noted.

Interrupts

The DL11 has two channels of interrupts: one for the receiver section (vector = XX0) and one for the transmitter section (vector = XX4). These two circuits operate independently, except that receiver takes priority on simultaneous interrupt requests (is closer to the processor on the bus).

However, it is very important to note that in the DL11-E (dataset operation), the receiver section handles a multiple source interrupt: RCVR DONE and DSET INT. Furthermore, DSET INT is set by several conditions (RING, CARRIER, etc.). If while servicing an interrupt for one condition, a second interrupt condition occurs, a unique second interrupt (and all subsequent ones as well) may not occur. To prevent this: 1) all possible interrupt conditions should be checked after servicing one particular condition, or 2) both interrupt enables (bits 5 and 6) should be cleared upon entry to the service routine for vector XX0, and set again at the end of service.

Address and Vector Assignments

The DL11-A and DL11-B follow the same address and vector assignments as the KL11:

	Address	Vector	Priority
Console	777 560 777 562 777 564 777 566	60/64	BR4
Additional Units	776 XX0 776 XX2 776 XX4 776 XX6	Floating	BR4

Since each DL11 unit has four registers, each requires four addresses. Address space assignment for the DL11-A and B is the same as that for the KL11; that is, unit 0 occupies addresses 777 560-777 566, and units 1-15 occupy from 776 500 through 776 676. For the DL11-C, D, and E, unit 0 will have address 775 610, unit 1, 775 620, etc., up to unit 30 at 776 170.

The four registers and their addresses are listed for DL11 unit 0, where XXX is 756 for DL11-A and B, and 561 for DL11-C, D, and E.

1. Receiver Status Register (RCSR) 77XXX0
2. Receiver Data Buffer Register (RBUF) 77XXX2
3. Transmitter Status Register (XCSR) 77XXX4
4. Transmitter Data Buffer Register (XBUF) 77XXX6

The interrupt vector addresses for the DL11-A and DL11-B follow the same scheme as for the KL11. That is, if one is used for the console teletype, it gets vector address 60 and 64. The next units occupy addresses beginning after all DC11's (if any) on the system are assigned, beginning at address 300. Any DP11, DM11, DN11, DM11-BB, DR11-A, DR11-C, and DT11's are then assigned. After all of the preceding are assigned, the DL11-C's, DL11-D's and DL11-E's are then assigned.

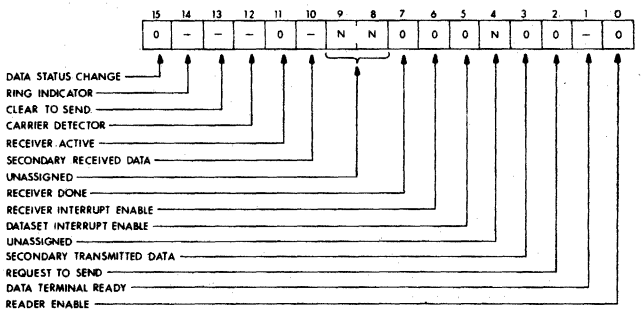
Register Definition

The following chart presents the bit assignments within each register. Bits marked "Unused" and "Write Only" are always read as zero. Attempting to write into "Unused" or "Read Only" bits has no effect on those bits. "INIT" refers to the initialize signal generated by the processor (e.g. upon execution of a RESET instruction.) "Transmit" and "Receive" are with respect to the DL11. All bits in the accompanying diagrams are shown in the state they assume on POWER CLEAR or INIT. A "dash" indicates that the bit is set by the terminal or dataset or the hardware and is not cleared by INIT.

BIT DESCRIPTION AND OPERATION

15* Dataset Status Change. Read only. This bit is set (1) by any change in the state of bits 10 (Secondary Receive Data), 12 (Carrier Det.), and 13 (Clear to Send) in RCSR, and by an off to on (0 to 1) change in the state of bit 14 (Ring Ind.) in RCSR. It is cleared (0) by INIT

Receiver Status Register (RCSR) 77XXX0



and by reading from RCSR. If bit 5 (Dataset Int. Enable) is set, the setting of bit 15 will cause an interrupt request to be generated.

14* Ring Indicator. Read only. The state of this bit follows the state of the Ring Indicator lead (Circuit CE, pin 22) from the dataset. It is set when the signal on Circuit CE is high, and cleared when that signal is low. A transition of this bit from 0 to 1 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

13* Clear to Send. Read only. The state of this bit follows the state of the Clear to Send lead (Circuit CB, pin 5) from the dataset. It is set when the signal on Circuit CB is high, and cleared when that signal is low. Any transition of bit 13 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

12* Carrier Detector. Read only. The state of this bit follows the state of the Received Line Signal Detector (Carrier) lead (Circuit CF, pin 8) from the dataset. It is set when the signal on Circuit CF is high, and cleared when that signal is low. Any transition of bit 12 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

11 Receiver Active. Read only. This bit is set when the receiver section of the UART detects a valid start bit on the Received Data lead. In the case of the DL11B, D, and E, this lead will be Circuit BB, pin 3 from the dataset. It is cleared when bit 7 in RCSR (Receiver Done) is set, and by INIT.

* Note that bits 15-12 in RBUF are not enabled in the DL11-A and DL11-B, and will appear as zero in these models when read by the program. This is to provide program compatibility with the DIGITAL KL11.
Note that all signals from the dataset will appear negated (low) to the program if the dataset is disconnected or loses power. This affects bits 14, 13, 12, and 10, all of which will appear as cleared under such conditions.

10 Secondary Received Data. Read only. The state of this bit follows the state of the Secondary Receive Data lead (Circuit SBB, pin 12) from a Bell 202 dataset. It is set when the signal on circuit SBB is high (spacing) and cleared when that signal is low (marking). Any transition of bit 10 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.

7 Receiver Done. Read only. This bit is set when the receiver section of the UART has transferred an incoming character to the Receiver Data Buffer Register (RBUF). It is cleared by setting bit 0 (Reader Enable) in RCSR, by addressing (read or write) RBUF, or by INIT. If bit 6 in RCSR is set, the setting of bit 7 will cause an interrupt request to be generated.

6 Receiver Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 7 in RCSR is set. It is cleared by INIT, or by the program.

5 Dataset Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 15 in RCSR is set. It is cleared by INIT, or by the program.

4 Unassigned

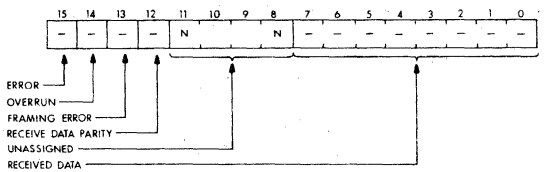
3 Secondary Transmitted Data. Read/Write. This bit, when set, causes the signal on Circuit SBA, pin 11, to the dataset to go high (spacing), and when cleared, causes that signal to go low (marking). It is cleared by INIT, or by the program.

2 Request to Send. Read/Write. This bit, when set, causes the signal on Circuit CA, pin 4, to the dataset to go high, and when cleared causes that signal to go low. There is a Jumper on the DL11-E Card such that this bit may be made to control the Forced Busy lead (pin 25) to the dataset instead of Circuit CA. It is cleared by INIT, or by the program.

1 Data Terminal Ready. Read/Write. This bit, when set, causes the signal on Circuit CD, pin 20 to the dataset to be asserted (high), and when cleared causes that signal to be negated (low). This bit is not cleared by INIT, and may be set/reset only by the program. It must be set or cleared as appropriate by the program after power is applied to the machine, since its state at that time is undefined.

0 Reader Enable. Write only. This bit, when set, causes the Reader Run Relay on certain DIGITAL-supplied teleprinters to advance the paper tape reader. It also clears Receiver Done (bit 7) in RCSR. It is cleared by INIT, or when bit 11 in RCSR is set. Operation of bit 0 is possible in all DL11's, but its associated 20 mA output circuit is used only on DL11-A and C.

Receiver Data Buffer Register (RBUF) 77XXX2



BIT	DESCRIPTION AND OPERATION

15* Error. Read only. This bit is set if bit 14, 13, or 12 (or any combination of these bits) in RBUF is set (logical OR of bits 14, 13, 12). It is cleared only if none of the above bits are set.

14* Overrun. Read only. This bit is set if bit 7 in RCSR (Receiver Done) is not cleared before the UART attempts to present a new character to RBUF, i.e., if the UART attempts to set bit 7 in RCSR, and it is already set. The previous character in RBUF is lost, and the new character replaces it.

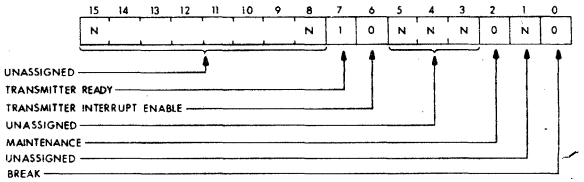
13* Framing Error. Read only. This bit is set if the UART, at the time it samples the received data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, "BREAK" signal, or excessive distortion of the received character.

12* Receive Data Parity Error. Read only. This bit is set by the UART if the parity of the received data character does not agree with the parity specified to the UART (odd or even). This bit is always zero if the "no parity check" option is specified. Bits 14, 13, and 12 are updated each time a character is received.

7-0 Received Data. Read only. These bits contains the last complete character assembled by the UART. If the character length specified to the UART is less than 8 bits, the character will appear right justified (low order bit in bit 0). The unused high order bits will contain 0.

* NOTE The state of bits 14, 13, and 12 applies to the character currently in RBUF, bits 7-0. It is not necessary to clear them in order to receive the next character. Also, these bits are not enabled in the DL11-A and DL11-B, and will appear as zero in these models when read by the program. This is to provide program compatibility with the DIGITAL KL11.

Transmitter Status Register (XCSR) 77XXX4



BIT	DESCRIPTION AND OPERATION
7	Transmitter Ready. Read only. This bit is cleared when a data character is loaded into XBUF. It is set when XBUF can accept another data character, and by INIT. If bit 6 in XCSR is set, this bit, when set, will cause an interrupt request to be generated. Note that this bit is set, not cleared, by INIT.
6	Transmitter Interrupt Enable. Read/Write. This bit, when set, will cause an interrupt request to be generated whenever bit 7 in XCSR is set. This bit is cleared by INIT and by the program.
5-3	Unassigned.
2	Maintenance. Read/Write. This bit, when set, causes data emitted at the serial output of the UART transmitter section to appear at the serial input of the receiver section. In addition, it forces the receiver to run at the same data rate as the transmitter, and disconnects the external serial line input to the receiver. It is cleared by INIT, and by the program.
1	Unassigned.
0**	BREAK. Read/Write. This bit, when set, clamps the serial data output of the UART transmitter to a spacing (logical 0) condition. The transmitter will appear to the program to function normally if characters are presented to XBUF, but a continuous spacing signal will appear on the Transmitted Data lead (Circuit BA). This bit is cleared by INIT, and by the program.

** Not available on DL11-A and DL11-B.

Transmitted Data Buffer Register (XBUF) 77XXX6

BIT	DESCRIPTION AND OPERATION
7-0	Transmitted Data. Write only. These bits contain the data character to be transmitted by the UART. If the data character contains fewer than 8 data bits, the character must be right justified when loaded into XBUF. The bits of the character are presented to the serial line low-order bit (bit 0) first. A bit set to one in XBUF will cause a marking condition to appear on the transmitted data lead for one bit time. Cleared by INIT.

SPECIFICATIONS

Function:	Provides an interface between the PDP-11 UNIBUS and a single asynchronous bit serial communications channel.
Mechanical:	The DL11 consists of one quad module and a connecting cable terminated in a plug appropriate to the data communications equipment to be connected.
Operating Mode:	Full or half duplex under program control.
Data Format:	Asynchronous, serial by bit. One start and one, one and one-half (5-level codes only), or two stop bits, supplied by the hardware. The DL11-A and B are supplied with 8 level, no parity, 2 stop bit code configuration. The DL11-C, D, and E will accommodate characters of 5, 6, 7, or 8 bits, with or without even or odd parity. The data format must be the same for transmitted and received data. The data format must be specified at the time of order. A one (1) presented by the program to any bit in the Transmitted Data Register will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one (1) in the Received Data Register, and a Spacing condition will be presented as a zero (0).
Order of Bit Transmission:	Low order bit first.
Distortion:	The DL11 receiver will operate properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received data bits, and up to ± 4.5%, long-term speed distortion, provided the data format contains at least one and one-half stop units. If the data format contains only one stop unit, the speed tolerance is ± 4%. The DL11 transmitter operates with less than 3% bit-to-bit or long-term distortion.
Bus Loading:	One DL11 presents one unit load to the PDP-11 UNIBUS.
Electrical Interface:	DL11-A and DL11-C provide a 20 mA active current loop for both send and receive leads for connection to local teleprinters such as the DIGITAL LA30-C and Teletype Models 33 and 35, and displays such as DIGITAL VT05 Terminal.

The DL11-A and DL11-C are supplied with a 2¼ ft., 6-conductor cable terminated with a female MATE-N-LOC connector.

The DL11-B and DL11-D provide a voltage level interface and connector whose signal levels and connector pinning conform to Electronic Industries Association Standard RS232C and CCITT Recommendation V.24. The leads supported by the DL11-B and D are:

Protective Ground, Circuit AA, pin 1.

Transmitted Data, Circuit BA, pin 2.

Received Data, Circuit BB, pin 3.

Signal Ground, Circuit AB, pin 7.

Data Terminal Ready, Circuit CD, pin 20*.

Request to Send, Circuit CA, pin 4*.

* These leads are held ON (logical 1) by the hardware.

The DL11-B and D are supplied with a 25-ft., 25-conductor cable terminated in a Cinch DB25P plug with a protective hood.

The DL11-E provides a voltage level interface as described above for the DL11-B, but in addition supports the following leads, giving full dataset control capability to the computer program:

Data Terminal Ready, Circuit CD, pin 20.

Clear to Send, Circuit CB, pin 5.

Request to Send, Circuit CA, pin 4.

Received Line Signal Detector (Carrier), Circuit CF, pin 8.

Ring Indicator, Circuit CE, pin 22.

Secondary Transmitted Data, Circuit SBA, pin 11*.

Secondary Received Data, Circuit SBB, pin 12*.

* Note that the pin assignment of these two leads conforms to that of the Bell 202 Dataset, rather than to the cited EIA/CCITT standard.

The DL11-E is supplied with a 25 ft., 25-conductor cable terminated in a Cinch DB25P plug with protective hood.

Power Requirements: The DL11 requires 1.8 amps of + 5v., .05 amps of + 15v., and .15 amps of — 15v.

Data Rate: The DL11 is supplied to customer order with 13 standard data rates in four groups.

Group 1. 110 baud receive and transmit.

Group 2.** 134.5 baud receive and transmit.

Group 3. Following 8 speeds, which may be different for receive and transmit: 50, 75, 150, 300, 600, 1200, 1800, 2400 baud.

Group 4.** Following 8 speeds, which may be different for receive and transmit: 200, 300, 600, 1200, 2400, 4800, 7200, 9600 baud.

** Not available on DL11-A and DL11-B.

Models

DL11-A: Single Asynchronous Serial Line Interface Unit. Full duplex operation, 20 milliampere neutral current loop electrical interface. Replaces and is program compatible with the DIGITAL KL11 for control of PDP-11 console teleprinters. Furnished with 2¼-ft. cable terminated in female Mate-n-Loc connector, suitable for connection to DIGITAL terminals. Supplied only with code configuration of 8 data bits, 2 stop bits, no parity generation or checking. Customer must specify speed groups 1 (110 baud) or 3 (50, 75, 150, 300, 600, 1200, 1800, 2400 baud) only. If not specified, unit will be supplied at 110 baud.

DL11-B: As DL11-A above, except electrical interface conforms to EIA RS232C. Supports Transmitted and Received data leads. Request to Send and Data Terminal Ready leads are clamped always ON. Supplied with 25-foot cable terminated by Cinch DB25P plug for connection to modem (BC05C-25 cable).

DL11-C: Single Asynchronous Serial Line Interface Unit. Full duplex operation, 20 mA neutral current loop electrical interface. Code configuration (5, 6, 7, 8 data bits; 1, 1.5, 2 stop bits; odd, even, or no parity) and speed (Groups 1, 2, 3, or 4) customer specified. Furnished with 2¼ ft. cable terminated in female Mate-n-Loc connector, suitable for connection to DIGITAL LA30-C DECwriter. DIGITAL VT05 Display Terminal, or DIGITAL-supplied Teletype. If speed and code configuration are not specified, unit will be supplied as 8 data bits, no parity, 2 stop bits, 110 baud.

DL11-D: As DL11-C above, except EIA RS232C electrical interface. Supports Transmitted and Received Data leads, and clamps ON Request to Send and Data Terminal Ready leads. Furnished with 25 ft. cable terminated in Cinch DB25P plug, for connection to modem (BC05C-25 cable).

DL11-E: As DL11-D above, except supports full dataset control interface, including Data Terminal Ready, Clear to Send, Request to Send, Carrier, Ring, Secondary Received and Secondary Transmitted leads.

AUTOMATIC CALLING UNIT INTERFACE, DN11

DESCRIPTION

With the DN11 and a Bell 801 Automatic Calling Unit (ACU), any PDP-11 can dial any telephone number in the Direct Distance Dial Network and establish a data link. The DN11 is a digit-buffered interface, and digits to be dialed are presented as four-bit binary numbers. The interface drives the ACU with EIA-232-C voltages and is connected via a standard 25-pin plug.

The programmer has access to all lines of the 801 through the DN11. The 801 presents the following leads to the DN11: Power Indicator, Data Line Occupied, Abandon Call and Retry, Data Set Status and Present Next Digit. The DN11 provides the following leads to the 801: Digit Present, Call Request and four Digit Leads.

Because the PDP-11 UNIBUS serves as a multiplexer, multiple automatic calling units can be added to the PDP-11. One PDP-11 System Unit accepts up to four 801 ACU Interfaces. Each interface looks like one device to the UNIBUS.

The Sequence of Operations

The following describes the use of the DN11 to originate a DDD call. This is an automated version of the procedure that everyone goes through when placing a telephone call.

1. Turn 801 power on (PWI = 0).
2. Check for unoccupied data line (DLO = 0).
3. Set Call Request bit (FCRQ = 1).
4. The 801 will seize the line on receiving the dial tone and assert Present Next Digit which causes a PDP-11 program interrupt (FPND = 1).
5. The line is now in use and the Data Line Occupied bit is set (DLO = 1).
6. The first digit to be dialed is provided by loading the four least significant bits of the byte into the digit bits (8 to 11) of the DN11 status register. The upper four bits of the byte are read-only and can have any value during the loading of the four low-order bits.
7. The 801 is informed that the 1st digit has been loaded by asserting the Digit Present Bit (FDPR = 1).
8. The 801 then reads Digit leads 1 through 4 and lowers Present Next Digit Lead (FPND = 0).
9. The hardware responds and lowers Digit Present Lead (FDPR = 0).
10. The 801 then dials the first digit and again raises Present Next Digit Lead (FPND = 1).

11. The next digit is loaded and the Digit Present bit is asserted (FDPR = 1).

12. Sequences 6 through 10 are repeated until all digits have been dialed.

13. When the last digit has been dialed, one of two procedures must be used to complete the call.

    a) If "handshaking signals" are used (Bell 100 series modems or equivalent):

    A Detect Answer option is used. The 801 retains line control and looks for an answering tone, from the called station. Upon receiving the tone the modem is connected to the line, Data Set Status is asserted and a program interrupt is generated (DSS = 1). This stops the Abandon Call and Retry timer which would have been initiated had no tone been received. These, in turn, would have generated a signal to the DN11 and cause a program interrupt with the Abandon Call and Retry bit set (ACR = 1). The program would then either retry or drop the call.

    b) If using modems without the automatic handshaking feature:

    The End-of-Number (EON) mode must be used. EON is sent after the last digit has been dialed. This causes the 801 to connect the modem to the line and assert Data-Set Status (DSS = 1). However, the modem and its controller must be able to determine when the called station has answered and is sending data. To do this, it is necessary to use an 801 with option "Y" (available from the Telephone Company). This option lets the Abandon Call and Retry timer continue running even after the DSS bit has been set. When the ACR timer times out it will notify the user of the line to check if data is being received by the modem.

14. There are two options available when terminating a call:

    a) The Call Request bit is set to zero (FCRQ = 0). This will remain until the Data Line Occupied bit also goes to zero (DLO = 0), which is a necessary condition before a new call can be initiated.

    b) If the 801 option "Z" is used, the call can be terminated by clearing Data Terminal Ready in the modem. In this case, dropping Call Request will not terminate the call. However, it must be dropped before a new call can be attempted.

15. Should the 801 lose power during a call an interrupt will be generated and the Power Off bit will be set (PWI = 1). The interface will not return an interrupt if the Call Request bit is set with the power off (FCRQ = 1).

Programming

Each ACU interface contains one register and therefore requires one

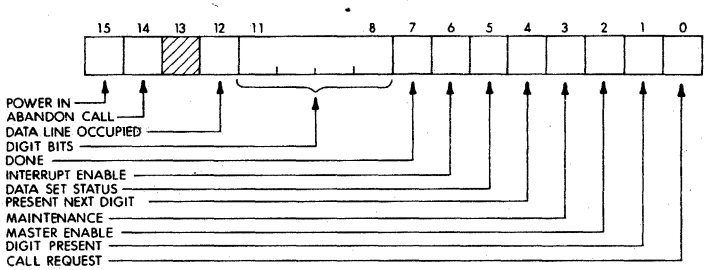
16-bit address. Address space has been assigned for 64 interfaces. The four addresses for the four interfaces that can be plugged into one system unit must be consecutive addresses starting with 775XX0 where XX = 20 for the first line. If only one line is in use, it uses address 775 200. Interface number 2 has address 775 202, and interface number 64 has address 775 376.

Note: In addition to the individual Interrupt Enable bit for each interface, there is a master enable bit associated with line number 1 of a given system unit. It enables the interrupts for the entire group. The master enable bit on lines 2 through 4 of a given system unit are ignored by the interface.

Each set of four DN11's require one interrupt vector. The vector address for communications options are assigned in the range from 300 to 777. (See Appendix A).

All units are shipped with the bus request line set to BR4. This can be changed in the field with a Bus Request Priority Jumper Plug.

ACU Interface Status Register



BIT	NAME	FUNCTION
15	Power Indicate (PWI)	This bit is normally zero and is set by the ACU whenever power is switched off at the unit. If a call is in progress at that time, DONE is set. This causes an interrupt if INTENB and MINAB = 1 (Read only).
14	Abandon Call and Retry (ACR)	A control lead from the ACU. This bit is set by the ACU whenever an internal timer times out. The timer is reset by the ACU whenever it gives PND and is for detecting wrong numbers and busy signals. It is inhibited by the presence of DSS except if

		the 801 option "Y" is in use; it times out even then and gives an interrupt (by setting DONE). This is used when the programmer wants a timer to detect wrong numbers and busy signals.
12	Data Line Occupied (FDLO)	This bit is set by the ACU whenever the line to the telephone central office is being used by the ACU. It allows the programmer to test the ACU to see if the last call was successfully terminated before he tries to use it for the next one (Read only).
11-8	Digit Bits (NB1-4)	These four bits are control leads to the ACU. These low order bits of the second byte make up the BCD digit to be dialed. Since the high-order four are read only, it does not matter what is in them during a load, and the programmer may use them as he wishes. In MAINT mode, these bits are used to drive the four control lines that can cause interrupts. See bit 3 for description (Read/Write).
7	DONE	This bit is set to indicate that the ACU is done with the previously requested action and ready to accept new data, usually the next digit in a sequence to be dialed. The conditions that set DONE are listed (CRQ must be a one): 1. Transition of PND to one (after CRQ set or previous DPR set). 2. Transition of DSS to one (after last DPR or EON). 3. Transition of ACR to one (if timeout error—anytime). 4. Transition of PWI to one (if power switched off) (Read/Write)
6	Interrupt Enable (INTENB)	This bit allows the setting of done to cause an interrupt if the master enable bit (bit 02 line #1 of a system unit) is set (Read/Write).
5	Data Set Status (DSS)	Control lead from ACU. This is a statement by the ACU that the called party has answered and that the associated data set now has control of the line. It is accom-

panied by the setting of DONE to obtain an interrupt. It remains set until after the end of the call (or until the data terminal ready lead to the associated modem is dropped which then drops FDSS).

If the associated modem answers a call while the dialer is in use (CRQ = 1), then DSS will be enabled and DONE set. If interrupt Enable is set there will be an interrupt (Read only).

4 Present Next Digit (FPND)

Control lead from the ACU. This is a request by the ACU for the program to load another digit during dialing. It is accompanied by the setting of DONE to obtain an interrupt. It is cleared by the ACU when the digit is accepted (after DPR is set) and will remain off at least 600 ms before coming up for the next request (Read only).

3 Maintenance (MAINT)

This bit, when set, allows checking of the interface without a connected ACU. It allows FCRQ to be read and switches the ACU response lines—PND, DSS, PWI and ACR to the output of the digit lines for testing purposes.

Bit	Digit	ACU Line to Ctl	Bit
08	NB1	PND FPND	04
09	NB2	DSS FDSS	05
10	NB4	PWI PWO	13
11	NB8	ACR FACR	14

This bit also forces CRQ (to ACU) off and forces FDLO (Bit 12) on. (Read/Write).

2 Master Enable (MINAB)

Allows the program to disable then reenable all 4 ACU interrupts easily with one bit. This bit is connected for only one of the four possible lines which mount in one system unit (Read/Write).

1 Digit Present (FDPR)

Control lead to the ACU. This bit must be set by the program after it loads the next digit (in response to a PND request) to inform the ACU to continue dialing. The interface automatically clears this bit when the ACU clears PND to indicate acceptance of the digit (Read/Write).

0	Call Request (FCRQ)	Control lead to ACU. This bit starts the Automatic Calling Sequence (Write only).

SPECIFICATIONS

Control Signals:	All control leads are brought into the DN11 from the Bell 801. All leads are EA RS-366 and CCITT compatible. All leads are fail-safe (i.e., they appear off if the 801 loses power).
Bus Load:	One DN11 interface represents one unit load to the PDP-11 UNIBUS. Thus, four controls in one System Unit represent four unit loads.
Program Interrupts:	Normal interrupts are caused during a call by: 1. Transition of PND to a one. Sets DONE. Digit desired. 2. Transition of DSS to a one. Sets DONE. Data set connected. 3. Transition of ACR to a one. Sets DONE. Busy or wrong number. Error interrupts are caused during a call by: 1. Transition of PWI to off. Sets DONE. Power to ACU was switched off. (Note: Appropriate Enable bits must be set.)
Physical Connection:	25-foot cable with RS-232-C compatible 25-pin male connector.
Power Required:	1.4 Amps of + 5V for the first line; 0.4 Amps of + 5V for the second through the fourth lines.
Temperature/Humidity:	0°-40°C with Relative Humidity of 20% to 90%, non-condensing.

Pin Numbers on the 801 Cable

Output

Pin	Designation	Abbr.
4	Call Request	CRQ
5	Digit Present	DPR
14	Digit Lead	NB1

15	Digit Lead	NB2
16	Digit Lead	NB4
17	Digit Lead	NB8

Input

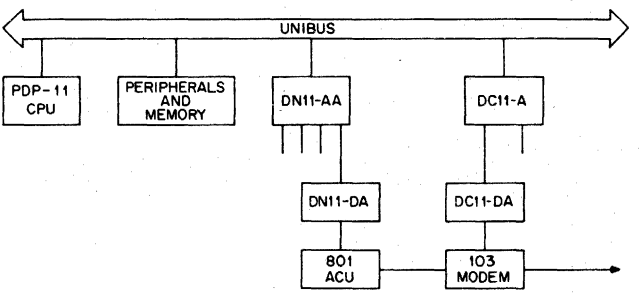
Pin	Designation	Abbr.
5	Present Next Digit	PND
6	Power Indication	PWI
22	Data Line Occupied	DLO
1	Frame GND	FGD
7	Signal GND	SGD

Models

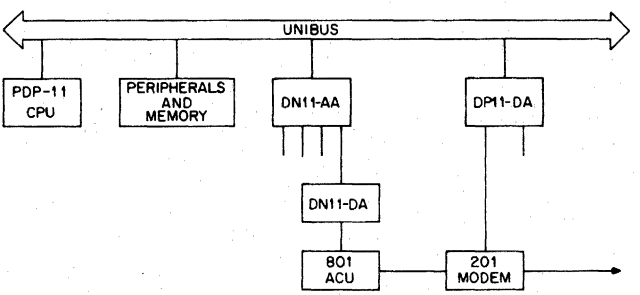
DN11-AA — Prewired System Unit for up to four Bell 801 Automatic Calling Unit interfaces. (DN11-DA)

DN11-DA — One Line Interface for a Bell 801 Automatic Calling Unit. Includes 25' Cable (Up to four DN11-DA's may be mounted in a DN11-AA).

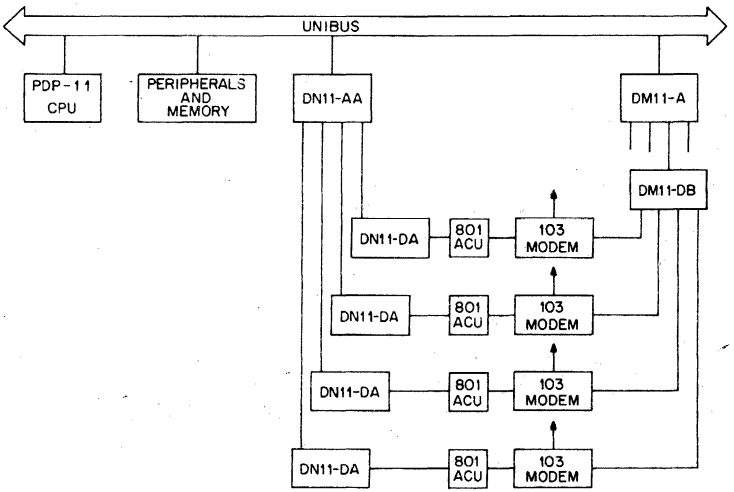
CONFIGURATIONS



ASYNCHRONOUS SINGLE-LINE INTERFACE



SYNCHRONOUS SINGLE-LINE INTERFACE



ASYNCHRONOUS MULTIPLE LINE INTERFACE

SYNCHRONOUS INTERFACE, DP11

DESCRIPTION

The DP11 provides a double-buffered program interrupt interface between a PDP-11 and a serial synchronous line. This interface allows the PDP-11 to be used in remote batch and remote concentrator applications. With the DP11, a PDP-11 can also be used as a front end synchronous line controller to handle remote and local synchronous terminals.

The DP11 interface offers flexibility. It handles a wide variety of terminals and line disciplines (i.e., line control procedures and error control techniques). A programmer can vary sync character, character size, and modem control leads. Automatic sync character stripping and automatic idling are also program selectable. While idling, the DP11 transmits the contents of the sync buffer.

The DP11 design provides individual interrupt vectors and hardware interrupt priority assignments for the transmitter and receiver. Interrupt priority is jumper selectable. This feature, coupled with the automatic transmit idle capability, enables dynamic system adjustment to peak message activity. For example, the programmer can temporarily ignore the transmitter if receive activity is high.

Because the PDP-11's UNIBUS serves as a multiplexer, multiple synchronous lines can be added to a PDP-11. One PDP-11 system unit's worth of mounting space is used for each independent synchronous line interface unit.

Operation

The DP11 is a fully character-buffered synchronous serial line interface capable of two-way simultaneous communications. The DP11 translates between serial data and parallel data. Output characters are transferred in parallel from the computer to a buffer register where they are serially shifted to the communication line. Input characters from the modem are shifted into a register, transferred to a buffer register, and made available to the PDP-11 on an interrupt basis.

Both the receiver and the transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts.

The clocking necessary to serialize the data is normally provided by the associated high-speed synchronous modem. Alternately, the internal clocking option can be used for local terminals when no external clocking is available.

Receiver

Synchronization between the DP11 and the transmitting terminal is established by a sync character code. Since the sync code and character size are programmable, the programmer must load them in the receiver status register prior to synchronization. After this is done, the controller will scan the incoming bit stream until it finds two sequential sync char- for eight-bit ASCII is 26_8(00010110) and eight-bit IBM BISYNC is 32_{16}(00110010).

Once synchronization is achieved, serial data can be transmitted and received continuously (no start or stop bits are required as in asynchronous communications).

The DP11 can be in one of two modes while receiving data:

1. All sync characters will be automatically stripped from the incoming data stream, if the receive active bit is set and the strip sync bit is set.

2. Sync characters will be treated as normal data and cause an interrupt request, if the receive active bit is set and the strip sync bit is not set.

Incoming characters appear right justified in the receive data buffer. The first bit received appears as the right-most bit in the buffer. When the character has been received, its parity is available for testing by the programmer.

There are two independent interrupt request levels and interrupt vectors associated with the DP11. One is for the receiver and the other is for the transmitter and the DP11 status.

A receive interrupt request is generated as the received character is transferred into the receive data buffer. If the program does not remove the character from the data buffer before the next character is transferred, a data overrun error bit is set in the DP11 status register. If the status interrupt enable bit is set, this error condition will cause a DP11 status interrupt request.

In half-duplex operation, setting the half-duplex bit will disable the receive logic when request to send is on. This prevents the transmitted character which appears on the receive data lead from also causing a receive interrupt.

Transmitter
The transmitter has two modes of operation:

1. When the idle sync bit is not set the transmitter must be refreshed approximately once a character time (i.e., (1/Baud) (bits per character—½) seconds) or the DP11 will stop transmitting (hold the transmitted data line in the binary 1 mark condition) and set the Request-to-Send to the modem to the off state.

2. When the idle sync bit is set the logic will transmit from the sync buffer if the programmer does not refresh the transmitter in approximately one character time (i.e., (1/Baud) (bits per character—½) seconds).

The transmitter has a separate interrupt enable control bit from the receiver and the DP11 status. When the transmitter interrupt is enabled, an interrupt request is generated when the leading edge of each character is presented to the line.

Control Leads

The modem control leads are provided to interface the DP11 to Bell 201, 303 or equivalent modems. These leads allow the DP11 to be used in switched or dedicated, full- or half-duplex configurations. The DP11 status interrupts have a separate interrupt enable bit but share the same bus request level and interrupt vector as the transmitter. If the status interrupt is enabled, a carrier flag, data overrun, or ring will generate interrupt requests. The control leads are fail-safe, i.e., they will appear off if the modem loses power.

The DP11-DA is connected to a Bell model 201 modem (or equivalent) by a 25-ft. cable terminated at the modem end with a 25-pin male connector. Standard interface signals are bipolar (EIA/CCITT).

Connector Pin Assignments for Bell Series 201 Modems

Pin	Signal
1	Signal or Protective Ground
2	Send Data
3	Receive Data
4	Send Request
5	Clear to Send
6	Interlock
7	Signal Ground
8	Carrier On-Off
15	Serial Clock Transmit
17	Serial Clock Receive
20	Remote Control
22	Ring Indicator 1
24	External Timing

The DP11-DC is connected to a Bell 303 modem (or equivalent) by a 25-ft. cable terminated at the modem end by a male 12-pin coaxial connector. Standard interface signals are the current mode type where a mark is 5 milliamperes or less and a space is 23 milliamperes or greater. However, there are two exceptions: data terminal ready and ring indicator. These signals are normally bipolar levels (EIA/CCITT).

Connector Pin Assignments for Bell Model 303 Interface

Pin	Signal
E	Send Data
K	Receive Data
D	Send Request
C	Clear to Send
F	(Center Conductor) AGC Lock
M	(Center Conductor) Carrier On-Off
J	Serial Clock Transmit
L	Serial Clock Receiver
M (Outer Conductor)	Data Terminal Ready*
F (Outer Conductor)	Ring Indicator*
H	Serial Clock Transmit (External)

*EIA Levels

Maintenance
The DP11 has on-line diagnostic capability. When the maintenance mode is set, the transmitter output is connected to the receiver input. Additionally, the clear-to-send lead is simulated and the transmit receive clocks are replaced by a 3000 Hz clock. This allows the DP11 diagnostics to be run without operator intervention (i.e., no cables must be removed).

Programming
Each line unit contains five registers and, hence, requires five addresses. Address space has been assigned for 32 line units. Line unit number 1 starts at 774 770, line unit 2 is at address 774 760, up to line unit 32 at address 774 400.

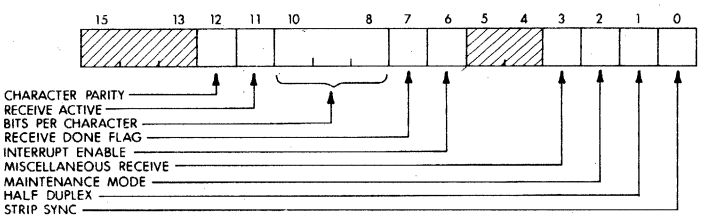
The five registers and their addresses are listed below (Note the XX = 77 for the first line unit and decreases to 40 for the 32nd line unit).

REGISTER	ADDRESS
Receiver Status Register	774XX0
Receiver Buffer	774XX2
Sync Register	774XX3
Transmitter Control and Status Register	774XX4
Transmitter Buffer	774XX6
Extended Sync Register (4 bits)	774XX7

Each synchronous modem interface requires two interrupt vectors: one for receive done and the other for transmit done and status. The vector addresses are assigned from 300 to 777. (See Appendix A.)

Each DP11 has two independent bus request levels. All units will be shipped with both bus requests lines set to BR5. These levels are field changeable with a priority jumper plug.

Receiver Status Register 774XX0



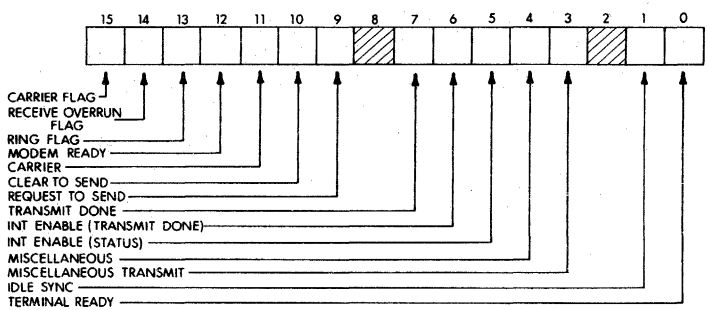
BIT	NAME	FUNCTION
12	Character Parity	The character parity (VRC) bit indicates the parity of the last character assembled and contained in the receive buffer. A

		"one" indicates "odd" character parity, while a "zero" indicates "even" parity. This bit is changed at the same time the receive done flag is set.
11	Receive Active	Receive active is set when the hardware recognizes two consecutive sync characters. This bit is read/write.
10-8	Bits Per Character	Selects 6, 7, 8, 10, 11 or 12 bits per character as follows: 000 8 bits per character 001 7 bits per character 010 6 bits per character 011 Not Used Optional with DP11-CA: 100 12 bits per character 101 11 bits per character 110 10 bits per character 111 Not Used These bits are write/read and initialize selects 8 bits per character.
7	Receive Done Flag	The receive done flag indicates that the receive buffer contains an assembled character. If the program does not respond to this flag in 1/Baud X bits per character seconds, the receive overflow flag will be set (causes a transmit status interrupt). This bit is read/write and is cleared by: a. Initialize b. By gating the receive buffer to the UNIBUS.
6	Interrupt Enable (Receive Done)	The receive done interrupt enable allows a receive interrupt to occur when the receive done flag is set. This bit is read/write.
5	Not Used	
4	Not Used	
3	Miscellaneous Receive	Miscellaneous receive is provided to monitor any non-standard modem status required by the user. Changes can be implemented by computer special systems or by the user. Standard units will be wired to secondary receive data (i.e. 202). This bit is read only.
2	Maintenance Mode	Maintenance mode provides an internal data loop which connects the transmitter

output to the receive input. Additionally, the clear-to-send lead is simulated by the hardware. This mode of operation provides its own clock which will handle data at approximately 3000 Baud.

1	Half Duplex	If set, request to send on will inhibit the receive logic. This bit is read/write.
0	Strip Sync	If set, all sync characters following receive active will be stripped from the incoming serial data. This bit is read/write.

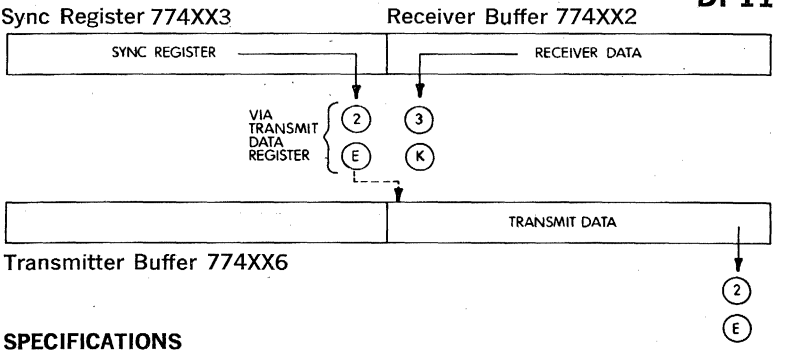
Transmit Status Register 774XX4



BIT	NAME	FUNCTION
15	Carrier Flag	This bit is set if the modem carrier lead made an on to off transition. A transition occurring on this lead while data is being received, indicates a high probability of data errors. Also, the receive synchronism with the incoming data bits is no longer reliable and a new sync sequence should be established. This is done by writing a zero into the receive active bit and requesting a re-sync (i.e., sync, sync) from the remote terminal.
14	Receive Overrun Flag	This bit is set if the receive buffer was not read in 1/Baud x bits per character time following the receive done flag. This flag indicates a loss of at least one data character and suggests that a re-transmission be requested. This bit is read/write.

13	Ring Flag	A one indicates that a ring signal has been received by the modem. Also the flag will cause a transmit status interrupt if interrupt enable (status) is set. This bit is read/write.
12	Modem Ready	This bit reflects the current state of the data set ready (also interlock) lead. This bit indicates that the modem is powered and not in test, talk, or dial mode. This bit is read only.
11	Carrier	This bit reflects the current state of the modem carrier (agc if 300 series) control lead. An off indicates that no signal is being received or that the received signal is unsuitable for demodulation.
10	Clear to Send	This bit reflects the current state of modem clear-to-send lead. A "one" indicates that the modem is ready to transmit data. This signal is a result of the request-to-send lead in a half-duplex configuration. Read only.
9	Request to Send	Request to send is a hardware function. This bit is set on the second positive transition of the transmit clock if the transmit buffer is loaded or if the idle sync bit is set. This bit is read only and is cleared: a. By initialize b. If idle sync is not set and the transmit buffer was not refreshed in 1/Baud x (bits per character—½) seconds after transmit done was set. Request to send will go to zero on the second positive transition of the transmit clock following the end of bit presented to the line.
8	Not Used	
7	Transmit Done	The transmit done flag is set to a one when the leading edge of the first bit of each character is presented to the line. Additionally, this flag will cause a transmit/status interrupt if interrupt enable (transmit done) is set. This bit is read/write and is cleared by: a. Initialize b. By loading the transmit buffer

6	Interrupt Enable (Transmit Done)	The interrupt enable (transmit done) if set allows the transmit/status interrupt to be generated by transmit done. This bit is read/write.
5	Interrupt Enable (Status)	Interrupt enable (status) if set allows the transmit/status interrupt to be generated by carrier flag, receive over run flag and by ring flag. This bit is read/write.
4	Miscellaneous	Provided to satisfy a variety of needs; such as: new sync rate selector, etc. This lead is expected to be wired by Computer Special Systems or the end user. This bit is write only.
3	Miscellaneous Transmit	Provided to satisfy a variety of needs such as: new sync, rate selector, etc. This lead is expected to be wired by Computer Special Systems or the end user. Standard units will be wired for secondary transmit data (i.e. 202). Additionally, the secondary transmit data line is used to generate the receive and transmit clock in the external loop test configuration. Note: The external loop configuration will not operate if the miscellaneous transmit lead is reassigned. This bit is read/write.
2	Not Used	
1	Idle Sync	Allows transmit from the sync buffer. Note: Transmit done is set (if enabled) as the first bit of each character as presented to the line. If the idle sync bit is set when the transmit is inactive, the logic will raise request to send and begin transmitting from the sync register. Once active, the transmit shift register will be loaded from the sync register if the program has not responded to transmit done in 1/Baud x (bits per character—$\frac{1}{2}$) seconds. This bit is read/write.
0	Terminal Ready	Controls switching of the data communication equipment to the communication channel. Auto dial and manual call origination: maintains the established call. Auto answer: allows handshaking in response to a ring signal. This bit is read/write.



SPECIFICATIONS

Type:	Double-buffered transmit and receive
Operating Mode:	Full- or half-duplex selected under software control
Maximum Data Rate:	50,000 bits per second (9600 bits per second with the DP11-DA)
Data Format:	Character size is variable under program control to 6, 7, or 8 bits (10, 11, or 12 bits optional)
Clocking:	Synchronous clock from the modem (internal clock optional)
Sync Character:	Programmable
Sync Detection:	Two successive sync characters required to activate the unit.
Bit Transmission:	Low order bit first
Parity:	Parity check bit provided on incoming characters

Modem Compatibility (Typical)

Type	Speed (Baud)	Communications Channel
Bell 201A	2000	direct distance dialing network Type 3002(C2)
Bell 201B	2400	leased line only; Type 3002 (C2)
Bell 303B	19,200	leased line only; half group (6 voice-band lines)
Bell 303C	50,000	leased line only; group (12 voice-band lines)

Data and Modem Control Signals: All leads of Bell 201 and 303 modems are brought into the unit. All leads are EIA RS-232-C and CCITT compatible for the 201

	modem. All leads for the 300 Series are current mode as defined in the appropriate reference manual.
Program Interrupts:	Receive Done, Transmit Done, Carrier Flag, Receive Overrun, and Ring (If appropriate Enable bits set)
Bus Load:	One line unit represents one unit load to the PDP-11 UNIBUS.
Physical Connection:	For 201 modems. 25-foot cable with RS-232-C compatible 25-pin male connector. For 303 modems, 25-foot coaxial cable with appropriate connector.
Space Required:	1 System Unit for one interface.
Power Required:	2.5 Amps of + 5 Volts
Temperature/Humidity:	0°40°C with 20 to 90% noncondensing humidity.

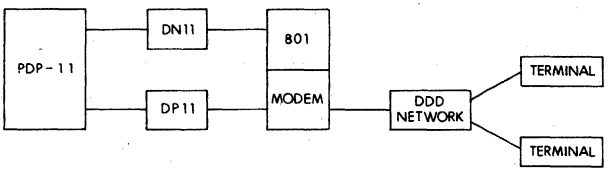
Models

DP11-DA	Full/half duplex synchronous line module set. Double buffered. 6, 7, or 8 bit characters. EIA/CCITT termination suitable for direct use with 201 modems. Includes 25-foot modem cable.
DP11-DC	Same as above except suitable for direct use with 303 modems. Includes 25-foot modem cable.
DP11-CA	Allows the DP11 to handle 10, 11, or 12 bits per character.
DP11-KA	Internal clock option. Clocking source to be used for direct connection of DP11 to a local synchronous terminal or a local synchronous computer interface. The following Baud rates are available: 2000, 2400, 4800, 9600, 19.2K, 40.8K and 50K Baud. If no rate is specified, 40.8K Baud will be supplied.
H312-A	Synchronous/asynchronous null modem jumper box. Allows direct connection of a PDP-11 to any peripheral with a modem type interface which conforms to EIA RS-232-C and CCITT specifications. (A DP11-KA is generally required when the HB312A is used with the DP11-DA).

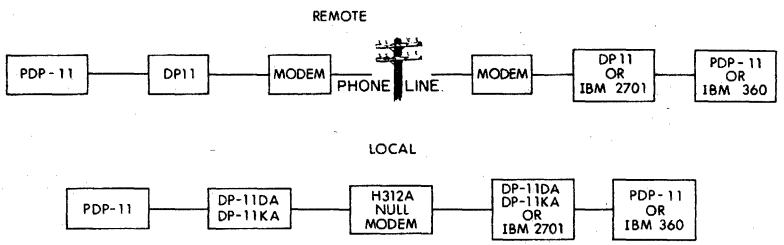
APPLICATIONS

The DP11 is ideally suited for interfacing the PDP-11 to high-speed synchronous lines for remote batch, remote data collection, and remote concentration applications. Multiple DP11's on a PDP-11 allow its use as a synchronous concentrator or front-end synchronous controller to a larger computer.

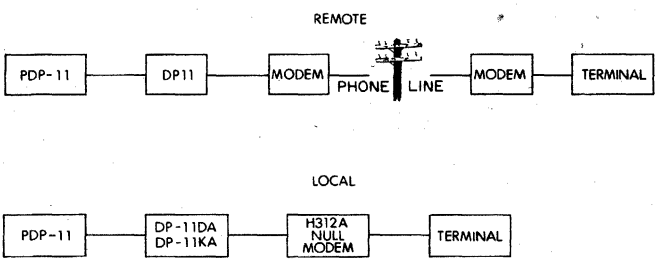
For applications requiring automatic calling the DP11 can be combined with the DN11 auto calling interface and a Bell 801 automatic calling unit. For more information on this interface, refer to the DN11.



The DP11 also can connect two PDP-11's together or a PDP-11 to another large processor (e.g., IBM 360). These connections which could be either remote or local would appear as:



The DP11 can connect a wide variety of terminals to the PDP-11 either remotely or locally. These configurations would be:



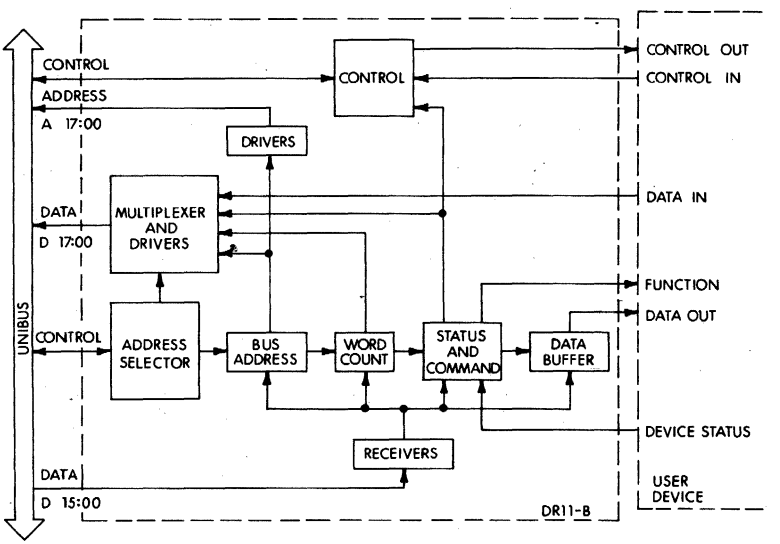
DIRECT MEMORY ACCESS INTERFACE, DR11-B

DESCRIPTION

The DR11-B is a general purpose direct memory access (DMA) interface to the UNIBUS. The DR11-B, rather than using program controlled data transfers, operates directly to or from memory, moving data between the UNIBUS and the user device.

The interface consists of four registers: command and status, word count, bus address, and data. Operation is initialized under program control by loading word count with the 2's complement of the number of transfers, specifying the initial memory or bus address where the block transfer is to begin, and by loading the command/status register with function bits. The user device recognizes these function bits and responds by setting up the control inputs. If the user device requests data from memory or a UNIBUS device, the DR11-B performs a UNIBUS Data In transfer (DATI) and loads its data register with the information held at the referenced bus address. The outputs of this register are available to the user device. (This output data is buffered.) If the user device requests data to be written into memory, the DR11-B performs a UNIBUS Data Out transfer (DATO), moving data from the user device to the referenced bus address. (This input data from the user is not buffered.) Transfers normally continue at a user defined rate until the specified number of words are transferred.

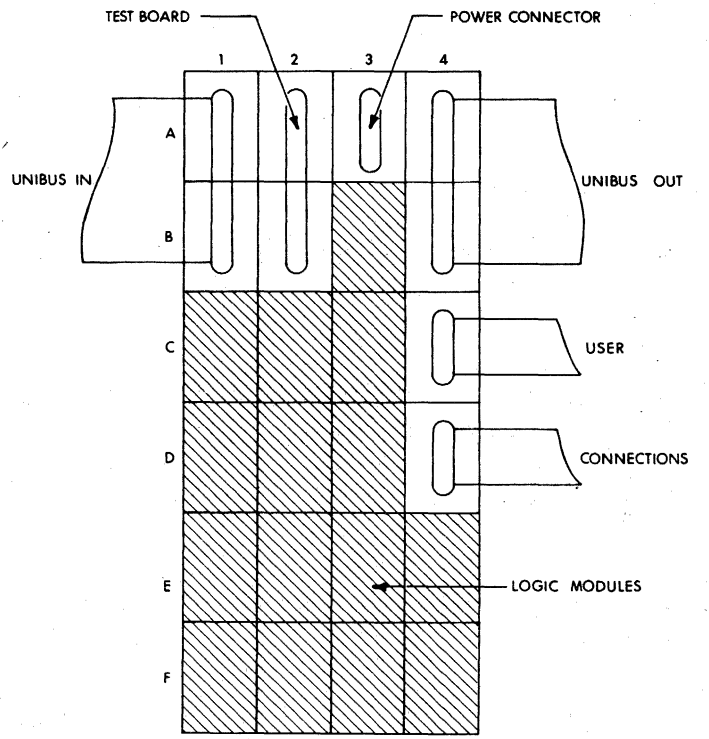
The user is given a number of control lines allowing for flexible operation. Burst modes, read-modify-restore operations, and byte addressing are possible with the control structure.



Physical Description

The DR11-B is packaged in one standard System Unit allowing convenient incorporation into a PDP-11 system. A UNIBUS jumper module (M920) is supplied with the unit.

Connections to the user device are made through two M957 split lug cable boards or one M9760 cable connector board (preferred over the M957's), which are supplied with the unit. Alternatively, an M920 can be used to jumper all user signals to an adjacent BB11 blank mounting panel, which can be used to hold some or all of the device logic. (Neither the additional M920 nor the BB11 is supplied with the unit.)



DR11-B System Unit

REGISTERS

Note: The INIT signal is held asserted internal to the DR11-B whenever an interlock error occurs (M9680 test board neither in slots AB02 for normal operation nor CD04 for maintenance mode).

Word Count Register (DRWC) 772 410
DRWC is a 16-bit R/W register. It is initially loaded with the two's complement of the number of transfers to be made and normally increments up towards zero after each bus cycle. Incrementation can be inhibited by the user device; refer to the WC INC ENB user signal. When overflow occurs (all 1's to all 0's), the READY bit of DRST is set and bus cycles stop. DRWC is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Bus Address Register (DRBA) 772 412
DRBA is a 15-bit R/W register. Bit 0, corresponding to address line A00 is provided by the user device. Along with XBA16 and 17 in DRST, DRBA is used to specify BUS A<17:01> in direct bus access. The register is normally incremented (by 2) after each cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding to A<15:01>) overflows (all 1's to all 0's) the ERROR bit in DRST is set. This error condition (BAOF) is cleared by loading DRBA or INIT. Incrementation can be inhibited by the user device; refer to the BA INC ENB user signal. With this control signal and A00 provided externally, DRBA can be used to address sequential bytes. This is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Status and Command Register (DRST) 772 414
The DRST is used to give commands to the user device and to provide status indicators of the DR11-B control and the user device.

BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition: either NEX (BIT 14), ATTN (BIT 13), interlock error (test board is neither in slots AB02 nor CD04), or bus address overflow (BAOF:DRBA incremented from all 1's to all 0's). Sets READY (BIT 7) and causes interrupt if IE (BIT 6) is set. ERROR is cleared by removing all four possible error conditions: interlock error is removed by inserting test board in CD04 for diagnostic tests or in AB02 for normal operation; bus address overflow is cleared by loading DRBA; NEX is cleared by loading bit 14 with a zero; ATTN is cleared by user device. Read only.
14	Nonexistent Memory (NEX)	Set to indicate that as Unibus master, the DR11-B did not receive a SSYN response 20 usec after asserting MSYN. Cleared by INIT or loading with a 0; can not be loaded with a 1. Sets ERROR. Read only.
13	Attention (ATTN)	Attention bit that reads the state of the ATTN user signal. Sets ERROR. (Used for

		device initiated interrupt.) Set and cleared by user control only. Read only.
12	Maintenance	Maintenance bit used with diagnostic programs. Cleared by INIT. Read/Write.
11-9	Device Status (DSTAT A,B,C)	Device status bits that read the state of the DSTAT A, B, and C user signals. (Not tied to interrupt.) Set and cleared by user control only. Read only.
8	Cycle	CYCLE is used to prime bus cycles; if set when GO is issued, an immediate bus cycle occurs. Cleared when bus cycle begins; cleared by INIT. Read/Write.
7	Ready	Set to indicate that the DR11-B is able to accept a new command. Set by INIT or ERROR; cleared by GO; set on word count overflow. Causes interrupt if bit 6 is set. Forces DR11-B to release control of the Unibus and prevents further DMA cycles. Read only.
6	Interrupt Enable (IE)	Set to allow ERROR or READY = 1 to cause an interrupt. Cleared by INIT. Read/Write.
5-4	Extended Bus Address	Extended bus address bits 17 and 16 that in conjunction with DRBA specify A(17:01) in direct memory transfers. Cleared by INIT. XBA17 & 16 do not increment when DRBA overflows; instead ERROR is set. Read/Write.
3-1	Function 3, 2, 1	Three bits made available to the user device. User defined. Cleared by INIT. Read/Write.
0	Go	Set to cause a pulse to be sent to the user device indicating a command has been issued. Clears READY. Always reads as a zero. Write only.

Data Buffer Register (DRDB) 772 416

The DRDB serves two functions: First, it is a 16-bit write only register. The outputs of this register are available to the user device (refer to the DATA OUT signals). The register can be loaded under program control, but is also used to buffer information when data is being transferred from the UNIBUS to the user device (when DR11-B does a DATI cycle). DRDB is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Second, the DRDB functions as a 16-bit read only register. Information to be read is provided by the user device on the DATA IN signal lines. These lines are not buffered and must be held until either read under program control or transferred directly to memory (DATO bus cycle).

Maintenance Mode

Checkout and test of the DR11-B is accomplished by using a MAINT bit in DRST along with a special maintenance module which simulates the user's device. The maintenance module plugs directly into the two slots normally occupied by the cable boards and jumps the output and input signals. The maintenance module is included with the DR11-B.

SPECIFICATIONS

Usage:		Direct memory access (DMA) data transfer
Input/output levels: (user interface)		logic 1 = +3 V logic 0 = 0 V
Register Addresses		
Word Count	(DRWC)	772 410
Bus Address	(DRBA)	772 412
Status and Command	(DRST)	772 414
Data Buffer	(DRDB)	772 416
2nd DR11-B		772 430 to 772 436
3rd DR11-B		772 450 to 772 456
4th DR11-B		772 470 to 772 476
UNIBUS Interface		
Interrupt vector address:		124 (1st DR11-B) (for other DR11-B's, assigned by user)
Priority level:		BR5
Data transfer:		NPR
Bus loading:		1 bus load
Mounting:		1 System Unit (SU)
Input Current:		3.3 A at + 5 V (no current needed at — 15 V)
Environment		
Operating temperature:		10°C to 50°C
Relative humidity:		20% to 90%

GENERAL DEVICE INTERFACE, DR11-C

DESCRIPTION

The DR11-C is a general-purpose interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions.

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

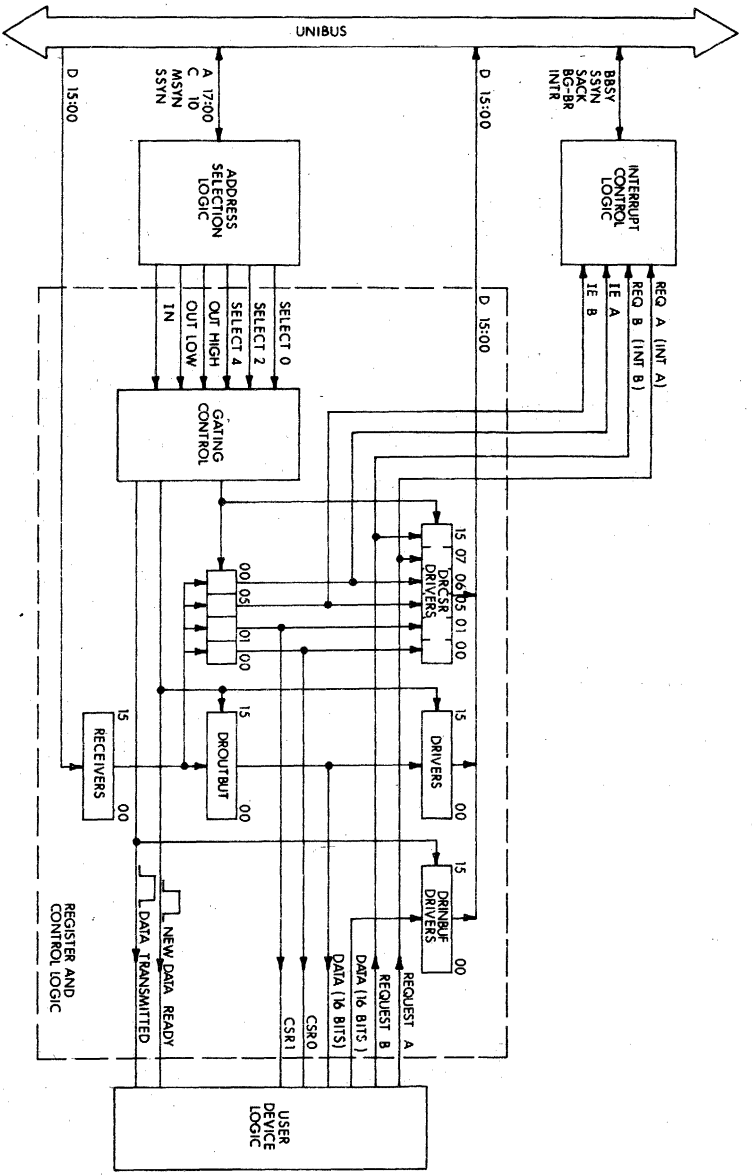
The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, a NEW DATA READY control signal is supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to UNIBUS transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the main-



DR11-C Interface, Block Diagram

tenance mode, they are also used to check operation of the interface.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, thereby permitting the two processors to communicate.

Physical Description

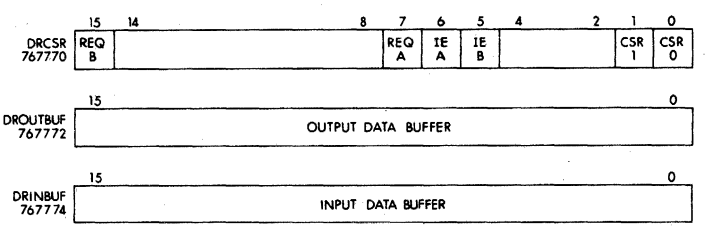
The DR11-C interface is packaged on a single quad module that can be plugged into a small peripheral slot (SPC).

The module has two Berg connectors for all user input/output signals. Two M971 connector boards, which are *not* supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two H856 cables. Note that this cable is a "mirror image" rather than a straight one-to-one cable.

The following accessories are available for interfacing:

a. BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8, 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.
b. M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.
c. BC11K-25 cable. Consists of a 20 twisted-pair cable with a Berg connector on one end only. Available in 25 ft lengths.
d. H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

REGISTERS



The register addresses can be changed by altering the jumpers on the address selection logic. However, any programs or other software re-

ferring to these addresses must also be modified accordingly if the jumpers are changed.

Control and Status Register (DRCSR) 767 770
The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT ENB (interrupt enable) bits which are under program control. Two other bits (CSR0 and CSR1) are controlled from the UNIBUS and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 7 for ready indications and both of these bits can generate interrupt requests. In addition, bit 0 is normally used for start or go commands.

DRCSR Bit Assignments

BIT	NAME	FUNCTION
15	REQUEST B	This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT when in Maintenance Mode.
07	REQUEST A	Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Read-only bit. Cleared by INIT when in Maintenance Mode.

06	INT ENB A	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
05	INT ENB B	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
01	CSR1	This bit can be loaded or read (under program control) from the UNIBUS and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Read/write bit (can be loaded or read by the program). Cleared by INIT.
00	CSR0	Performs the same functions as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.

Output Buffer Register (DROUTBUF) 767 772

The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Information from the bus is loaded into this register under program control. At the time of loading, a pulsed signal (NEW DATA READY) is generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic.

The DROUTBUF is cleared by INIT.

Input Buffer Register (DRINBUF) 767 774

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the UNIBUS. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the UNIBUS for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

Input and Output Signals

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	CC	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS.*	2	C
			CSR0	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

* Pulse signals, approximately 400-ns wide. Width can be changed by user.

Pin Connections

M971		DR11-C				M971	
		Connector No. 2		Connector No. 1			
Board	Berg Header	Pin	Name	Name	Pin	Berg Header	Board
U2	A	VV	OPEN	OPEN	A	VV	A1
U1	B	UU	GND	OPEN	B	UU	A2
V2	C	TT	IN00	OUT00	C	TT	A1
V1	D	SS	GND	OPEN	D	SS	A2
T2	E	RR	INIT H	OPEN	E	RR	B1
T1	F	PP	GND	OPEN	F	PP	B2
T2	H	NN	INIT H	OPEN	H	NN	C1
T1	J	MM	GND	GND	J	MM	C2
S2	K	LL	IN01	OUT01	K	LL	D1
S1	L	KK	IN04	OUT04	L	KK	D2
R2	M	JJ	GND	GND	M	JJ	E1
R1	N	HH	IN05	OUT05	N	HH	E2
P2	P	FF	OPEN	INIT H	P	FF	F1
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	CC	IN07	OUT07	T	CC	H2
M2	U	BB	IN03	OUT03	U	BB	J1
M1	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M1
J1	BB	U	IN12	OUT12	BB	U	M2
H2	CC	T	GND	GND	CC	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
E1	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSR0	REQ A	LL	K	S2
C2	MM	J	GND	GND	MM	J	T1
C1	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	IN02	OUT02	RR	E	T2
A2	SS	D	OPEN	GND	SS	D	V1
A1	TT	C	DATA TRANS.	OPEN	TT	C	V2
A2	UU	B	OPEN	GND	UU	B	U1
A1	VV	A	OPEN	NEW DATA RDY	VV	A	U2

BC11K Connections

Twisted Pair	Color	Pin	Connector No. 1	Connector No. 2
black/white-orange	black	A	OPEN	OPEN
	wh-org	B	OPEN	OPEN
black/white-yellow	black	C	OUT00	DATA TRANS.
	wh-yel	D	OPEN	OPEN
black/white-grey	black	E	OPEN	IN02
	wh-gry	F	OPEN	OPEN
black/white-red	black	H	OPEN	IN02
	wh-red	J	GND	GND
black/white-green	black	K	OUT01	CSR0
	wh-grn	L	OUT04	GND
brown/green	brown	M	GND	IN15
	green	P	INIT	IN13
brown/red	brown	N	OUT05	IN14
	red	R	OUT06	GND
black/white-blue	black	S	GND	REQ B
	wh-blu	T	OUT07	GND
black/orange	black	U	OUT03	IN12
	orange	V	GND	IN11
black/white-violet	black	W	OUT08	IN10
	wh-vio	X	OUT09	GND
black/red	black	Y	GND	IN09
	red	Z	OUT10	IN08
brown/yellow	brown	AA	OUT11	GND
	yellow	BB	OUT12	IN03
black/blue	black	CC	GND	IN07
	blue	DD	CSR1	GND
brown/orange	brown	EE	GND	IN06
	orange	FF	OUT13	OPEN
brown/blue	brown	HH	OUT14	IN05
	blue	JJ	OUT15	GND
black/yellow	black	KK	GND	IN04
	yellow	LL	REQ A	IN01
brown/violet	brown	MM	GND	GND
	violet	NN	OUT02	INIT

black/violet	black	PP	GND	GND
	violet	RR	OUT02	INIT
black/green	black	SS	GND	GND
	green	TT	OPEN	IN00
pink/white-red	pink	UU	GND	GND
	wh-red	VV	NEWDATA RDY	OPEN

SPECIFICATIONS

Usage: Priority interrupt interface control

Input/output levels: (user interface)
logic 1 = +3 V
logic 0 = 0 V

Register Addresses

Control and Status (DRCSR)	767 770
Output Buffer (DROUTBUF)	767 772
Input Buffer (DRINBUF)	767 774
2nd DR11-C	767 760 to 767 764
3rd DR11-C	767 750 to 767 754
4th DR11-C	(etc) (etc)

UNIBUS Interface

Interrupt vector addresses:	floating (see Appendix A) (2 needed for each DR11-C)
Priority level:	BR5 (may be changed)
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot
Size:	quad module

Input Current: 1.5A at +5V
(no current needed at −15V)

Environment

Operating temperature:	10°C to 50°C
Relative humidity:	20% to 90%

Miscellaneous:

Inputs: One standard TTL unit load; diode protection clamps to ground and +5V

Outputs: TTL levels capable of driving 8 unit loads except for the following:

NEW DATA READY = 30 unit loads

DATA TRANSMITTED = 30 unit loads

INIT (initialize) = common signal on both connectors driven by one 30-unit load driver

Signals:	NEW DATA READY—drives 30 units, positive pulse, 400-ns wide unless width changed by an external capacitor
	DATA TRANSMITTED—drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor
	INIT (initialize)—common signal on both connectors driven by one 30-unit load driver
Data Inputs:	16-bit word from the external device
Data Outputs:	16-bit word from the UNIBUS. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.
Maintenance Mode:	A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 7 to read as CSR1 and CSR0, respectively.

UNIBUS SWITCH, DT03-F

The DT03-F UNIBUS Switch is an electronic switch that allows a single peripheral or a group of peripherals to be switched from one processor to another. It provides on-line system back-up and dynamic reconfiguration for systems where very high reliability is required.

The UNIBUS Switch implements a switched or "common" bus that can be selectively connected to the UNIBUS of any processor in a multiprocessor system. Any device or devices except a processor may be connected to this common bus. When the switch is connected to a particular processor's UNIBUS, all peripherals and memory on the common bus operate just as though they were permanently connected to that bus. When the switch is disconnected, all peripherals on the common bus are removed from that UNIBUS and are available for connection to any other processor's UNIBUS. Once switched to a particular UNIBUS, the Bus Switch is transparent to the processor program. The switch is engineered to preserve the transmission properties of all busses attached to it regardless of the switch's position. Even during on-line switching all busses are synchronized to prevent interfering with individual programs. In order to guarantee bus operations, the switching elements are electronic circuits that receive and regenerate all bus signals passing through the switch. These electronic circuits not only eliminate impedance-mismatch and crosstalk problems, but also provide the long-term reliability inherent in solid-state circuits.

The bus switch is available in two versions:
DT03-FP—Both programmable and manual control
DT03-FM—Manual control only

Both models are constructed from modular sections, each of which is analogous to a multi-pole, single-throw switch that connects the shared bus to one processor bus at a time. The module consists of a UNIBUS isolation circuit, a bus repeater, bus-synchronization logic, and, in the case of the -FP version, a programmable controller.

Each DT03-F section (a DT03-F has one section for each processor that can attach to the common bus) has two switch positions: Connected and Neutral, defined as follows:

Connected: In this position the switched bus is connected directly to the processor associated with that section, and all of the devices on the switched bus are available to that processor. Only one section of a switch can be in the connected position at a time (i.e., the common bus can only be used by one processor at a time).

Neutral: In this position the switched bus is not connected to the processor. When the switches in all sections are in the neutral position, devices on the switched bus can then be serviced or repaired without disturbing operations on any processor busses.

In the manual-control mode, the operator can select either local- or remote-command inputs to the DT03-F. Local control is derived from a

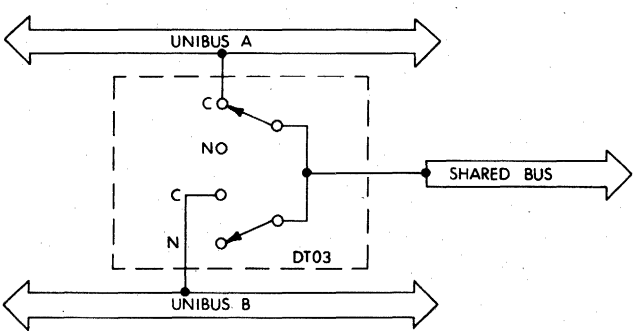
toggle switch that either enables or disables the bus signal-flow through the switch section. In the remote mode, the DT03-F position can be manually controlled via signal wires from a distant location.

The FP version includes a programmable control that allows switch operation under processor control.

In both manual and programmable modes, the bus synchronizer assures that the switch changes position without interfering with any operations on the processor bus, i.e., the switch can be thrown while a program is running. If two or more processors request use of the shared bus simultaneously, a priority-arbitration circuit within the switch specifies which processor will be serviced first. The priority-arbitration circuit assures that no more than one processor at a time is connected to the shared bus.

All DT03-F's include circuitry to isolate the switch itself from the processor buses in the event that either the switch power supply is de-energized or a peripheral-device power supply is de-energized on the shared bus. When the supply is off, a relay disconnects the + 5 V and ground lines between the supply and the logic modules. The UNIBUS interface circuits are held in a high-impedance state that will not load down the processor busses. At the same time, another set of relays close and provide an alternate path to preserve continuity of the bus grant signals on each processor bus. The DT03-F logic panel can then be serviced without interfering with program operation.

An important feature of the bus switch in high-reliability applications is the ability to disconnect itself from a processor that is no longer operational. The DT03-FP contains a "watch-dog" timer that monitors the processor currently using the switch. If that processor does not reset the timer within the allotted interval (thereby indicating that the processor has halted or is executing an invalid program), the switch automatically disconnects. Similarly, a power failure in the system to which the common bus is connected automatically disconnects the switch. A back-up processor can then assume control of the switch and proceed to operate the devices on the shared bus.



Equivalent Circuit of DT03

PROGRAMMING

The DT03-FP has associated with it two programmable registers (one for each CPU), the Control and Status Registers, and one interrupt vector for each processor connected to it. The bits of the Control and Status Registers are defined as follows:

BIT	NAME	FUNCTION
15	Watch-Dog Timer Overflow	Set to indicate that the processor failed to clear the Common Bus Requested bit (bit 12) within 10 milliseconds. The common bus is automatically disconnected. Causes an interrupt if Interrupt Enable (bit 6) is set.
14	Power Failure	Set to indicate a power failure on the shared bus or in the switch itself. Setting of this bit also triggers a power-fail interrupt in the processor connected to this switch section and isolates the switch from the processor bus, thereby allowing the processor to restart.
13	Bus Active	Set to indicate that the shared bus is already connected to a processor.
12	Common Bus Requested	Set to indicate that some other processor wants to use the common bus, i.e., it has set its own Request bit (bit 0). Causes an interrupt if Interrupt Enable (bit 6) is set and also starts the watch-dog timer. (Clearing this bit stops the watch-dog timer.)
11		Not used.
10		Not used.
9	Reset	Set to send an initialize pulse to all devices on the common bus.
8		Not used.
7	Common Bus Connected	Set to indicate that the processor has been connected to the common bus. Causes an interrupt if Interrupt Enable (bit 6) is set.
6	Interrupt Enabled	Set by the processor to allow interrupts under the following conditions: 1. Common bus connected (bit 7) 2. Common bus requested (bit 12) 3. Watch-dog timer overflow (bit 15) 4. Connect request failed (see bit 0)
5—1		Not used.
0	Request Common Bus	Set to request connection to the common bus. If the common bus is not in use, the switch will connect the processor to it immediately. If the shared bus is in use, the Common Bus Requested bit (bit 12) is set for the processor connected to the common bus and the watch-dog timer is started for that processor. At the same time, a Request Timer in this DT03-F section is started. If the

processor using the shared bus does not relinquish the bus within the timer interval, the Request bit will be cleared and an interrupt will occur (if Interrupt Enable, bit 6, is set). If the other processor does release the shared bus in time, this DT03-FA will connect and will set the Connected bit (bit 7).
The Request bit can be cleared by the processor to disconnect itself from the shared bus.

SPECIFICATIONS

Option Designations	DT03-FP UNIBUS Switch (Programmable and Manual Control). DT03-FM UNIBUS Switch (Manual Control Only).
Interrupt Vector	Requires one vector assigned from either the User Reserved Vectors (170, 174, 270, 274) or from the Floating Vector Field.
Priority Level	BR7
Switching Time	Less than one microsecond; busses automatically synchronized.
Watch-dog Timer	Interval set to approximately 10 milliseconds.
Latency	Bus cycles that go through the switch (i.e., between a switched and a non-switched peripheral) are extended 450 nanoseconds.
Bus Loading	Each DT03-F module places a one-unit load on its processor UNIBUS and on the shared UNIBUS.
Power Supply	Power supply is mounted on rear door of cabinet. Relay power isolation when de-energized.
AC Power	115/230 V, 50/60 Hz, 2 A.
Installation	Each DT03-F section is constructed on a standard 5¼ x 19-inch rack-mountable logic panel.
UNIBUS Compatibility	Can be used with any PDP-11 Family processor. (When used with the PDP-11/20, the KH11-A Large-System Capability Option must be installed in the processor).

GRAPHIC DISPLAY SYSTEM, GT40

DESCRIPTION

The GT40 is a low-cost, high-performance graphic display system which operates through a powerful general-purpose computer. The GT40 is designed for applications which require both visualization and computation. The system can display either alphanumeric information or graphic information such as drawings, diagrams, or patterns. It is especially valuable for displaying dynamic, fast changing information such as wave forms. Designs and layouts can be plotted in minutes instead of hours, then instantly modified using the light pen. Designers are free to concentrate on layout while the system handles the calculations. And, the computer can easily monitor a check list to make sure every detail is included.

System

The GT40 is a multipurpose system. It is a graphic display system which

operates through a sophisticated terminal connected to a PDP-11 minicomputer. When not engaged in graphics tasks, it is a general-purpose computer which can operate as a stand-alone system or initiate dialogue with a central computer as part of a computer network.

The GT40 consists of seven parts: central processor, display processor, light pen, keyboard, communications interface, memory, and bootstrap read-only memory.

The central processor is a 16-bit processor with standard PDP-11 instruction set capability and 8K words of memory. Because the GT40 has its own programmable, general-purpose processor, expansion to keep pace with increased needs and changing requirements is always possible.

For example, the GT40 can be programmed to simulate any alphanumeric or graphic terminal. A programmable terminal also permits the use of different line protocol and allows different interfacing requirements to be satisfied. The PDP-11 UNIBUS makes interfacing easy because the diversity of inexpensive peripheral and communications options simply plug in. All of the peripheral equipment available for use on PDP-11 family computers can be used by the GT40. As the system grows, it is only necessary to modify the software to meet almost any change.

The display processor performs the most popular graphic techniques quickly in hardware with minimum central processor overhead. The heart of the GT40, it fetches data and commands from memory, interprets and executes these commands, and performs all vector and character calculations. The display processor consists of the UNIBUS control, the data and instruction processor, the vector generator, the character generator and CRT monitor. A solid-state light pen is provided to facilitate interaction with the system.

The keyboard is free-standing, full-ASCII encoded with serial output coupling directly into the central processor. Character capability includes ASCII upper and lower case with italics and special characters. A separate eight-key function pad is located adjacent to the operator's keyboard for convenience in entering instructions.

The communications interface is a flexible, serial, asynchronous interface with both EIA level and 20 milliampere current loop output capability for unrestricted intercomputer dialogue and data flow. It also has multibaud rates and separate transmit and receive timing.

The 8K memory is supplemented by a 256-word read-only memory which contains the programming required to read in a program or initiate dialogue with a timesharing computer.

Operation

Because the GT40 uses digital techniques, it is a stable system which requires only minimum adjustments. The vector function operates through a combination of digital and analog techniques, providing a good compromise of speed and accuracy and assuring a precise digital vector

calculation. The presentation and accumulation of vectors mean that every point of the vector is available in digital form.

During plotting, the end-point position is automatically and accurately held, preventing accumulated errors or drift. The vectors are of near constant velocity and are time-efficient regardless of length. Four different vectors—solid, long dash, short dash, and dot/dash—are available in hardware. The smooth ramp deflection signal permits fast vectoring with moderate deflection of band width and power.

The GT40 character generator has both upper and lower case capability with a complete repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous image with excellent contrast ratio is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock in the display permits the GT40 to be synchronized to line frequency of 60 Hz. Scope resolution is precise enough to allow overprinting.

The terminal includes logic for descender characters such as "p" and "g", positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes. These include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Eight intensity levels permit varying the brightness and contrast so that the scope can be viewed even in a normally lighted room.

The instruction set consists of four control-state instructions and five data-state formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of five different formats, allowing multiple tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the GT40 automatically plots the X or Y axis according to preset distances as values for the opposite axis are recorded.

SPECIFICATIONS

CRT

Viewable Area	6.75" x 9"
Brightness	> 30 foot lamberts
Contrast Ratio	> 10:1
Spot Size	20 mils at 30 foot lamberts (FWHM)
Phosphor	P39 (medium-long persistence)
Pincushion	± 1% of full scale to best fit line

DISPLAY CONTROLLER

General

Resolution	10 bits (1024 words x 1024 words)

Viewable Size	1024 words horizontal, 768 words vertical
Paper Size	12 bits (4096 words)
Hardware Blink	Programmable
8 Intensity Levels	Programmable
Line Frequency Synchronization	Programmable
Characters	
Font	6 by 8 dot matrix
Characters/Line	72
Lines/Frame	31
Character Set	96 ASCII—upper and lower case, 31 special symbols (Greek letters, math symbols, etc.)
	Italics for the above printing characters (programmable)
Control Characters	Carriage return, line feed, backspace & bell
Vectors	
Relative Vectors	Just give $\triangle$ X and $\triangle$ Y of the move
Arbitrary Vectors	Can draw at any angle on the screen
Vector Writing Rate	$\backsim$ 200 μs for full-screen vector (min)
Vector Types	4—solid, long dash, short dash, dot/dash—all programmable
Points	
Point Plotting Rate	$\backsim$ 20 μs/point
GENERAL INFORMATION	
Word Length	16 bits
CPU Instruction	Entire PDP-11/10 Instruction Set
Display Processor Instruction	Set Graphic Modes (3 registers) Jump No-op
Data Formats	Character (2 char/word) Short Vector (1 word) Long Vector (2 words) Point Mode (2 words) Relative Point Mode (1 word) Graph Plot X, Y (1 word/point)
Keyboard	Full ASCII keyboard with separate function keys
Light Pen	Solid-state light pen
Communication Controller	Asynchronous dialogue
	Separate RECEIVE and TRANSMIT speeds up to 9600 baud
	Capable of driving EIA data leads, with full data set control

SPECIFICATIONS

Mechanical

Mounting:	table top unit
Size:	18"H x 20"W x 24"D
Weight:	150 lbs.

Power

Input current:	15 A at 115 VAC
Heat dissipation:	1500 W

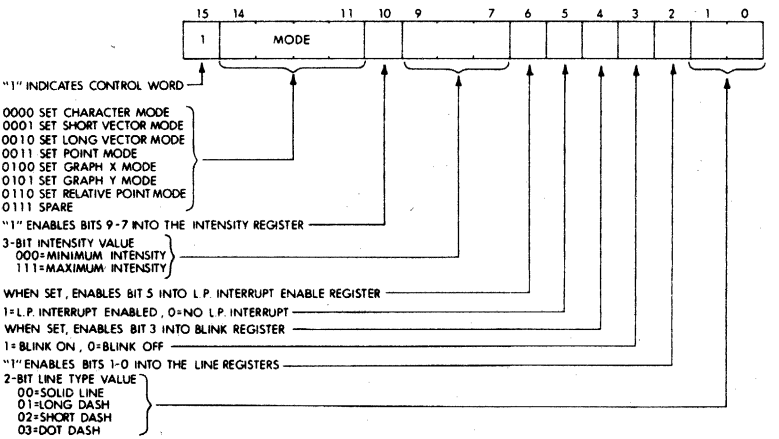
Environment

Operating temperature:	15°C to 35°C
Relative humidity:	20% to 80%

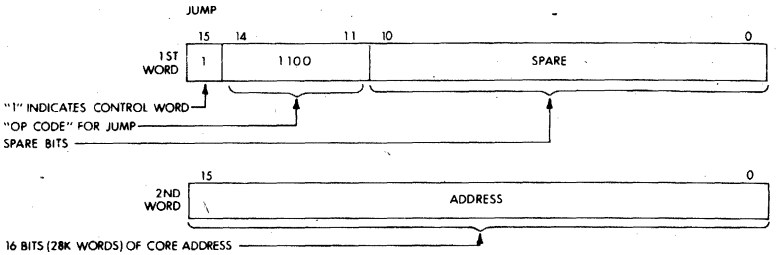
GT40 INSTRUCTION SET

The basic instruction set for the GT40—Set Graphic Modes, Jump, No-Op, and Load Status Registers—is simple, concise, and powerful. It is augmented by the versatility of the PDP-11 CPU instructions which are executable by the GT40.

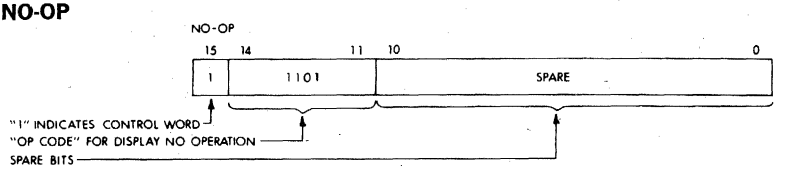
SET GRAPHIC MODE



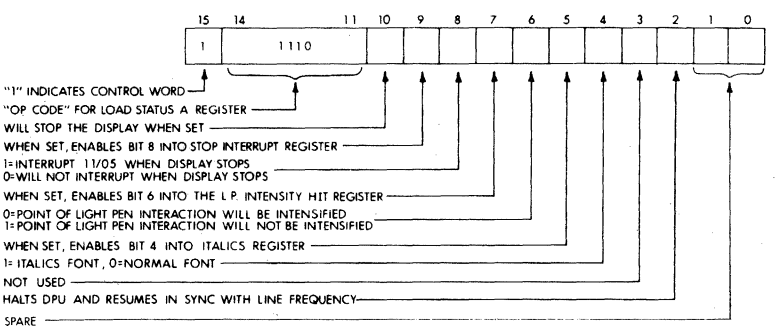
JUMP



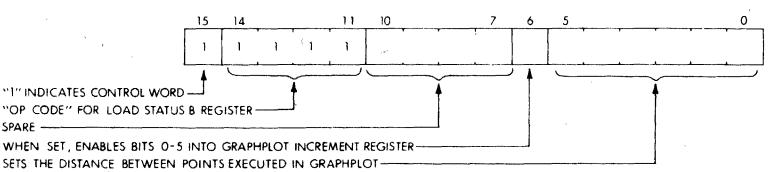
NO-OP



LOAD STATUS REGISTER A



LOAD STATUS REGISTER B

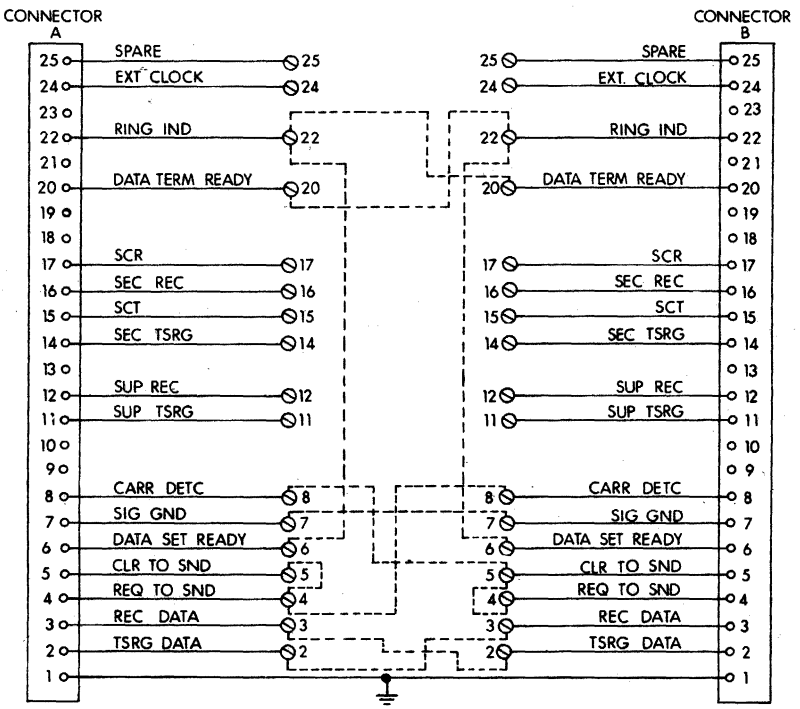


ASYNCHRONOUS NULL MODEM, H312-A

ASYNCHRONOUS NULL MODEM, H312-A

The H312 null modem allows a user to connect a terminal device to a computer without the use of two modems as would be normally required. It consists of two female 25-pin data-phone sockets mounted on a printed circuit board with the 15 most commonly used wires brought out to split lugs in the center of the board. The split lug allows the user to interconnect the two sockets in any way he wishes as long as the pins used are on the split lug interconnection points.

The H312 is wired (as shown below) to simulate back-to-back Bell 103A's. However, the user may make wiring modifications.

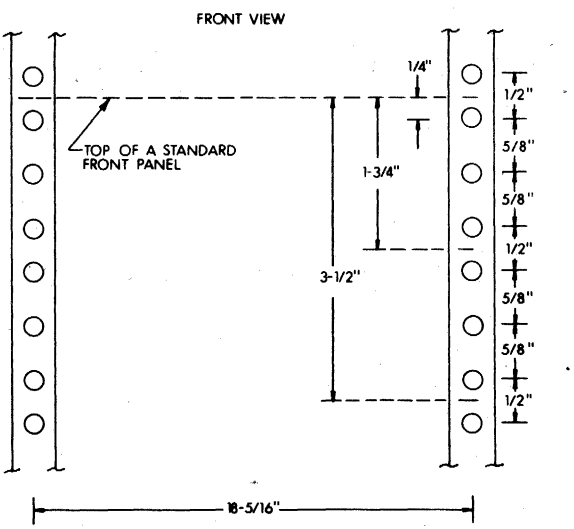


STANDARD PDP-11 CABINETS, H960 & H961

Cabinets
The standard PDP-11 cabinet is 72" high by 21" wide by 30" deep. It has mounting space for six 10½" front panel units of equipment. Each cabinet contains a power control and switched AC outlets so that all equipment within the cabinet (and other connected cabinets) can have their power turned on and off together.

The cabinet can mount standard 19" wide equipment, and has two rows of mounting holes in the front, spaced 18 5/16" apart. The holes are located at ½" or ⅝" apart from each other, see the following diagram. Standard front panel increments are 1¾".

$$(\tfrac{5}{8} + \tfrac{5}{8} + \tfrac{1}{2} = 1\tfrac{3}{4})$$



Standard PDP-11 Cabinet

H960-CA & H961-A
The H960-CA is a basic PDP-11 cabinet with power control, fans, extension feet, but no power supplies. The H961-A is the same as the H960-CA, except it does not have side panels. It is used as the second, third, or higher cabinet in a multi-cabinet system that is tied together (only 1 set of side panels are needed).

H960-D

The H960-D cabinet has a sliding extension mounting box drawer which fits in the lower half of the cabinet. The sliding drawer provides mounting space for 9 System Units (SU). Power supplies are provided to furnish a total of:

75 amps at +5 V
20 amps at −15 V
1 amp at +15 V

The component parts are:

H742	1 amp at +15 V	Power supply with room for 5 regulators; includes input transformer and mechanical housing.
H744	25 amps at +5 V	+5 V regulator (3 per H960-D)
H745	10 amps at −15 V	−15 V regulator (2 per H960-D)

H960-E

The H960-E cabinet has two sliding extension mounting box drawers, and has mounting space for 18 System Units. The included power supplies provide twice the power capability of the H960-D, divided evenly between the two sliding drawers.

SPECIFICATIONS

Size:	72"H x 21"W x 30"D
Weight:	120 lbs (H960-C) 300 (H960-D) 470 (H960-E)

Models:

H960-CA:	Cabinet with side panels
H961-A:	Cabinet without side panels
H960-DA:	Cabinet with sliding drawer and power supplies, 115 VAC, 60 Hz
H960-DB:	Cabinet with sliding drawer and power supplies, 230 VAC, 50 Hz
H960-EA:	Cab with 2 sliding drawers and power supplies, 115 VAC, 60 Hz
H960-EB:	Cab with 2 sliding drawers and power supplies, 230 VAC, 50 Hz

COMMUNICATIONS ARITHMETIC OPTION, KG11-A

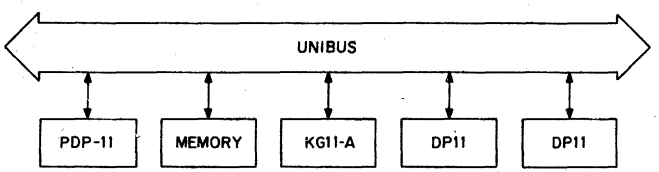
FEATURES

- Computes three different Cyclic Redundancy Check (CRC) polynomials and two Longitudinal Redundancy Checks (LRC)—CRC-16, CRC-12, CRC-CCITT, LRC-8, LRC-16
- Program selection of desired polynomial
- Fits in small peripheral slot
- Computes an 80-character message block in less than 100 microseconds

DESCRIPTION

The KG11-A is attached to the UNIBUS and is used to compute a Cyclic Redundancy Check (CRC) or Longitudinal Redundancy Check (LRC) for detecting errors in serially transmitted data. It is used with a DP11 serial synchronous line interface to compute the Block Check Character(s) (BCC) appearing at the end of a block of data transmitted over a serial synchronous line.

A typical configuration might be:



For received data, the characters are moved to the KG11-A and a BCC is computed for the data and compared to the BCC received. If they are equal, the data is assumed to be correct and is accepted. If they do not match, the message is not accepted and the data is retransmitted.

When data is being transmitted, the BCC is generated by moving all the characters to the KG11-A. The resulting BCC is transmitted at the end of the message.

* Not all characters are included in the BCC. The exclusions will depend on the line protocol used.

The KG11-A, under program control, can compute the most popular CRC and LRC polynomials:

1. CRC-16 $X^{16} + X^{15} + X^2 + 1$
2. CRC-12 $X^{12} + X^{11} + X^3 + X^2 + X + 1$
3. CRC-CCITT $X^{16} + X^{12} + X^5 + 1$
4. LRC-8 $X^8 + 1$
5. LRC-16 $X^{16} + 1$

CRC-16

CRC-16 is used for synchronous systems that employ 8-bit characters. It is used in IBM binary synchronous systems when the transmission code is EBCDIC or 8-bit transparency. For IBM compatible systems, the message format is:

1

```
  S          Ebb
(1)T—text—Tcc
  X          Bcc
```

2

```
  S          Ebb
(2)T—text—Tcc
  X          Xcc
```

```
  S          I bb          Ebb
(3)T—text—Tcc —text—Tcc
  X          Bcc           Bcc
```

3

```
  S          I bb          Ebb
(4)T—text—Tcc —text—Tcc
  X          Bcc           Xcc
```

4

In the preceding examples, each character represents an 8-bit character. The first BCC character is the least significant 8 bits of the BCC computed in the KG11-A. The STX is not included in the BCC. The BCC includes the first text character through the ETB, ITB or ETX. In examples (3) and (4), the second BCC begins with the character following the first BCC in the block (even if it is an STX or DLE). The examples are for normal transmission. For transparent transmission, the characters indicated by (*) in the following example are not included in the BCC.

```
␣  ␣  ␣  ␣
** *  *  *
DS DD D I b b¹ D S     D E b b
LT—text—LL —text—L T c c L T—text—L T c c
EX EE   E B c c E X     E X c c
```

¹ At this point, a new BCC sequence is begun which includes initialization of the BCC registers.

The DLE DLE indicates that the second DLE is really data and not the control character and is, therefore, included in the BCC. It may appear in text as often as that 8-bit representation is required. Because the DLE ITB sequence takes the system out of the transparent mode, the DLE STX following the BCC is included in the next BCC and also puts the system back into the transparent mode.

CRC-12

CRC-12 is used for six-bit characters. It is compatible with IBM Binary Synchronous Communications (BSC) when the transmission code used is Six-Bit Transcode. The characters included in or excluded from the BCC are the same as for CRC-16. The difference is only in the length of character (6 versus 8 bits).

CRC-CCITT

CRC-CCITT is the standard polynomial used to compute BCC for European systems. The characters included or excluded will depend on the line protocol used for the system in which the KG11-A is used.

LRC-8
Some systems use only an 8-bit LRC on the characters. LRC-8 performs an exclusive OR on an 8-bit or less character. The LRC is usually used in combination with a Vertical Redundancy Check (VRC). VRC is possible only when the characters are 7-bit or less plus one parity bit. LRC/VRC is used for IBM BSC when the transmission code is USACII. For IBM systems, the parity bit makes the character contain an odd number of bits.

LRC-16
LRC-16 performs an exclusive OR on a 16-bit or less character. It can be used to perform a word exclusive OR, or to compute LRC for 10, 11 and 12 bit characters transmitted via a DP11 with the DP11-CA option.

KG11-A Programming Techniques—Recommended Practice
There are two ways to use the KG11-A: Message Basis and Character by Character (Partial BCC). It is recommended that the KG11-A be used to compute on a message basis. The BCC register is Write Only. Therefore, a partial BCC has to be loaded through the data register in the LRC-16 mode. To do a partial polynomial computation (character by character), for example, a character is added to the accumulation as it is received. This can be done efficiently for one line (half duplex) because the BCC can be left in the KG11-A until all the characters have been processed. However, for full duplex and/or multiple lines, the BCC accumulation cannot be left in the KG11-A because it may have to be used for another line before the next character appears. Therefore, the partial BCC has to be saved and reloaded when the next character appears. The following sequence is required to load a partial BCC, add a character, and store the new partial BCC:

1. Set mode to LRC-16 and clear BCC
2. Load the partial BCC
3. Test DONE flag
4. Set mode to proper polynomial (don't clear BCC)
5. Load character
6. Test DONE flag*
7. Store partial BCC

* Depending on which PDP-11 processor is used, these tests may not be required for single-byte operations because the KG11-A completes the operation in one microsecond. For word operations, the maximum cycle time of the KG11-A is 2 μsec. The KG11-A does not generate an interrupt so, if a programmer wants confirmation, he must test the DONE bit.

It is recommended that the message be passed through the KG11-A in one continuous loop operation after the entire message is received or prior to commencing transmission. If this method is undesirable, multiple KG11's can be used. For full duplex, two KG11-A's can be used, one for each direction. Addresses for eight KG11-A's have been allocated.

Figure 1 is a flow chart of the recommended practice (complete BCC). The numbers in parenthesis represent the KG11-A operations.

* Not required but may be used (see description).

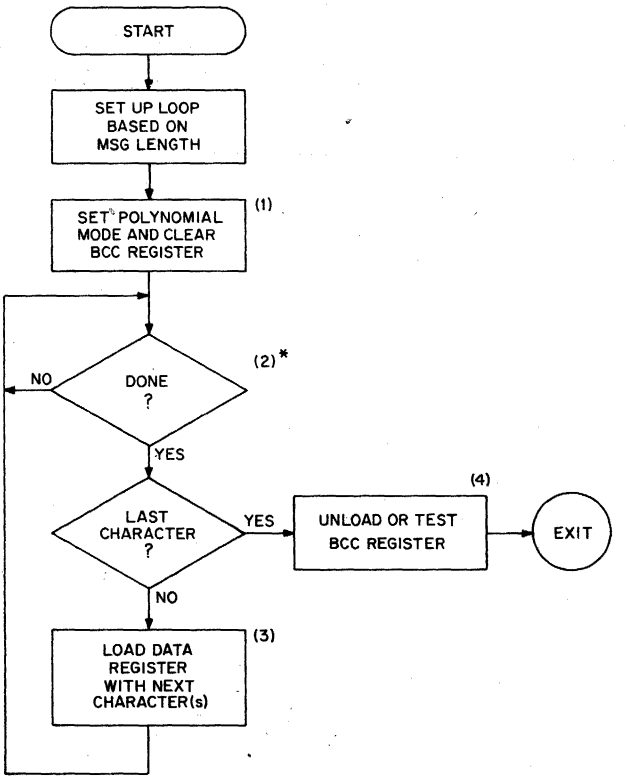


Figure 1

KG11-A Programming
Registers

The KG11-A consists of these three registers:

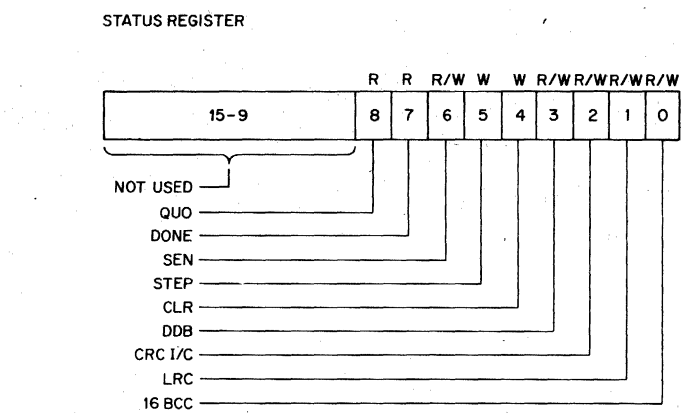
Address	Description
7707x0	Status register
7707x2	BCC register
7707x4	Data register

Where x = 0-7, assignments for 8 KG11-A's.

Status Register—This is a 16-bit register used to control (set mode) and to present status. Some bits are Read Only (QUO, DONE), some are Write Only (STEP, CLR) and the rest are Read/Write. Figure 2 describes the status register.

BCC Register—This is the result register and is Read Only. The format of this register will be described later for each KG11-A operational mode.

Data Register—This is a 16-bit Write Only register. It is used as the input register for the data on which the BCC is calculated. The format of the input data will be described later for each KG11-A operational mode.



R = Read Only
W = Write Only (ONES)
R/W = Read/Write

Figure 2

Initialize KG11-A ((1) in Figure 1)
The initialization procedure consists of moving a command word to the Status Register that selects the desired polynomial, indicates whether bytes or words will be presented for accumulation, indicates whether the unit is to cycle or be single stepped and clears the BCC register.

Select the Desired Polynomial
The polynomial is selected by a combination of bits 2, 1, 0 (CRCI/C, LRC, 16 BCC respectively) of the Status Register. The bit selection is as follows:

Polynomial	STATUS BIT 2 CRC I/C	1 LRC	0 16 BCC
1. CRC-12	0	0	0
2. CRC-16	0	0	1
3. LRC-8	0	1	0
4. LRC-16	0	1	
5. Undefined*	1	0	0
6. CRC-CCITT	1	0	
7. Undefined*	1	1	0
8. Undefined*	1	1	1

* The "undefined" polynomials mean the combinations will have undefined results.

Indicate Word or Byte Operation (DDB)

The purpose of this indicator is to tell the KG11-A if the data register will be loaded each time with a word (16 bits) or a byte (8 bits). Bit 3 (DDB) selects word (DDB = 1) or byte (DDB = 0). Even if characters are being accumulated, the program loop (Figure 1) is shorter if the characters can be presented two-at-a-time (WORD option).

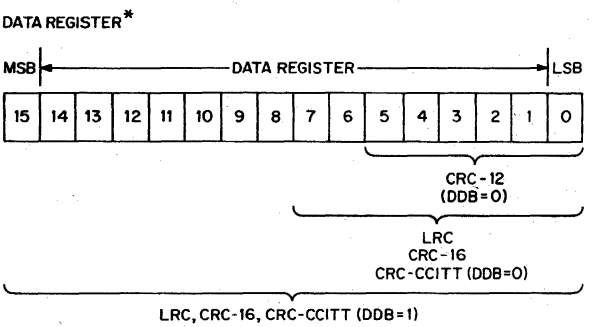
Caution:
CRC computations are correct only if the characters are presented to the KG11-A in the order in which they are put on or received from the communications line. If the messages are formed (received) in byte mode, then a word move can be made to the Data Register. In other words, the message must be stored in memory in ascending order of byte address. Figure 3 shows the order of characters on the basis of words moved to the KG11-A.

Character Order

Relative Word Address		
0	2	1
2	4	3
4	6	5
6	8	7
.	.	.
.	.	.
.	.	.
.	.	.

Figure 3

The position of the data for the KG11-A option is given in Figure 4. Note that if CRC-12 is selected, double mode (DDB = 1) produces undefined results.



* Write Only
MSB Most Significant Bit
LSB Least Significant Bit
CRC-12 (DDB 1) is not supported

Figure 4

Cycle or Single-Step Mode
For diagnostic purposes, the unit can be single stepped and the operation can be monitored at each step. For normal operation, a complete cycle can be initiated. The two states are set up as follows:

Operation	Status Bits	
	SEN	STEP
Cycle	1	Ignored
Single Step	0	1

Cycle Mode
Once the status register is initialized with SEN = 1, the KG11-A will perform a complete cycle each time the data register is loaded as specified in Figure 4. Once the data register is loaded, the DONE flag is inactivated until all shifting ceases and the new BCC is in the BCC Register. Elapsed time is 2 μsec (max) for 16 data bits and 1 μsec (max) for 8 or less data bits. The programmer can test the DONE flag (there is no interrupt unless requested) but it is not necessary for proper operation of the KG11-A.

Step Mode
The STEP bit is a gate, not a flip-flop. Each time it is set by a Bit Set instruction, the KG11-A performs one shift and exclusive OR.

The programmer can monitor the operation by examining the contents of the BCC register after each step and by testing the QUO bit (8) in the status register. The QUO bit is the result of the exclusive OR of the LSB Data Bit shifted out of the data register and the LSB Data Bit shifted out of the BCC register. This value is fed back and an exclusive OR is performed with bits in the BCC register as specified by the polynomial. By examining QUO and the BCC register, the programmer can determine whether the KG11-A is functioning properly.

Initialize BCC Register
To begin a new BCC accumulation, the BCC Register has to be cleared to zero. This can be done under program control by setting the CLR bit (4) at the same time (or independently) the polynomial is selected. CLR is a gate and the BCC register is reset each time CLR is set by the program.

Test for KG11-A Completion ((2) in Figure 1)
When the BCC register is cleared or a KG11-A cycle is complete, the DONE flag is set. When it is set, the contents of the BCC register can be used, or the data register can be loaded with the next character, pair of characters or word. On the flow chart (Figure 2), the DONE flag is set the first time because of the initialization in (1). Each time thereafter, it is set because a new character has been loaded into the data register and is added to the BCC accumulation.

If the programmer wishes, he does not have to test the DONE flag before proceeding. The KG11-A is fast enough to complete its cycle while the program is testing to see if there are more characters to accumulate.* The DONE flag is provided for testing purposes in case of malfunctions of the KG11-A.

* This may not be true for all PDP-11 processors.

Load Data Register With Next Character(s) ((3) in Figure 1)
The manner used to load the data register depends on the polynomial and the DDB flag. Figure 4 shows the bits that have to be loaded for each operation.

Once initialized, the act of loading the data register by a MOV(B) instruction initiates a cycle that results in the data being processed and added to the BCC accumulation in the BCC register. When shifting starts, DONE is cleared. When the shifting is complete, the data register is clear and DONE is set.

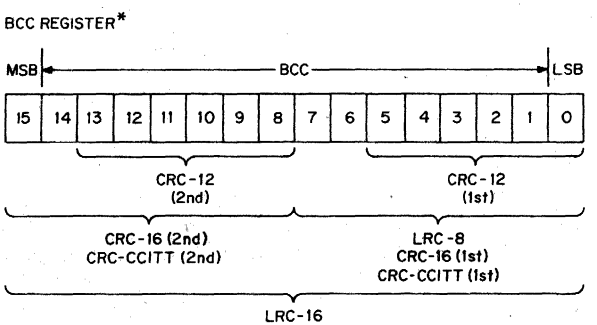
Note: The data is to be right justified in the data register. If double byte mode is used, the leading character is to be in the right byte and the trailing character in the left byte. The Data Register operation assumes the least significant bit of each byte to be to the right (low bit number of the register).

Unload BCC Register ((4) in Figure 1)
Once the CRC (or LRC) has been performed on the message, it is ready to use. If the value is the BCC of a received message, the value can be compared to the received BCC characters. In this case, the value does not have to be moved out of the register to perform the comparison. Alternatively, the received BCC may be included in the accumulation. A good BCC will result in a zero accumulation.**

** When ITB is used, the BCC that follows can be included in the accumulation. The results should be zero. If the rest of the message is accumulated without testing for zero, the only way the final BCC (after ETB or ETX) can compare is if the intermediate BCC's caused the accumulation to go to zero. This method will reduce the operations on the KG11 because the BCC does not have to be reset after the ITB, and only one loop has to be set up.

If the BCC is for a message to be transmitted, the contents of the BCC register can be moved to the message buffer for subsequent transmittal.

The format of the data in the BCC register is different for each polynomial type. The formats are displayed in Figure 5.



* Read Only

Figure 5

Applications

The KG11-A can be used in any application where error detection and correction of serially encoded data are required. The source can be conventional communication channels, paper tapes or magnetic tape recording provided the required CRC or LRC polynomial is one of the options of the KG11-A.

Configurations

The number of KG11-A's required on a system will depend upon the number of messages requiring concurrent calculation of block check characters. When used in conjuntion with the DP11, the following number of KG11-A's is recommended:

Number of DP11's at 3KB	Number of KG11-A's	
	FULL DUPLEX	HALF DUPLEX
1-4	1	1
5-8	2	1

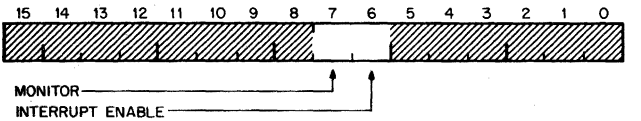
LINE TIME CLOCK, KW11-L

DESCRIPTION

The KW11-L Clock divides time into intervals, 16-2/3 msec or 20 msec, determined by the line frequency, 60 Hz or 50 Hz. The accuracy of the clock period is that of the frequency source.

There are two modes of operation:
Interrupt Mode—An interrupt is generated for each cycle of the line frequency.
Non-Interrupt Mode—The program checks a Monitor bit for timing information.

Clock Status Register (LKS) 777 546



Effect of the Initialize (INIT) signal: clear bit 16, set bit 7.

BIT	NAME	FUNCTION
7	Monitor	Set by the line frequency clock signal and cleared by the program.
6	Interrupt Enable	Set to allow Monitor = 1 to cause an interrupt. Determines mode of operation; 1 = interrupt, 0 = non-interrupt.

SPECIFICATIONS

Main Specifications

Time intervals:	16-2/3 msec at 60 Hz line frequency 20 msec at 50 Hz
Operating modes:	Interrupt Non-Interrupt
Register Address (LKS)	777 546

UNIBUS Interface

Interrupt vector address:	100
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	(Within main CPU assembly)
Size:	1 single height module
Power	0.8 A at +5 V

PROGRAMMABLE REAL-TIME CLOCK, KW11-P

FEATURES

- Four clock rates, program selectable
- Crystal-controlled clock for accuracy
- Two external inputs
- Three modes of operation
- Interrupts at 50 or 60 Hz line frequency

DESCRIPTION

The KW11-P Clock provides programmed real-time interval interrupts and interval counting in 3 modes of operation. The major functional units of the Clock include:

16-bit Counter—Counts up or down at 4 selectable rates and can be read while operating. The interrupt sequence is initiated at zero (underflow) during a count down from a preset interval count. The count-up mode is used to count external events; an interrupt is initiated at zero (overflow).

16-bit Count Set Buffer—Stores the preset interval count. At underflow, depending on the operating mode, the buffer automatically reloads the Counter or is cleared.

Control and Status Register—Provides various control and status signals related to the operation of the buffer and counter.

Clock—Provides 2 crystal-controlled signals of 100 kHz and 10 kHz to clock the counter. Two external clock inputs are provided: 50/60 Hz line frequency and an analog signal input.

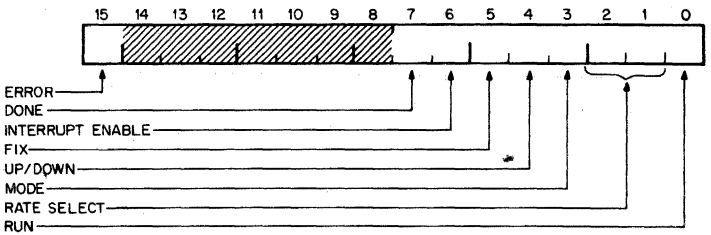
MODES OF OPERATION

Single Interrupt Mode—A program specified time interval is preset and an interrupt is generated at the end of the interval. The time interval, represented as a specific count, is loaded into the counter. Count down or count up is initiated at 1 of 4 selectable rates, and at underflow or overflow an interrupt is generated. Clocking is stopped and the counter is reset to zero.

Repeat-Interrupt Mode—A program specified time interval is preset and repeated interrupts are generated at a rate corresponding to the time interval. Operation is similar to the Single-Interrupt Mode, except that after the interrupt is generated on underflow or overflow, the counter is automatically reloaded from the count set buffer, and clocking is restarted. At the next underflow or overflow, another interrupt is generated.

External Event Counter Mode—The external input is used to clock the counter in the count-up or count-down mode. The counter may be read during operation to determine the number of events that have occurred.

REGISTERS
Control and Status Register 772 540



Effect of the Initialize (INIT) signal: clear all bits.

Read only: bits 15 and 7
Write only: bit 5

BIT	NAME	FUNCTION
15	Error	Set when, in Repeat-Interrupt Mode, a second underflow or overflow occurs before the interrupt of the preceding one has been serviced. It is cleared when the Status Register is addressed.
7	Done	Set on underflow or overflow.
6	Interrupt Enable	Set to allow Done = 1 to cause an interrupt.
5	Fix	Set to cause single clocking of the counter as a maintenance aid.
4	Up/Down	Selects either count-up or count-down for the counter; 1 = up, 0 = down.
3	Mode	Selects interrupt mode of operation; 1 = Repeat-Interrupt, 0 = Single-Interrupt.
2,1	Rate Select	Selects 1 of 4 available clock rates.
0	Run	Set to allow the counter to count. Cleared on underflow or overflow in Single-Interrupt Mode.

Bit 2	Bit 1	Rate
0	0	100 kHz
0	1	10 kHz
1	0	Line frequency
1	1	External

Count Set Buffer Register 772 542
This 16-bit register is used for storage of the interval count. It allows automatic reloading of the Counter in Repeat-Interrupt Mode. The register is cleared by the INITIALIZE signal and by underflow or overflow in the Single Interrupt Mode. The bits are write only.

Counter Register 772 544
This 16-bit register is a binary up/down counter. It is cleared by the INITIALIZE signal. The bits are read only.

SPECIFICATIONS

Main Specifications

Clock rates:	100 kHz, 10 kHz } crystal-controlled
	Line Frequency
	External (Schmitt Trigger input)
Operating modes:	Single Interrupt
	Repeated Interrupt
	External Event Counter
	Non-Interrupt

Register Addresses

Control and Status	772 540
Count Set Buffer	772 542
Counter	772 544

UNIBUS Interface

Interrupt vector address:	104
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot (quad module)

Power 0.5 A at +5 V

DECWRITER, LA30

DESCRIPTION

The LA30 DECwriter is a fast, reliable and low cost data terminal. It prints from a set of 64 characters at speeds up to 30 characters per second. Data entry is made from either a 97- or 128-character keyboard. It produces an original and one copy on a standard 9 7/8-inch wide, tractor-driven continuous form.

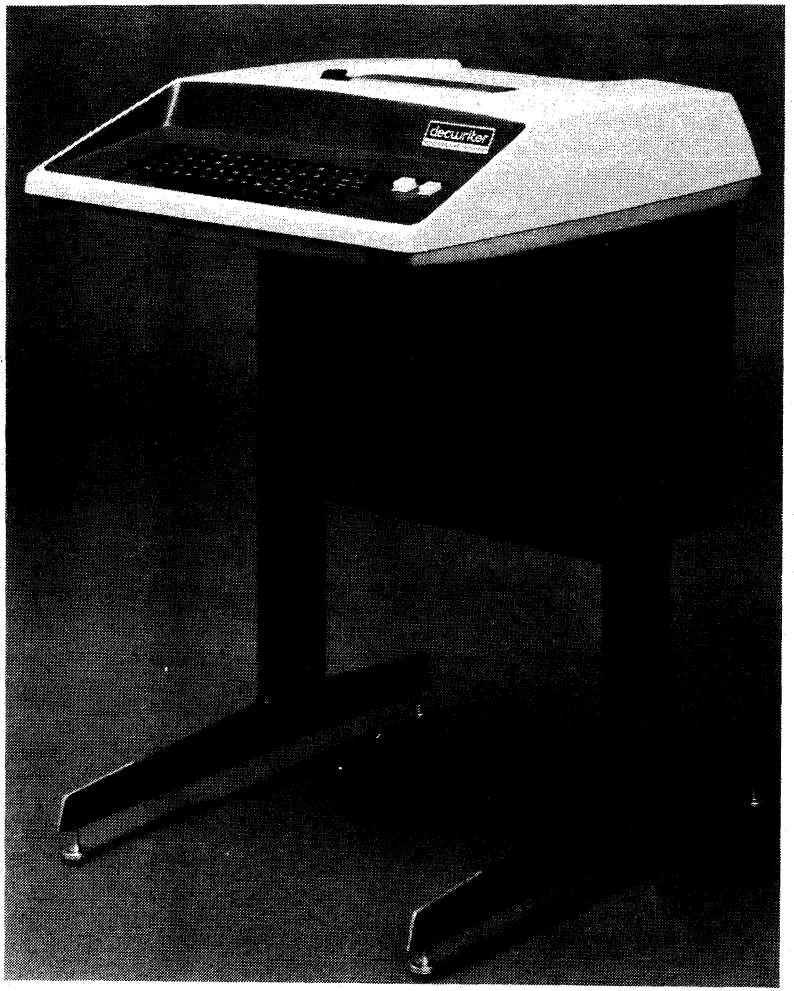
The DECwriter is delivered with an attractive stand. The noise generated by the terminal is less than that of an electric typewriter, a feature, welcomed in an office environment. Because of its low price, the DECwriter is particularly appropriate for systems requiring large numbers of highly reliable printer/terminals.

High reliability has been achieved through reduction of the number of mechanical parts. Clutches, brakes, dashpots and other similar parts have been eliminated from the printing mechanism. Instead, the DECwriter generates a 5 x 7 matrix. Seven solenoid-driven, spring-loaded pins are arranged vertically in the printing head. The head is advanced by solid-state logic; drive circuitry actuates selected pins to generate characters.

CONTROLS AND INDICATORS

The following Table shows the controls and indicators for the serial version of the LA30; the parallel version has only the READY lamp and the LOCAL LINE FEED switch.

READY	**Lamp**—Indicates power up on printer electronics and that the DECwriter is READY for use. Indicates an interrupt is enabled by keyboard electronics, if INT ENB bit is set by software.
LOCAL LINE FEED	**Switch**—When depressed, causes a local line feed to be applied to the printer without a code being sent out to the computer. This control will also disrupt printing, but no characters will be lost.
MODE LOCAL/LINE	**2-Position Switch**—Selects either local or on-line operation.
BAUD RATE 110, 150, 300	**3-Position Switch**—Selects the baud rate clock frequencies for 110, 150, or 300 baud.
MOTOR POWER	**Breaker (CB2)**—Applies power to printer stepping motor electronics.
AC POWER	**Breaker (CB1)**—Applies ac power to the unit power supply.



LA30-DECwriter

REGISTERS

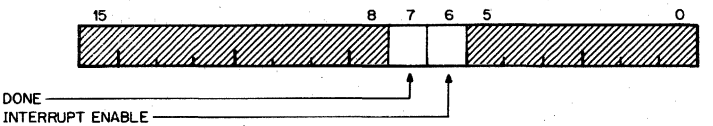
Programming

The parallel version of the LA30 interfaces to the PDP-11 via the LC11-A Control Unit and is explained in this section. The serial version uses the DL11-A Control Unit, which is explained in the LT33 section. The serial LA30 uses a few bits that the parallel LA30 does not.

All software control of LC11-A is accomplished via four device registers. These are assigned memory addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their address.

The UNIBUS addresses mentioned in this section apply only when the LA30 is being used as the console terminal. When used in other applications, the addresses and vectors float, see Appendix A.

Keyboard Status Register (KBS) 777 560

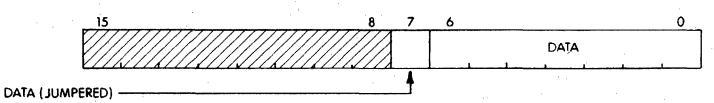


Effect of the Initialize (INIT) signal: clear all bits

Read only: bit 7

BIT	NAME	FUNCTION
7	Done	Set when a character is available in the Keyboard Data Buffer (KBB). It is cleared by any instruction that modifies KBB. If maintenance bit (bit 2 in Printer Status Register) is set, loading the Printer Buffer sets this bit.
6	Interrupt Enable	Set to allow Done = 1 to cause an interrupt.

Keyboard Data Buffer (KBB) 777 562



BIT	NAME	FUNCTION
7	Data (jumpered)	If desired, this bit can be gated onto the bus along with information in the data buffer (bits 6-0). Note that this bit does not come directly from the DECwriter keyboard but is provided by a jumper on the control module. If a jumper is added at J1, the state of this bit is dependent on the condition of the MAINT bit (bit 2 in the Printer Status

Register). If the MAINT bit is not set, KBB bit 7 is read as a 1.

If a jumper is added at J2, this bit is always a 0.

NOTE

A jumper must be added to either J1 or J2 but never to both. If no jumper is present, the bus may hang with BUS D07 asserted; with both jumpers, the keyboard buffer reads as all 0s regardless of the state of the MAINT bit.

Note that bit 7 is not offered as a parity option with the LA30.

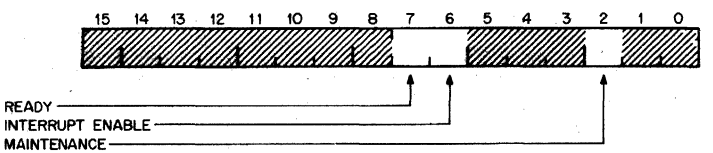
Bits 6 through 0 hold the 7-bit ASCII character read from the keyboard. To the processor, the data is read only.

CAUTION

A character is stored in the buffer only until the next character is keyed. At this time, the buffer is reloaded and the previous character, if it has not already been read, is lost. There is no overrun condition to inform the program of this.

Any program reference to KBB (777 562 or 777 563) as a word or byte will clear Done, bit 7 of the Keyboard Status Register (KBS).

Printer Status Register (PRS) 777 564



Effect of the Initialize (INIT) signal: clear bits 6 and 2, set bit 7

Read only: bit 7

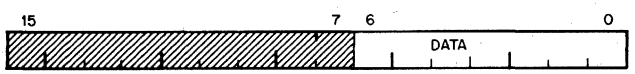
BIT	NAME	FUNCTION
7	Ready	Set when the printer is ready for the next character to be loaded. Indicates that the previous function is either complete or has been started and continued to a point where the printer can accept the next command.
		The bit is set when power is applied to the LA30 and cleared by the leading edge of

the PRINT STROBE signal, which indicates that a character is being sent to the printer.

The printer sets Ready approx 2 μsec after it receives a Carriage Return (CR) command. This permits "non-printing" characters, such as Line Feed (LF), to be received during carriage return time. If a "printing" character is received during carriage return time, Ready is cleared and is then set after CR and printing are complete.

6	Interrupt Enable	Set to allow Ready = 1 to cause an interrupt.

Printer Data Buffer (PRB) 777 566



Bits 6 through 0 hold the 7-bit ASCII coded data for the character to be printed (or acted upon). To the processor, the date is write only.

Any instruction that modifies PRB as a word or byte, clears Ready, bit 7 of the Printer Status Register (PRS).

Note that bit 7 is not offered as a parity option on the LA30.

PROGRAMMING EXAMPLES

Read a character (from keyboard)

```
LOOP:   TSTB KBS        ;LOOK FOR DONE
        BPL LOOP        ;WAIT IF DONE = 0
READ:   MOV KBB, R0     ;READ CHARACTER
```

ECHO keyboard

```
ECHO:   TSTB KBS        ;CHARACTER AVAILABLE?
        BPL ECHO        ;WAIT IF DONE = 0
WAIT:   TSTB PRS        ;IS PRINTER READY?
        BPL WAIT        ;WAIT IF READY = 0
        MOV KBB, PRB    ;PRINT CHARACTER
        BR ECHO         ;REPEAT FOR NEXT CHARACTER
```

SPECIFICATIONS FOR LA30

Main Specifications

Printing speed:	30 char/sec, asynchronous
Number of columns:	80
Printing characters:	64 (upper case ASCII subset)

Keyboard characters:	97 or 128 (switch selectable)
Carriage return time:	300 msec

Printing

Type:	impact, 5 x 7 dot matrix
Vertical spacing:	6 lines/inch
Horizontal spacing:	10 char/inch

Paper

Type:	9-7/8 inch wide, continuous form, tractor-driven, original plus one copy
Slew speed:	30 lines/sec

Mechanical

Mounting:	1 free-standing unit
Size:	31"H x 21"W x 24"D
Weight:	110 lbs

Power

Input current:	3 A at 115 VAC
Heat dissipation:	300 W

Environment

Operating temperature:	15°C to 35°C
Relative Humidity:	20% to 80%

Models

LA30-PA:	DECwriter, parallel interface, (Control is LC11-A), 115 VAC, 60 Hz
LA30-PD:	DECwriter, parallel interface, (Control is LC11-A), 230 VAC, 50 Hz
LA30-CA:	DECwriter, serial interface, (Control is DL11-A), 115 VAC, 60 Hz
LA30-CD:	DECwriter, serial interface, (Control is DL11-A), 230 VAC, 50 Hz
LA30-EA:	DECwriter, serial interface to a modem, 115 VAC, 60 Hz
LA30-ED:	DECwriter, serial interface to a modem, 230 VAC, 50 Hz

SPECIFICATIONS FOR LC11-A or DL11-A (interfaced to LA30)

Usage:	Control for LA30 DECwriter

Register Addresses

Keyboard Status (KBS)	777 560
Keyboard Buffer (KBB)	777 562
Printer Status (PRS)	777 564
Printer Buffer (PRB)	777 566

UNIBUS Interface

Interrupt vector address:	60 (for keyboard) 64 (for printer)
Priority level:	BR4 (keyboard has precedence over printer)
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot
Size:	quad module

Input current

LC11-A:	1.5 A at +5 V
DL11-A:	1.8 A at +5 V, 0.15 A at −15 V

Models

LC11-A:	Control for parallel LA30
DL11-A:	Control for serial LA30

HIGH SPEED LINE PRINTER, LP11

DESCRIPTION

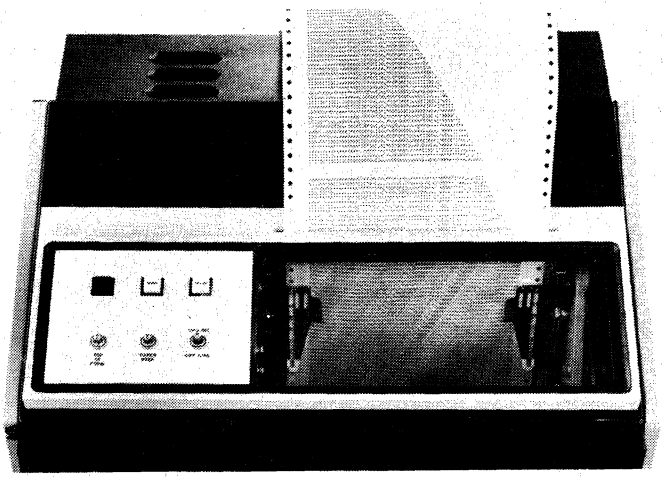
The LP11 High Speed Line Printer is available in several models, ranging from an 80-column, 64-character model to a 132-column, 96-character model. Either column-width printer is available with 64- or 96-character print sets. The printer is an impact type using a revolving character drum and a hammer per column. Forms up to six-parts, may be used for multiple copies. Fanfold paper from 4-inch to 19 inches wide (depending on model) may be used with adjustment for pin-feed tractors. The print rate is dependent upon the data and the number of columns to be printed.

There are six different line printers to choose from. A control unit is included.

LP11-F	80 column, 64 character
LP11-H	80 column, 96 character
LP11-J	132 column, 64 character
LP11-K	132 column, 96 character
LP11-R	132 column, 64 character (heavy duty, high speed)
LP11-S	132 column, 96 character (heavy duty, high speed)

LP11-F, LP11-H, LP11-J, LP11-K

- Low cost
- High reliability
- Upper and lower case characters
- Print up to 1110 lines per minute
- Long-life print hammer
- Easy to read indicators
- 90 degree drum gate opening for easy paper and ribbon loading



LP11 HIGH SPEED LINE PRINTER

Operation

Characters are loaded into the printer memory via the LPB (Line Printer Buffer) serially by character. When the memory becomes full (20 characters) they are automatically printed. This continues until the full 80 columns have been printed or a special character is recognized. The 132-column model prints 24 characters at a time. The special characters (non-printing) are:

CR (015_8) Carriage Return. Causes the currently-stored characters to be printed, and resets the column counter to 1 (the next printing character loaded would print in column 1). Does not advance the paper.

LF (012_8) Line Feed. Causes the currently-stored characters to be printed, then resets the column counter to 1 and advances the paper one line.

FF (014_8) Form Feed. Causes the currently-stored characters to be printed, then resets the column counter to 1 and advances the paper to top of next page.

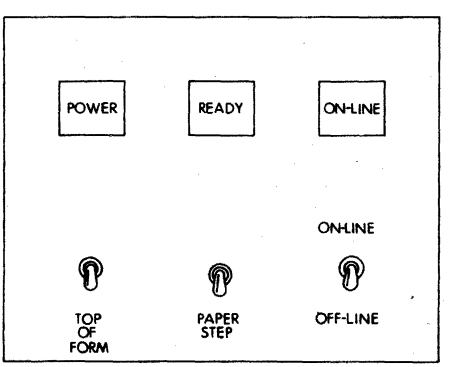
Timing Considerations

The LP11 will accept characters at a 750 KHz rate until the character print memory is filled. There is a delay of approximately 4 milliseconds while the printing is done. An LF command requires about 20 milliseconds. FF commands cause paper slewing at a maximum rate of 13 inches per second—timing is dependent upon the distance to the next top of form.

For maximum transfer and highest printing rate, a full (20 or 24) character buffer should be transferred as rapidly as possible with the interrupt disabled. If the interrupt is enabled after the buffer is filled or after an FF, CR or LF command, then the interrupt will occur following the completion of the print and/or paper-move cycles.

INDICATORS & CONTROLS

The following figure shows the printer control panel on which are mounted three indicator lights and three toggle switches.



Line Printer Control Panel

Operation of the lights and switches is as follows:

POWER light	Glows to indicate main power switch is at ON position and power is available to the printer.
READY light	Glows shortly after the POWER light goes on to indicate that internal components have reached synchronous state and the printer is ready to operate.
ON LINE light	Glows to indicate that ON LINE/OFF LINE toggle switch is in ON LINE position.
ON/OFF (main power) switch	This switch controls line current to the printer. If power is available, the POWER light on the control panel will glow when the switch is positioned at ON. The switch is on when in the up position. The ON and OFF labels are printed on the stem of the switch.
TOP OF FORM switch	This switch is used to roll up the form to the top of the succeeding page. It is spring returned to null position, and produces a single top-of-form operation each time it is actuated. The switch is effective only when the printer is off line.
PAPER STEP switch	Operates similarly to TOP OF FORM but produces a single line step each time it is actuated. It is only effective with printer off line.
ON LINE/ OFF LINE switch	This two-position toggle switch is spring-returned to center. When momentarily positioned at ON LINE it logically connects the printer to the computer and causes the ON LINE light to glow. Positioned momentarily at OFF LINE, the logical connection to the computer is broken, the ON LINE light goes off, and the TOP OF FORM and PAPER STEP switches are enabled.

LP11-R and LP11-S

- Minimum wander in print line
- Simple rugged hammer mechanism
- Vernier adjustment for both horizontal and vertical paper tension
- Copies control to compensate for thickness
- Full line buffering

The LP11-R and LP11-S are fast, reliable, high quality drum printers with 64 and 96 characters respectively. Paper and inked ribbon pass between a row of hammers and a continuously rotating metal drum, containing 132 columns of all print characters. A 132-column line is printed in one drum revolution or less.

The LP11-R and S require minimum maintenance due to their modular design and integrated circuitry. Paper is loaded by opening the drum gate and placing the paper directly on the tractors. The wide swing of the gate provides complete access to the paper loading area and the print ribbon.

Operator Controls
The operator's control panel, externally located on top of the cabinet, contains the following switches and indicators.

Indicators:
Power—Illuminated when power is on.

Ready—Illuminated when power is on and all interlocks are closed.

On Line—Illuminated when printer is in the ready condition, the print inhibit switch is off, and the on line switch has been actuated.

Drum Gate—Indicates the drum gate is unlatched.

Print Inhibit—Indicates the print inhibit switch is on—Hammer Fault.

Paper Fault—Indicates the paper is torn or out: ribbon counter alarm or runaway is detected.

Switches
Top of Form—A momentary switch used to advance the tractors to a top of form position, i.e., channel zero of the tape reader. This switch is disabled when the printer is on line.

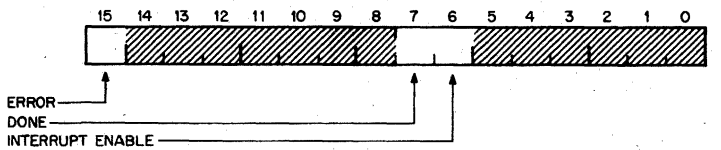
On Line/Off Line—A momentary switch that puts the printer on line and illuminates the on line indicator. In order to put the printer on line, the ready indicator must be on and the print inhibit switch must be off. If the printer is on line and the switch is actuated, the printer will go off line and extinguish the on line indicator.

Master Clear—A momentary switch that initializes the printer control electronics.

Main Power—A circuit breaker which allows the operator to enable or disable primary power to the printer.

REGISTERS

Line Printer Status Register (LPS) 777 514

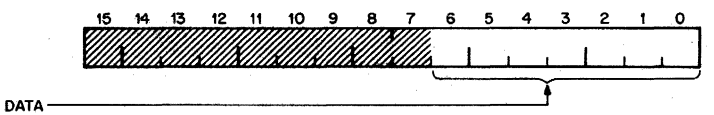


Effect of the Initialize (INIT) signal: clear bit 6

Read only: bits 15 and 7

BIT	NAME	FUNCTION
15	Error	Set when an error condition exists in the printer. Errors are: a) Power off b) No paper c) Printer drum gate open d) Over temperature alarm e) Printer placed OFF-LINE Reset only by manual correction of error condition.
7	Done	Set whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point when the printer may accept the next command. Set only by printer condition. Will not be set if printer is OFF-LINE.
6	Interrupt Enable	Set to allow Done or Error =1 to cause an interrupt.

Line Printer Data Buffer Register (LPB) 777 516



Bits 6 through 0 hold the 7-bit ASCII coded data for the character to be printed. To the processor, the data is write only.

PROGRAMMING EXAMPLE

Interrupt Service Routine

```
200:    LPSERV              ;VECTOR TO SERVICE ROUTINE
242:    200                 ;SERVICE AT PRIORITY 4
MAIN:   BIS #100,LPS        ;ENABLE INTERRUPT
LPSERV: TST LPS             ;CHECK FOR ERROR
        BMI ERROR           ;BRANCH IF ERROR
        MOV R0,-(SP)        ;SAVE R0
        MOV BUFADR,R0       ;GET BUFFER POINTER
```

```
LOAD:   MOVB (R0) + ,LPB    ;LOAD PRINTER BUFFER
        CMP R0,BUFEND       ;END OF DATA?
        BHI PRCOMP          ;YES, GO TO PRINT COMPLETE
        TSTB LPS            ;NO, CHECK DONE
        BMI LOAD            ;NOT FULL, GET ANOTHER CHAR.

EXIT:   MOV R0,BUFADR       ;SAVE BUFFER POINTER
        MOV (SP) + ,R0      ;RESTORE R0
        RTI
```

SPECIFICATIONS

Main Specifications

Number of columns:	80 or 132
Number of characters:	64 or 96
Printing speed:	170 to 1200 lines/min (full line)

Printing

Method:	drum
Size of characters:	0.095" high x 0.065" wide
Vertical spacing:	6 lines/inch
Horizontal spacing:	10 char/inch

Character Set

64 characters:	A to Z, 0 to 9, ! " # $ % & ' ( ) * + — / : , . ; < = > ? @ [ ] \ — space ^
96 characters:	all the above plus a to z { } \ ~

Paper

Type:	standard fanfold, edge punched, 11 inches between folds 15 lb bond for single copy 12 lb bond with single shot carbon for up to 6 parts.

Register Addresses

Printer Status (LPS)	777 514
Printer Data Buffer (LPB)	777 516

UNIBUS Interface

Interrupt vector address:	200
Priority level:	BR4
Bus loading:	1 bus load

Mounting: 1 free-standing unit + 1 SPC slot

Current for control: 1.5 A at +5 V

Environment

Operating temperature:	10°C to 43°C
Relative humidity:	15% to 80%

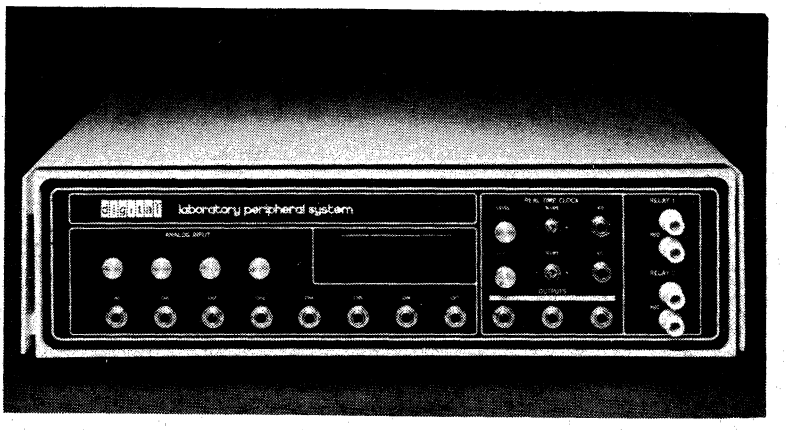
Models

	LP11-F	LP11-H	LP11-J	LP11-K	LP11-R	LP11-S
Number of columns:	80	80	132	132	132	132
Number of characters:	64	96	64	96	64	96
Print speed (full line):	350 LPM	250	240	170	1200	900
Line advance time:	20 msec		20 msec		20 msec	
Paper width:	4" to 9⅞"		4" to 14⅞"		4" to 19"	
Paper slew speed:	13 in/sec		13 in/sec		35 in/sec	
Size:	46H x 24W x 22D		46 x 48 x 25		48 x 49 x 36	
Weight:	200 lbs.		575 lbs.		800 lbs.	
Current at 115 VAC:	2 A		4 A		17 A	
Power dissipation:	250 W		500 W		2000 W	

LAB PERIPHERAL SYSTEM, LPS11

FEATURES

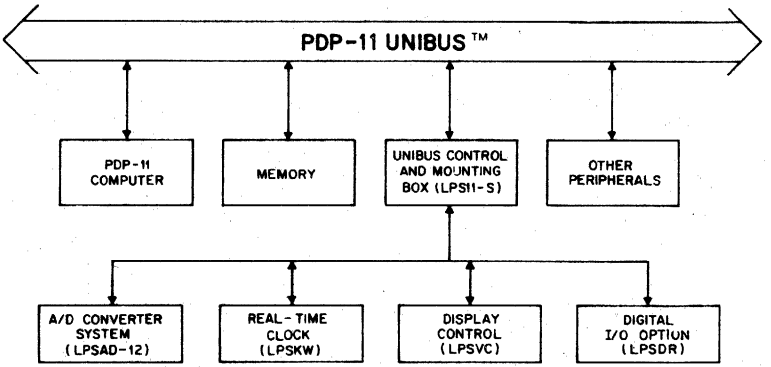
- Flexible
- Low cost
- Easy to Interface
- 5¼ Inches High
- 4 Plug-In Options
  —A/D Converter
  —Real Time Clock
  —Display Controller
  —Digital I/O Registers



LPS-11 Lab Peripheral System

The LPS-11 Lab Peripheral System is a high performance, modular, real-time subsystem which interfaces to the PDP-11 family of computers. The system houses a 12-bit A/D Converter, Programmable Real Time Clock, Display Controller and a 16-bit Digital I/O Option. The front panel is designed to permit easy interfacing with outside instrumentation. The LPS is 5¼ inches high and mounts in a standard 19-inch cabinet. All necessary power and cables are included.

The flexibility of the LPS makes it well-suited to a variety of applications including biomedical research, analytical instrumentation, data collection and reduction, monitoring, data logging, industrial testing, engineering and technical education.



LAB PERIPHERAL SYSTEM

A/D CONVERTER SYSTEM (LPSAD-12)

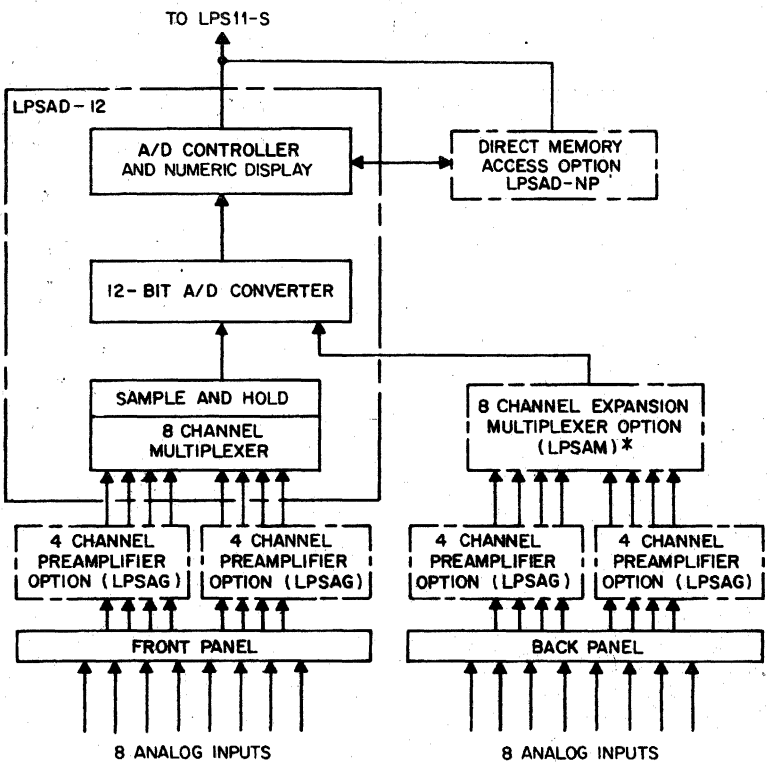
- Sample and Hold Circuitry
- Dual Sample and Hold Option
- DMA Option
- 8-Channel Multiplexer
- Optional Expansion Multiplexer
- Light Emitting Diode (LED) Display
- Differential Preamplifier Option

The 12-bit A/D Converter System enables the user to sample analog data at specified rates and store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The throughput rate for a single channel is approximately 40 kHz.

Included in the system is an 8-channel multiplexer which provides 8 single-ended ± 5 volt inputs. Four of the channels are connected to phone jacks on the front panel and to potentiometer knobs, which can be used as program parameter inputs. The other four channels are also connected to phone jacks which permit direct interfacing with the laboratory equipment. An 8-channel expansion multiplexer option (LPSAM) may be added so that the system can handle a total of 16 channels.

The LPSAG option implements 4 channels with preamplifiers and provides a ± 1 volt differential input to the preamplifier-implemented channels. Ranges of 0 to 2, ± 5, and 0 to 10 volts are optionally available.

A direct memory access (DMA) option (LPSAD-NP) to the A/D Converter allows the conversions to be stored in memory at maximum rates without processor intervention. The user can specify the buffer size (4K maximum) and location for the digitized data. This frees the central



A/D CONVERTER SYSTEM (LPSAD-12)

processor for other tasks until an interrupt indicates the buffer has been filled. The throughput rate will depend on the number of bits used in the conversion. For example, for 12-bit single channel A/D operation, the throughput rate is 47 kHz; if only 10 bits are used, the rate is 75 kHz; for 8 bits, the rate is 100 kHz.

Also implemented in the system is a programmable 6-digit decimal numeric readout Light Emitting Diode (LED) display, which is mounted on the front panel of the LPS11-S. The LED display is useful for programmed visual indications.

* If a dual Sample and Hold configuration is required, the LPSSH option must be implemented. The LPSAM is prerequisite for the LPSSH.

When speed as well as accuracy is of primary importance, a dual sample and hold configuration (LPSSH option) will enable the user to acquire data from two fixed and predetermined channels simultaneously.

PROGRAMMABLE REAL-TIME CLOCK (LPSKW)

- 5 Programmable Frequencies
- 4 Programmable Modes of Operation
- 2 Schmitt Triggers and Line Frequency
- Concurrent Operations

The LPSKW Programmable Real-Time Clock offers the user several methods for accurately measuring and counting intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events or provide interrupts at programmable intervals. It can be used to start an analog to digital converter with the overflow from the clock counter or from the firing of a Schmitt trigger. Many of these operations can be performed concurrently.

The clock will operate in any one of four programmable modes: single interrupt, repeated interrupts, external event timing, and event counting from zero base.

The user can choose from five programmable frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz. The real-time clock also provides an external (Schmitt trigger) input and a line frequency input.

Included with the real-time clock are two Schmitt triggers with the front panel slope and level adjusting knobs. The Schmitt triggers can start and read the clock, start the A/D converter, and cause program interrupts.

DISPLAY CONTROL (LPSVC)

- 4096 By 4096 Dot Array
- "Fast Intensification Enable" Feature
- 4 Program-Controlled Modes

The LPSVC Display Control will display data in the form of a 4096 by 4096 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix RM503, 602 and 604 scopes and the 611 and 613 storage scopes.

The display control offers four program-controlled modes in which the scope can intensify a point. In addition, the "Fast Intensification Enable" feature enables X or Y register values to be changed by a small increment without a long scope settling time. This feature is useful in developing a software character generator. The display control includes two 12-bit D/A converters with ± 5 V full scale nominal output and all the necessary circuitry and controls.

DIGITAL I/O OPTION (LPSDR)

- Program Controlled Relays
- Two Modes of Program Control

- Recoverable Overload Protection
- TTL Compatible Voltage Levels

The Digital I/O Option consists of a 16-bit buffered input register and a 16-bit buffered output register. The I/O Option features two program controlled relays which are normally left open. Using these relays, laboratory equipment such as recorders, oscillators, lamps, motors and general instrumentation may be conveniently controlled.

Program control of digital input/output can be achieved in either of two selectable modes.

Program Transfer Mode
The transfer of data between the digital I/O registers and memory may be accomplished through the use of a MOVE instruction. Flags are set when data has been received and accepted by either the input or output registers. The user program tests the data flag and determines what additional operations are necessary.

External Interrupt Mode
This mode allows an external device to initiate the transfer of data. A pulse is received from the external device and an interrupt is automatically initiated. The program is then vectored to a predetermined memory address and the user routine takes control. This mode frees the user program from having to read and clear the data transfer flags.

All voltage levels are TTL compatible with a recoverable overload protection of up to ± 20 volts. The circuits are equipped with fuse resistors to ensure protection above 20 volts.

PROGRAMMING

STANDARD* REGISTER ADDRESSES

Option	Register	Address
LPSAD-12	Status	770 400
LPSAD-12	Buffer/Led	770 402
LPSKW	Status	770 404
LPSKW	Buffer/Preset	770 406
LPSDR	Status	770 410
LPSDR	Input	770 412
LPSDR	Output	770 414
LPSVC	Status	770 416
LPSVC	X—D/A	770 420
LPSVC	Y—D/A	770 422
LPSVC	EXT D/A	770 424
Unused	—	770 426
Unused	—	770 430
Unused	—	770 432
Unused	—	770 434
LPSAD-NP	DMA	770 436

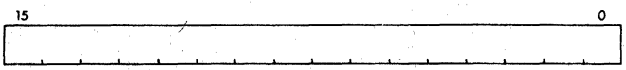
* The register address is jumper selectable in increments of 40 locations; however, the relative location of the various registers will remain the same (see Appendix A).

VECTOR ADDRESSES** And PRIORITY LEVELS

Option	Address	BR Level
LPSAD-12	300	6
LPSKW	304	5
LPSDR (IN)	310	4
LPSDR (OUT)	314	4
LPSVC	320	4
UNDEFINED	324	4
LPSAD-NP	300	6

** The vector address field is jumper selectable, and will be assigned in conjunction with existing options. However, the relative positions of the option will remain constant once the initial location is determined.

LPSAD-12 STATUS REGISTER

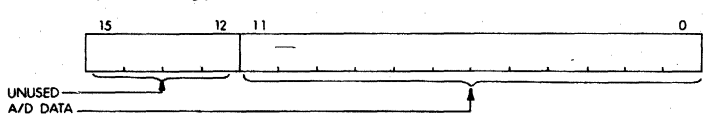


Bit	Function
15	Error Flag
14	Dual Mode Enable (LPSSH)
13-8	Multiplexer Channel
7	A/D Done Flag
6	Interrupt Enable
5	Clock Overflow Enable
4	Schmitt Trigger Enable
3	Burst Mode (LPSAD-NP)
2, 1	DMA Address Pointer (LPSAD-NP)
0	A/D Start

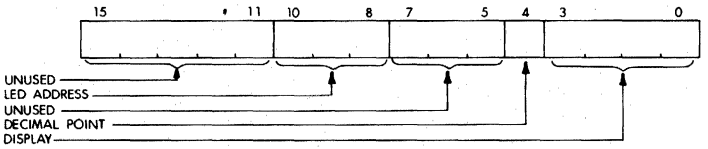
Bit 2	Bit 1	Function
0	0	Unused
0	1	DMA Status Register
1	0	DMA Word Count Register
1	1	DMA Current Address Register

LPSAD-12 BUFFER/LED REGISTER

A/D Buffer (Read only)



LED Register—Numeric Display (Write only)



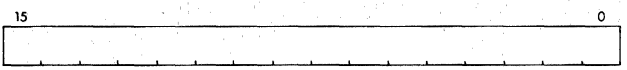
LED Address

Bit 10	Bit 9	Bit 8	Digit
0	0	0	LED 1 (Rightmost)
0	0	1	LED 2
0	1	0	LED 3
0	1	1	LED 4
1	0	0	LED 5
1	0	1	LED 6 (Leftmost)
1	1	0	Unused
1	1	1	Unused

Display

Bit 3	Bit 2	Bit 1	Bit 0	Numeric Value
0	0	0	0	Number 0
0	0	0	1	Number 1
0	0	1	0	Number 2
0	0	1	1	Number 3
0	1	0	0	Number 4
0	1	0	1	Number 5
0	1	1	0	Number 6
0	1	1	1	Number 7
1	0	0	0	Number 8
1	0	0	1	Number 9
1	0	1	0	Test Pattern
1	0	1	1	Blank
1	1	0	0	Blank
1	1	0	1	Minus Sign
1	1	1	0	Blank
1	1	1	1	Blank

LPSKW STATUS REGISTER



Bit	Function
15	Schmitt Trigger #1 Flag
14	Schmitt Trigger #1 Interrupt Enable
13	Schmitt Trigger #1 Clock Start Enable
12	Maintenance Schmitt Trigger #1
11	Maintenance Count
10	Maintenance Schmitt Trigger #2
9, 8	Mode
7	Mode Flag
6	Mode Interrupt Enable
5, 4	Unused
3, 2, 1	Rate
0	Clock Enable

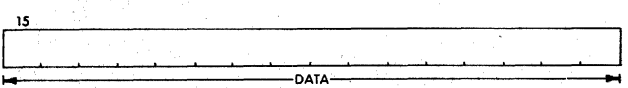
Mode

Bit 9	Bit 8	Function
0	0	Single Interval
0	1	Repeated Interval
1	0	External Interval (Schmitt Trigger #2)
1	1	External Interval from Zero Base

Rate

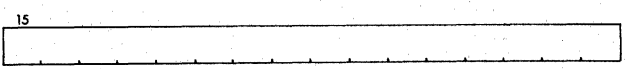
Bit 3	Bit 2	Bit 1	Base Frequency
0	0	0	Stop
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	External (Schmitt Trigger #1)
1	1	1	Line Frequency

LPSKW BUFFER/PRESET REGISTER



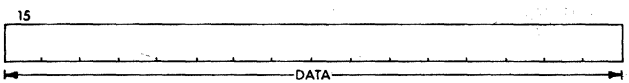
No byte operation is permitted. Data will simultaneously be loaded to the clock counter when Bit 0 of the status register is disqualified.

LPSDR STATUS REGISTER



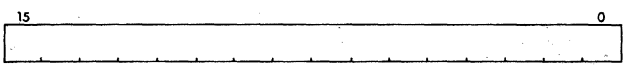
Bit	Function
15	Output Flag
14	Output Interrupt Enable
13	Maintenance Bit 2
12-9	Unused
8	Relay #2
7	Input Flag
6	Input Interrupt Enable
5	Maintenance Bit 1
4-2	Unused
1	Load Input Buffer
0	Relay #1

LPSDR INPUT and OUTPUT REGISTERS



Input — Read only
Output — Read/Write

LPSVC STATUS REGISTER

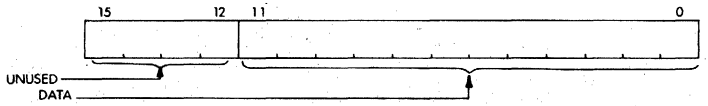


Bit	Function
15-13	Unused
12	Erase (Storage Scope)
11	Write thru (Storage Scope)
10	Store (Storage Scope)
9	Channel (VR14)
8	Unused
7	Ready Flag
6	Interrupt Enable
5	Unused
4	Ext Delay (Special Scopes)
2, 3	Mode
1	Fast Intensify
0	Intensify

Mode

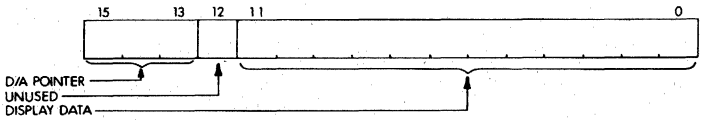
Bit 3	Bit 2	Function
0	0	Intensification with Bit 0 only
0	1	Intensification on Loading X Register
1	0	Intensification on Loading Y Register
1	1	Intensification on X or Y

LPSVC X and Y REGISTERS



Data is in offset binary format.

LPSVC EXT D/A REGISTER



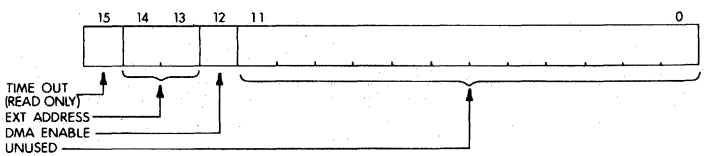
D/A Pointer

Bit 15	Bit 14	Bit 13	Expansion D/A Converter
0	0	0	DAC 0 (LPS DA #1)
0	0	1	DAC 1 (LPS DA #1)
0	1	0	DAC 2 (LPS DA #2)
0	1	1	DAC 3 (LPS DA #2)
1	0	0	DAC 4 (LPS DA #3)
1	0	1	DAC 5 (LPS DA #3)
1	1	0	DAC 6 (LPS DA #4)
1	1	1	DAC 7 (LPS DA #4)

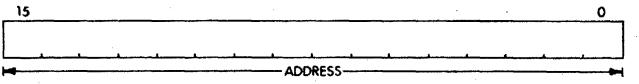
LPSAD-NP DMA REGISTER

The DMA Register will function as defined by the DMA Pointer in the LPS AD-12 Status Register

DMA Status Register

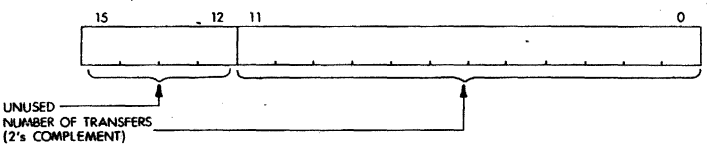


DMA Current Address Register



Bit 0 will always be loaded as a zero.

DMA Word Count Register



SPECIFICATIONS FOR LPS11-S

Register Addresses:	floating (see Appendix A)
UNIBUS Interface	
Interrupt vector address:	floating (see Appendix A)
Priority level:	BR 4 to 6
Data transfer:	NPR (optional)
Bus loading:	1 bus load
Mechanical	
Mounting:	1 panel mounted unit (or table top)
Size:	5¼" front panel height (5¼"H x 19"W x 23"D)
Weight:	80 lbs.
Power	
Input Current:	3 A at 115 VAC, max.
Heat dissipation:	300 W
Environment	
Operating temperature:	5°C to 43°C
Relative humidity:	20% to 80%

Models

LPS11-SA: Lab Peripheral System, rack mount, 115 VAC, 60 Hz
LPS11-SB: " rack mount, 230 VAC, 50 Hz
LPS11-SD: " table top, 115 VAC, 60 Hz
LPS11-SE: " table top, 230 VAC, 50 Hz

Model	Description	Prerequisite
LPSAD-12:	12-bit ADC, sample & hold, 8 channel multiplexer, and LED (Light Emitting Diodes) 6-digit programmable decimal readout display.	LPS11-S
LPSAD-NP:	Direct memory access (DMA) option for LPSAD-12 ADC.	LPSAD-12
LPSAM:	8 channel expansion multiplexer (if more than 8 channels are implemented).	LPSAD-12
LPSSH:	Second Sample & Hold for a Dual Sample & Hold Configuration.	LPSAM
LPSAG:	Four differential preamplifiers with ± 1 volt input. Maximum of 4 LPSAGs per LPS11-S system.	LPSAD-12
LPSAG-VG:	Four independently selectable multigain differential preamplifiers. Ranges: ± 1V, ± 5V, 0 to + 2V, 0 to + 10V; and all differential inputs.	LPSAD-12
LPSKW:	Programmable real-time clock & two Schmitt triggers.	LPS11-S
LPSVC:	Display control including two 12-bit DACS. This controller is capable of handling a VR14; also, Tektronix's RM503, 602, 604, 611 & 613 scopes.	LPS11-S
LPSDR:	16-bit buffered digital I/O with drive capabilities and two programmable N.O. relays.	LPS11-S

LINE PRINTER, LS11

FEATURES

- 132-column impact printer
- Prints expanded or oversized characters
- 60 lines per minute—165 characters per second
- Vertical forms control
- Pin feed forms handlling
- Multiple copy
- Variable paper width
- Software select/de-select codes

DESCRIPTION

The LS11 Line Printer is a functional and attractive forms-handling unit designed to print clear reports, statements, and listings as required by most users. It is an inexpensive, medium-speed, and reliable impact dot-matrix line printer for the PDP-11 family. The Line Printer prints at a rate of 165 characters per second at 10 characters per inch with up to 132 characters per line, using the latest state-of-the-art imprint techniques. Printing speeds range from 60 lines per minute on full lines to 200 lines per minute for 20-character lines. The print assembly is a completely self-contained unit that includes the power supply plus the mechanical and logical components.

Vertical Forms Control (VFC)

The LS11 includes a vertical forms control feature that consists of a two-track tape-controlled tractor carriage. The two-track tape is standard 1-inch perforated tape (10 holes per inch) that can be readily obtained in a variety of materials to meet desired life requirements. This feature provides flexibility of vertical forms movement under program control. The two channels are designated (1) top of form and (2) vertical tab. The top of form can also be operated manually.

Vertical line spacing is 6 lines per inch. Slew speed is 4 inches per second and single-line spacing takes 45 milliseconds, with 40 milliseconds added for each additional line of multiple-line slew.

Line/Form Feed

A line- or form-feed instruction causes a carriage return (print cycle) and then executes the line or form feed. This assures compatibility with software written for the LP-11 Line Printers.

Printable Character Set

The basic character set is USASCII. The USASCII character set consists of 10 numeric digits (0 through 9), 26 upper-case letters (A through Z), and the 26 special characters shown below.

USASCII	
"	'
:	+
.	;
$	=
,	[
#	]
>	?
*	&
%	—
@	/
(	<
)	\
!	^

SPECIAL CHARACTERS

Ribbon
The LS11 Printer uses a special single-color 1-inch fabric ribbon on standard 3-inch spools. The ribbon is mounted such that it angles across the face of the platen and allows full utilization of the entire ribbon, thereby extending ribbon life.

Forms Specification
Width of forms used on the LS11 Line Printer is restricted only to the width of the standard 14 7/8-inch form. Both tractors are adjustable and can be moved to accommodate narrower form widths.

CONTROLS & INDICATORS

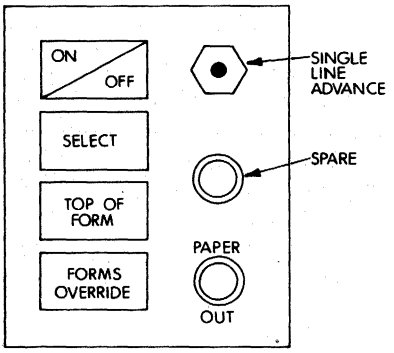
On/Off Switch—lighted in the on position.

Top of Form Switch—used for manual slewing to top of form for proper location of the VFC tape when installing forms.

Select Switch—used to select the printer after turning on power.

Forms Override—an operator override on the paper out switch. This allows the operator to complete the form being printed before changing paper.

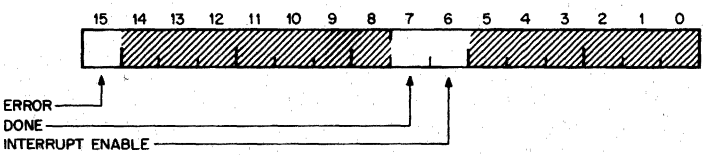
Paper Out Indicator Light—indicates out of paper or a paper-handling malfunction.



OPERATOR PANEL

REGISTERS

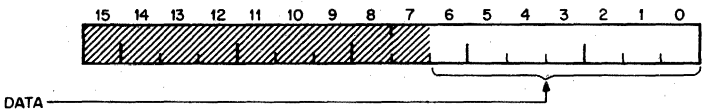
Control and Status Register (LSCS) 777 514



BIT	NAME	FUNCTION
15	Error	ERROR asserted indicates the Inclusive OR of one of the following line printer error conditions: a. Paper Empty b. Hardware Alarm c. Light Detection d. Select ERROR is Read Only, and is reset only when the error condition is removed. If Interrupt Enable is also set, the LS11 starts an interrupt sequence.
7	Done	DONE is asserted when the line printer is ready to accept another character. DONE is set by INIT and cleared by loading the LSDB. If Interrupt Enable is also set, the LS11 starts an interrupt sequence.

6	Interrupt Enable	Interrupt Enable is set or cleared by the program and cleared by INIT. Either DONE or ERROR set when IE is set initiates an interrupt sequence.

Data Buffer Register (LSDB) 777 516



BIT	NAME	FUNCTION
6-0	Data	The Data bits are the 7-bit characters transferred to the line printer. The characters are coded in ASCII and are Write Only.

PROGRAMMING EXAMPLE

The following example represents a typical program used to control the line printer by means of an interrupt service routine.

The routine requires 18 words. This routine may be speeded up by saving and restoring R1, R2, and R3, and loading these registers with the LPCS, LPDA, and BUFFEND values.

Interrupt Service Routine

```
        LPCS = 777 514                  ;CONTROL AND STATUS
                                        ;REGISTER
        LPDB = 777 516                  ;DATA BUFFER REGISTER
        SP = %7
        . = 200                         ;ORIGIN FOR LPT VECTOR
        .WORD   LPSERV                  ;VECTOR TO SERVICE
                                        ;ROUTINE
        .WORD   200                     ;SERVICE AT PRIORITY
                                        ;LEVEL 4
        . = 1000
        .

MAIN:   BIS     #100,   LPCS            ;ENABLE INTERRUPT
        .
        .
        . = 2000

LPSERV: TST     LPCS                    ;CHECK FOR ERROR
        BMI     ERROR
        MOV     %0,     -(SP)           ;SAVE R0
        MOV     BUFADR, %0              ;GET BUFFER POINTER
```

```
LOAD:   MOVB    %0,     LPDB    ;LOAD PRINTER BUFFER
        CMP     (%0) +, BUFEND  ;END OF DATA?
        BHI     PRCOMP          ;YES, GO TO PRINT
                                ;COMPLETE
        TSTB    LPCS            ;NO, CHECK READY
        BMI     LOAD            ;NOT FULL, GET ANOTHER
                                ;CHARACTER

EXIT:   MOV     %0,     BUFADR  ;SAVE BUFFER POINTER
        MOV     (SP) +, %0      ;RESTORE R0

        RTI                     ;BACK TO MAIN PROGRAM
BUFADR:                         ;BUFFER DATA POINTER
BUFEND:                         ;BUFFER END ADDRESS
ERROR:                          ;START OF ERROR
                                ;ROUTINE
PRCOMP:                         ;START OF ROUTINE FOR
                                ;PRINTER COMPLETE

        .END
BUFADR  002 044
BUFEND  002 044
ERROR   002 044
EXIT    002 034
LOAD    002 014
LPCS    777 514
LPDB    777 516
LPSERV  002 000
MAIN    001 002
PRCOMP  002 044
SP      000 007R
```

SPECIFICATIONS

Main Specifications

Number of columns:	132
Number of characters:	62
Printing speed:	165 char/sec 60 lines/min (for 132 columns)
Carriage return time:	200 msec, max

Printing

Method:	impact, 7 x 9 dot matrix
Vertical spacing:	6 lines/inch
Horizontal spacing:	10 char/inch

Paper

Type:	multiple copy, up to 5 parts with single-shot carbon
Size:	4" to 14⅞" wide
Slew speed:	4 inches/sec
Single line advance:	45 msec

Register Addresses

Data Buffer	(LSCS)	777 514
Control and Status	(LSDB)	777 516

UNIBUS Interface

Interrupt vector address:	200
Priority level:	BR4
Bus loading:	1 bus load

Mechanical

Mounting:	1 table-top unit + 1 SPC slot
Size:	12"H x 28"W x 20"D + quad module
Weight:	155 lbs.

Power

Input current:	3 A at 115 VAC
	1.5 A at + 5 V (for control)
Heat dissipation:	300 W

Environmental

Operating temperature:	5°C to 38°C
Relative huimidity:	5% to 90%

Models

LS11-A: Printer and control, 115 VAC, 60 Hz
LS11-B: " 230 VAC, 50 Hz

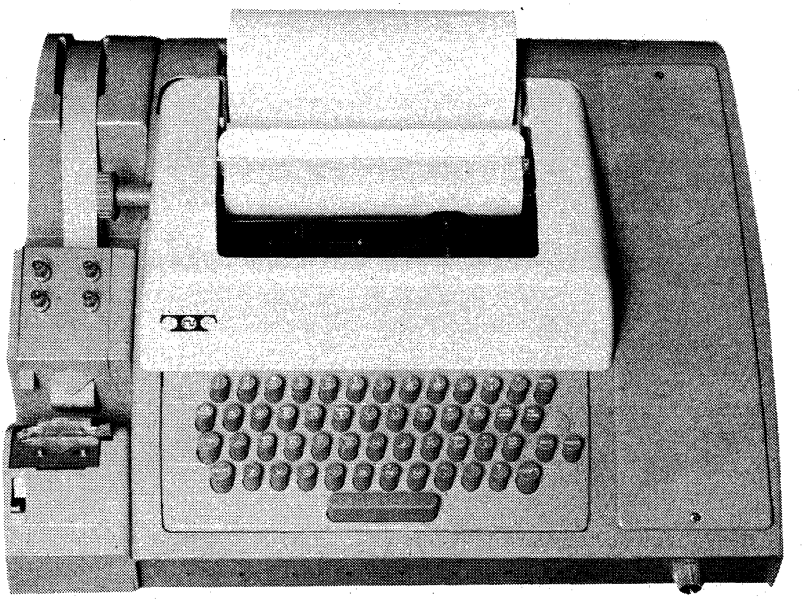
TELETYPE TERMINAL, LT33

DESCRIPTION

The LT33 Teletype can be used to type in or print out information, or to read in or punch out perforated paper tape. Printing, punching and reading are performed at rates of up to 10 characters per second. The DL11-A Teletype Control assembles or disassembles Teletype serial information for parallel transfer to, or from, the UNIBUS.

OPERATING THE TELETYPE

The LT33 Teletype is a basic input/output device for PDP-11 computers. It consists of a printer, keyboard, paper tape reader, and paper tape punch, all of which can be used either on-line under program control or off-line. The Teletype controls (see following figure) are described as they apply to the operation of the computer.



ASR-33 Teletype Console

Power Controls

LINE The Teletype is energized and connected to the computer as an input/output device, under computer control.

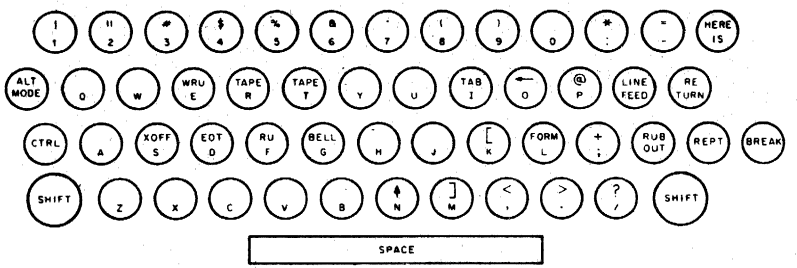
OFF The Teletype is de-energized.

LOCAL The Teletype is energized for off-line operation.

Printer
The printer provides a typed copy of input and output at 10 characters per second, maximum.

Keyboard
The Teletype keyboard is similar to a typewriter keyboard. However, certain operational functions are shown on the upper part of some of the keyboard tops. These functions are activated by holding down the CTRL key while depressing the desired key.

Although the left and right square brackets are not visible on the keyboard keytops, they are shown in the following figure and are generated by typing SHIFT/K and SHIFT/M, respectively. The ALT MODE key is identified as ESC (ESCape) on some keyboards.



ASR-33 Teletype Keyboard

Paper Tape Reader
The paper tape reader is used to read data punched on eight-channel perforated paper tape at a rate of 10 characters per second, maximum. The reader controls are described below.

START Activates the reader; reader sprocket wheel is engaged and operative.

STOP Deactivates the reader; reader sprocket wheel is engaged but not operative.

FREE Deactivates the reader; reader sprocket wheel is disengaged.

The following procedure describes how to properly position paper tape in the reader.

a. Raise the tape retainer cover.
b. Set reader control to FREE.
c. Position the leader portion of the tape over the read pens with the

sprocket (feed) holes over the sprocket (feed) wheel and with the arrow on the tape (printed or cut) pointing outward.

d. Close the tape retainer cover.
e. Make sure that the tape moves freely.
f. Set reader control to START, and the tape will be read.

Paper Tape Punch

The paper tape punch is used to perforate eight-channel rolled oiled paper tape at a maximum rate of 10 characters per second. The punch controls are described below.

RELease	Disengages the tape to allow tape removal or loading.
B.SP	Backspaces the tape one space for each firm depression of the B.SP button.
ON (LOCK ON)	Activates the punch.
OFF (UNLOCK)	Deactivates the punch.

Blank leader/trailer tape is generated by:

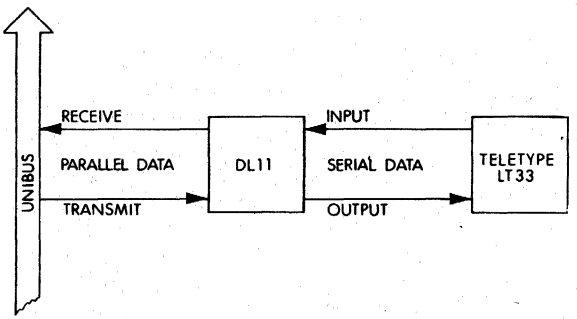
1. Turning the Teletype switch to LOCAL.
2. Turning the Punch ON.
3. Typing the HERE IS key.
4. Turning the Punch OFF.
5. Turning the Teletype switch to LINE.

TELETYPE CONTROL, DL11-A

The DL11 is a character-buffered communications interface that performs two basic operations: receiving and transmitting asynchronous data. When receiving data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the UNIBUS. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or the external device.

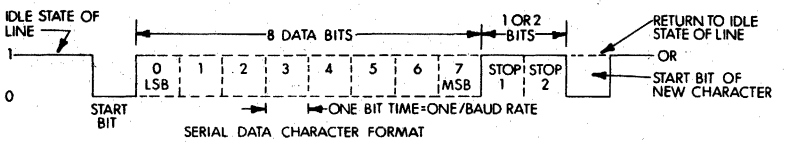
Operation

Signals transferred between the Teletype and the control logic are standard serial, asynchronous, 11-unit code signals. They consist of "marks" and "spaces" which correspond to bias and idle current in the Teletype serial line, and 1's and 0's in the control and computer. The 11-bit code consists of a start bit, 8 data bits, and 2 stop bits.



Teletype and Control, Block Diagram

Data Transfer	DL11	External Device
RECEIVE (from external device)	INPUT	Keyboard or Reader
TRANSMIT (to external device)	OUTPUT	Printer or Punch



The 10-bit code consists of a start bit, 8 data bits, and only 1 stop bit.

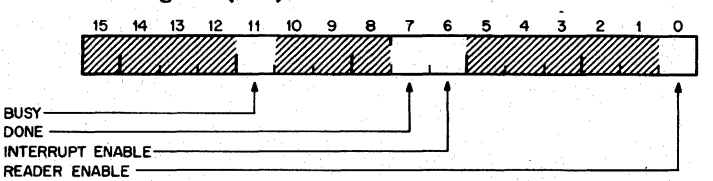
In addition to the LT33, the DL11-A can also be the control unit for a VT05 Alphanumeric Terminal, or an LA30-C serial DECwriter.

REGISTERS

The UNIBUS addresses mentioned in this section apply only when the Teletype is being used as the console terminal. When used in other applications, the addresses and vectors float, see Appendix A.

The DL11-A Teletype Control has 4 addressable registers.

Reader Status Register (TKS) 777 560

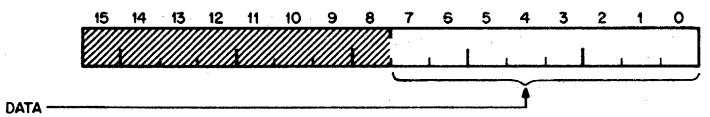


Effect of the Initialized (INIT) signal: clear all bits

Read only: bits 11 and 7
Write only: bit 0

BIT	NAME	FUNCTION
11	Busy	Set when receiving information. It is set by the start bit and is cleared by the leading edge of Done, bit 7.
7	Done	Set when a character is available in the Reader Data Buffer. It is cleared by any program reference to the Reader Data Buffer, or when Reader Enable, bit 0, is set.
6	Interrupt Enable	Set to allow Done = 1 to cause an interrupt.
0	Reader Enable	Set to allow the Paper Tape Reader (not keyboard) to read one character. It is cleared when a legitimate start bit is detected.

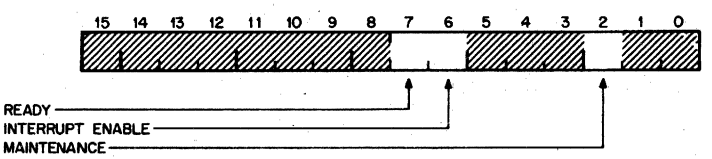
Reader Data Buffer (TKB) 777 562



Bits 7 through 0 hold the coded data for the character read. The register is double buffered. To the processor, the data is read only.

Any program reference to TKB (777 562 or 777 563) as a word or byte will clear Done, bit 7 of the Reader Status Register.

Punch Status Register (TPS) 777 564



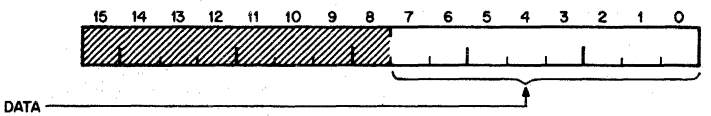
Effect of the Initialize (INIT) signal: clear bits 6 and 2, set bit 7

Read only: bit 7

BIT	NAME	FUNCTION
7	Ready	Set when the Punch is available to accept data. It is cleared when the Punch Data Buffer is loaded, and is set when another character can be loaded.

6	Interrupt Enable	Set to allow Ready = 1 to cause an interrupt.
2	Maintenance	Set to disable the serial line input from the Teletype (or terminal) and enable serial output of the Punch to feed into the Reader Data Buffer. It also forces the receiver to run at transmitter speed.

Punch Data Buffer (TPB) 777 566



Bits 7 through 0 hold the coded data for the character to be printed or punched. The bits are cleared by the Initialize signal. The register is double buffered. If a RESET instruction is given after a data message, a fill character (all zeroes) must be used as the last character to prevent losing the last character of data.

Any instruction that could modify TPB as a byte or word, clears Ready, bit 7 of the Punch Status Register. Other program reference has no effect on the Punch Registers.

Receiver
The Reader DONE flag (bit 7 in TKS) sets when the Universal Asynchronous Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the DONE flag.

Transmitter
The transmitter section of the UART is also double buffered. The Punch RDY flag (bit 7 in the TPS) is set after initialization. When the buffer (TPB) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

PROGRAMMING EXAMPLES
Reading a Character (from reader or keyboard):

```
READ:   INC TKS          ;SET RDR ENB
LOOP:   TSTB TKS         ;LOOK FOR DONE
        BPL LOOP         ;WAIT (BRANCH) IF DONE = 0
        MOVB TKB,R0      ;READ CHARACTER
```

Punching or Printing a Character

```
PUNCH:  TSTB TPS        ;TEST FOR READY
        BPL PUNCH       ;WAIT IF READY = 0
        MOVB R0,TPB     ;PUNCH CHARACTER
```

Echoing Keyboard

```
ECHO:   TSTB TKS        ;CHARACTER AVAILABLE?
        BPL ECHO        ;WAIT IF DONE = 0
LOOP:   TSTB TPS        ;IS PUNCH READY?
        BPL LOOP        ;WAIT IF READY = 0
        MOVB TKB,TPB    ;PUNCH CHARACTER
        BR ECHO         ;REPEAT FOR NEXT CHARACTER
```

Reading 10 Characters (by means of an interrupt)

```
START:  MOV #10,R0      ;SET UP COUNTER
        MOV #2000,R1    ;SET UP BUFFER POINTER
        MOV #101,TKS    ;SET INTR ENB AND RDR ENB
STALL:  BR STALL        ;HANG UP HERE UNTIL
                        ;BLOCK IS READ
        .
        .
        .
        .
        .
        .
60:     RDRINT          ;START OF READER SERVICE
                        ;ROUTINE
62:     000200          ;RAISE PROCESSOR TO PRIORITY
                        ;LEVEL 4
        .
        .
        .
RDPRINT: MOVB TKB,(R1)+ ;PUT CHARACTER INTO BUFFER
        DEC R0          ;DECREMENT COUNTER
        BEQ END         ;IF COUNT = 0, BRANCH TO END
        INC TKS         ;ENABLE READER AGAIN
        RTI             ;RETURN FROM INTERRUPT
END:    CLR TKS         ;CLEAR INT ENB
        TST(SP)+        ;POP RETURN ADDRESS
        MOV(SP)+,PS     ;RESTORE PROCESSOR STATUS WORD
        JMP STALL + 2   ;BACK TO PROGRAM
```

SPECIFICATIONS FOR LT33

Teleprinter

Printing speed:	10 char/sec
Number of columns:	72
Number of characters:	64

Reader/Punch

Storage medium:	8-hole paper tape
Reader speed:	10 char/sec

Punching speed:	10 char/sec
Data format:	8-bit characters

Mechanical

Mounting:	1 free-standing unit
Size:	34"H x 22"W x 19"D
Weight:	60 lbs

Power

Input current:	2 A at 115 VAC
Heat dissipation:	200 W

Environment

Operating temperature:	15°C to 35°C
Relative humidity:	20% to 80%

Models

LT33-DC: Teletype with KB, printer, paper tape rdr/punch, 115 VAC, 60 Hz
LT33-DD: Teletype with KB, printer, paper tape rdr/punch, 230 VAC, 50 Hz
LT33-CC: Teletype (without paper tape capability), 115 VAC, 60 Hz
LT33-CD: Teletype (without paper tape capability), 230 VAC, 50 Hz

SPECIFICATIONS FOR DL11-A (interfaced to LT33)

Usage: Control for LT33 Teletype

Register Addresses			Alternate Names	
Reader Status	(TKS)	777 560	Receiver Status	(RCSR)
Reader Buffer	(TKB)	777 562	Receiver Buffer	(RBUF)
Punch Status	(TPS)	777 564	Transmitter Status	(XCSR)
Punch Buffer	(TPB)	777 566	Transmitter Buffer	(XBUF)

UNIBUS Interface

Interrupt vector address:	60 (for keyboard/reader) 64 (for teleprinter/punch)
Priority level:	BR4 (keyboard has precedence over printer)
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot
Size:	quad module

Input current: 1.8 A at +5 V
0.15 A at −15 V

ELECTROSTATIC PRINTER/PLOTTER, LVII

DESCRIPTION

The LV11 high-speed Electrostatic Printer-Plotter provides quieter and more reliable operation than conventional impact printers and pen plotters, especially under heavy, continuous use. The entire ASCII character set (including upper- and lower-case alphabet) is printed in 132 columns per line at 500 lines per minute. The included control unit allows both printing and plotting, and accommodates most DIGITAL line printer software. In the plotting mode, the LV11 prints 122,880 dots per second (independent of picture complexity) with a resolution of 10 bits (1024 dots per line). The Printer-Plotter uses roll paper for continuous plots and printouts (up to 500 feet), or fanfold paper for easier handling.

The electrostatic printing technique employs a fixed writing head with 1024 addressable writing electrodes. As the paper passes over the writing head, any (or all) of the electrodes may be requested to deposit a charge on the coated paper. The charged paper then passes over a liquid toner containing carbon particles; the particles are attracted to the charged areas on the paper, causing the appearance of black dots.

The only moving parts in the LV11 are the paper-moving motor and a small toner pump—simplicity of design that guarantees long, trouble-free operation that more than offsets the small additional cost of the coated paper.

CONTROLS & INDICATORS

ON/OFF	Applies ac power to the LV11. When power is applied, the switch is illuminated and remains depressed. Depressing the switch a second time removes power from the unit.
PAPER ADVANCE	Depressing this switch causes paper to advance provided no data remains in the data buffer. The switch remains inoperative until the data is printed. Printing may be accomplished under computer control or by depressing the FORM FEED switch located just below the PAPER ADVANCE switch. Paper movement will continue until the switch is released.
FORM FEED	This switch causes the printer to enter a print cycle and print any data remaining in the data buffer. Upon completion of printing of the line, the paper is advanced to the top of the next page when using fanfold paper and the ROLL/FAN FOLD switch is in the FAN FOLD position, or for a distance of 2-1/2 inches when this switch is in the ROLL position.

LOW PAPER — This indicator is red in color and, when illuminated, indicates an out-of-paper condition in the printer. The LV11 will not accept data when this condition exists. An additional supply of paper should be loaded.

CONTRAST ADJUSTMENT — The contrast adjustment is located inside the front panel and is labeled DARK. Its purpose is to allow the operator to compensate for variations in contrast due to humidity changes in the atmosphere. It should be turned as far clockwise as necessary to permit high contrast writing without excessive background writing.

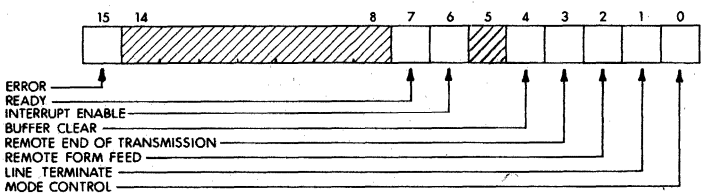
ROLL/FAN FOLD — This switch is located on the frame behind the front door. When this switch is in the ROLL position, the top-of-form detection circuit is disabled. The paper is advanced 2½ inches for an FF and 8 inches for an EOT. When in the FAN FOLD position, the printer commands are executed. Should this switch be placed in the FAN FOLD position when using roll paper, the top-of-form circuitry will be disabled following the first FF or EOT command. These commands will then be treated as an LF command when in print mode, or as a Line Terminate in the plot mode.

CAUTION

Should any of the manual controls be depressed while the LV11 is in operation, printing will be interrupted to perform the manual function indicated.

REGISTERS

Control and Status Register (LVCS) 777 514

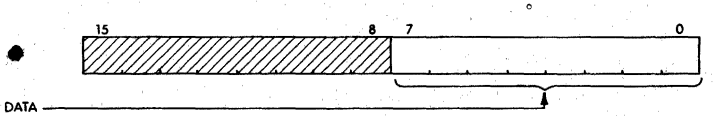


Effect of the Initialize (INIT) signal: clear bits 6 and 0

Read only: bits 15 and 7
Write only: bits 4 through 1

BIT	NAME	FUNCTION
15	Error	Set when an error condition exists in the printer. Error conditions are: 1. No Paper 2. Power off 3. No printer connected to control unit. This bit is reset only by manual correction of the error condition.
7	Ready	Set when the printer is ready to receive the next data transfer. Indicates that the previous function is either complete or has been started and continued to a point where the printer can accept the next data.
6	Interrupt Enable	Set to allow Ready or Error = 1 to cause an interrupt.
4	Buffer Clear	Set to clear the buffer indicated by the Mode Control bit.
3	Remote End of Transmission	Set to perform an EOT when in plot mode.
2	Remote Form Feed	Set to perform an FF when in the plot mode.
1	Line Terminate	Set to print the graphics line prior to receipt of a complete scan line.
0	Mode Control	Selects printer or plotter operation: 0 = printer, 1 = plotter.

Data Buffer Register (LVDB) 777 516



BIT	NAME	FUNCTION
7-0	Data	Eight-bit data buffer. Bits 6 to 0 contain the ASCII characters. Bit 7 is used only in the plot mode.

SPECIFICATIONS

Printing Specifications

Number of columns:	132
Number of characters:	96
Printing speed:	500 line/min
Type of printing:	electrostatic, 7 x 9 dot matrix
Vertical spacing:	8 lines/inch
Horizontal spacing:	12.5 char/inch
Memory:	one-line buffer (132 char)

Plotting Specifications

Plotting area:	10.24 sq inches
Total writing points:	1024
Vertical spacing:	100 lines/inch
Horizontal spacing:	100 points/inch
Input:	8-bit parallel bytes
Data transfer rate:	500,000 bytes/sec
Plotting speed:	122,880 dots/second
Memory:	one-line buffer (1024 bits)

Paper

Type:	roll, 11" wide x 500 ft long fanfold, 11" wide x 1000 sheets
Slew speed:	1.2 inches/sec

Register Addresses

Control and Status (LVCS)	777 514
Data Buffer (LVDB)	777 516

UNIBUS Interface

Interrupt vector address:	200
Priority level:	BR4
Bus loading:	1 bus load

Mechanical

Mounting:	1 free-standing unit + 1 SPC slot
Size:	38"H x 19"W x 18"D + quad module
Weight:	160 lbs

Power

Input current:	5 A at 115 VAC 1.5 A at +5 V (for control)
Heat dissipation:	600 W

Environment

Operating temperature:	10°C to 43°C
Relative humidity:	20% to 80%

Models

LV11-BA: Printer and control,	115 VAC, 60 Hz
LV11-BB: "	230 VAC, 50 Hz

CORE MEMORY

Core memory is available in basic increments of 8,192 words (8K). Core memory is a read/write, random access, coincident current memory with a cycle time of 900 nsec and an access time of 360 nsec. It is organized in a 3D, 3-wire (X, Y, & sense/inhibit) planar configuration using 18 mil magnetic cores. A stored word contains 16 bits. Each word contains two 8-bit bytes. All PDP-11 CPU's can handle either full word or byte addressing.

Options

The MM11-L is the basic unit of core memory. It contains 8K words, and mounts either in dedicated space within a CPU, or within an MF11-L or ME11-L. The MF11-L contains 8K of memory, but it also includes cables and a mounting assembly that can be expanded to 16K, 20K, or 24K. The mounting assembly occupies the space of 2 System Units (SU), but it is an integrated double SU that has 9 modules slots, instead of the 8 slots available from 2 separate SU's. Each 8K of memory uses 3 modules slots. The MF11-L cannot mount in the BA11-ES Extension Mounting Box, but in the sliding drawer assembly of a PDP-11/40 or 11/45 (or an H960-D cabinet).

The ME11-L is a completely self-contained core memory system. It is an MF11-L mounted in a 5¼" high box that includes a power supply to take care of the current requirements for 24K words. The ME11-L has chassis slides and mounts in a standard PDP-11 cabinet.

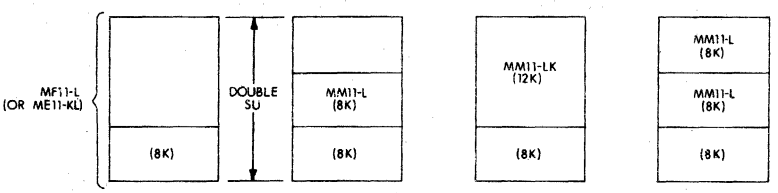
Other core memory options available include an MM11-S that has 8K words and mounts in a single System Unit; and an MM11-LK that has 12K of words of memory and uses the remaining space (6 modules slots) within an MF11-L or ME11-L.

CORE MEMORY SPECIFICATIONS

Access time:	360 nsec	
Cycle time:	900 nsec	
Word size:	16 bits (2 8-bit bytes)	
UNIBUS loading:	1 bus load per 8K	
Operating temperature:	0°C to 50°C	
Relative humidity:	10% to 90% (non-condensing)	
Power dissipation:	125 W per 8K	
Current requirements:	**+ 5V**	**− 15V**
8K words (active)	3.4 A	6.0 A
8K words (standby)	1.7	0.5

Model No.	Words	Mounting Space	Description
MF11-L	8K	2 SU	Includes a double system unit mounting assembly, expandable to 24K.
MM11-L	8K	(in MF11-L or ME11-L)	Memory expansion
MM11-LK	12K	(in MF11-L or ME11-L)	Memory expansion
MM11-S	8K	1 SU	Includes System Unit
ME11-LA	8K	panel mount, 5¼" high	Includes mounting assembly and power supply, expandable to 24K. Requires 5A at 115 VAC.
ME11-LB	8K	(same as ME11-LA, except requires 2.5A at 230 VAC)	

Core Memory Configurations



Word storage:	8K	16K	20K	24K
Bus loads:	1	2	3	3
Current at + 5V:	3.4 A	5.1 A	6.8 A	6.8 A
Current at — 15V:	6.0 A	6.5 A	7.0 A	7.0 A

PARITY CORE MEMORY

Parity core memory is available on the PDP-11/40 and 11/45 to check the integrity of stored data. A total of 18 bits are stored per word, with one parity bit per 8-bit byte. Odd parity is generated when writing to memory, and is checked when reading from memory. The 8 bits of each byte are checked for the number of 1's; if the number is even, a 1 is written into the parity bit to make the total number of 1's (byte plus parity) odd. When reading out, the 9 bits are checked for an odd number of 1's; if the number is even, an error is indicated.

Error Indication

Although parity is always monitored within the memory system, indication of a parity error to the CPU (or bus master) can be enabled or disabled under program control. Compared to nonparity core, access time increases by 125 nsec when Error Indication is enabled and 30 nsec

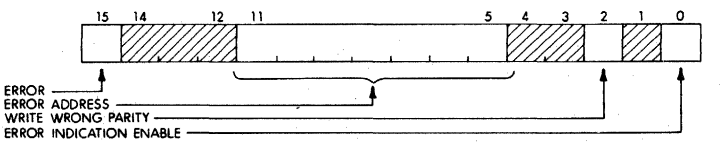
when disabled; the cycle time remains the same. If Error Indication is enabled, a parity error will cause the processor to enter a trap service routine through a vector at address 114.

Comparison

Parity core memory is similar to non-parity. Mounting space requirements are the same as the MM11-L 8K word sections. All the extra logic is contained on a double height module, called Parity Control. Only one control is needed per 24K parity words, and it fits within the same double System Unit space needed by the rest of the Memory System.

Parity and non-parity can be mixed in the same system, but not within the same physical mounting assembly. The MF11-L holds nonparity memory only, and the MF11-LP holds parity memory only.

Control and Status Register (CSR)



Effect of the Initialize (INIT) signal: clear bits 15, 2, and 0.

BIT	NAME	FUNCTION
15	Error	Set when a parity error occurs, even if Error Indication is not enabled.
11-5	Error Address	Contains the 7 highest order address bits (17 through 11) of the most recent location causing a parity error.
2	Write Wrong Parity	Diagnostic aid to force a parity error. Set to cause the controller to generate incorrect parity on write cycles (DATO or DATOB), forcing a parity error on the next read cycle (DATI or DATIP) to the same location.
0	Error Indication Enable	Set to enable error indication on the UNIBUS.

There is one CSR per 24K of parity core memory. The address of the CSR is in the range 772 100 to 772 136. The address to be used depends on where the parity memory is placed in memory address space.

PARITY CORE MEMORY SPECIFICATIONS

Access time:	485 nsec, error indication enabled 390 nsec, error indication disabled
Cycle time:	900 nsec
Word size:	18 bits (includes 2 parity bits, 1 per byte)
Parity:	Odd
Control and Status Register	
Trap vector address:	114
CSR addresses:	772 100 to 772 136
UNIBUS loading:	1 bus load per 8K 1 bus load for Parity Control (each 24K)

Current requirements:

	+ 5V	− 15V
8K words (active)	3.6 A	6.5 A
8K words (standby)	1.8	0.6
Parity Control	1.2	

Model No.	Words	Mounting Space	Description
MF11-LP	8K	2 SU	Parity memory, includes a double system unit, parity control and space for 24K total parity memory
MM11-LP	8K	(in MF11-LP)	Parity memory expansion

Words	Options	Bus Loads	+ 5V	− 15V	Mounting Space
8K	MF11-LP	2	4.8 A	6.5 A	2 SU
16K	MF11-LP + MM11-LP	3	6.6	7.1	2
24K	MF11-LP + (2) MM11-LP	4	8.4	7.7	2

SEMICONDUCTOR MEMORY

To take advantage of the superior performance of the PDP-11/45, bipolar and MOS semiconductor memories are offered. These faster memories allow obviously faster computer processing, and are especially useful in storing often used data and instructions. Semiconductor memory plus clever programming can yield much improved performance and reduced throughput time.

Provision is made for semiconductor memory as an integrated part of the PDP-11/45. A dedicated, pre-wired area within the main CPU assembly is provided. All necessary interfacing and power have been arranged. Configuration optimization has already been performed.

The PDP-11/45 can handle a maximum semiconductor memory size of:

a) 8K words of bipolar, or
b) 32K words of MOS, or
c) 4K words of bipolar plus 16K words of MOS

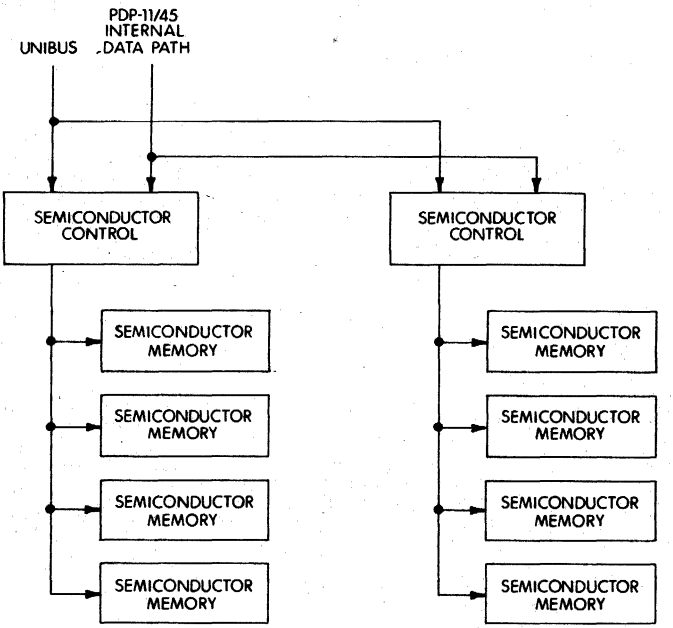
The semiconductor read/write, random access memory is available with parity. There would be one parity bit per 8-bit byte.

Bipolar memory is the fastest type offered; it has an access time of 200 nsec and a cycle time of 300 nsec. MOS is a little slower, but it offers higher packaging density. It has an access time of 350 nsec and a cycle time of 450 nsec. When semiconductor memory is read, the contents are not destroyed, so that information does not have to be restored as with core memory. This markedly decreases the cycle time.

Interface to the PDP-11/45
In addition to the standard UNIBUS, the PDP-11/45 has an internal data path that is connected to Semiconductor Memory for faster transfers and performance. Actually, Semiconductor Memory contains two ports, so that it can be connected to both buses at the same time. Access control would be shared.

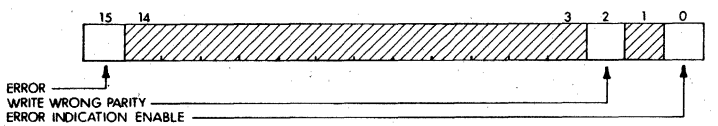
Options
Semiconductor Memory consists of two parts; a Semiconductor Memory Control and the units of Semiconductor Memory themselves. A maximum of two controls can be used with any single processor. Each control can handle up to 4K of bipolar or 16K of MOS. Semiconductor Memory is available in increments of 1K for bipolar and 4K for MOS.

Parity on Semiconductor Memory
There is one Control and Status Registers (CSR) per Semiconductor Control when parity memory is implemented. (Maximum of 2 CSR's in a system). The addresses of the CSR's are in the range 772 100 to 772 136.



Block Diagram of Semiconductor Memory System

Control and Status Register (CSR)



Effect of the Initialize (INIT) signal: clear all bits

BIT	NAME	FUNCTION
15	Error	Set when a parity error occurs, even if Error Indication is not enabled.
2	Write Wrong Parity	Diagnostic aid to force a parity error. Set to cause the control to generate incorrect parity on write cycles, forcing a parity error on the next read cycle to the same location.
0	Error Indication Enable	Set to enable error indication.

If Error Indication is enabled, a parity error will cause the processor to enter a trap service routine through a vector at address 114.

There is no increase in mounting space requirements with parity semiconductor memory. The same semiconductor control (MS11-CC, MS11-BC, or MS11-BD) is used, with or without parity.

SEMICONDUCTOR MEMORY SPECIFICATIONS (PDP-11/45 only)

	Bipolar	**MOS**
Access time:	200 nsec	350 nsec
Cycle time:	300 nsec	450 nsec
Word size:	16 bits (18 bits with parity)	
Memory increments:	1K words	4K words
Max memory size:	8K words of bipolar,	
	or 32K words of MOS,	
	or 4K words of bipolar and 16K of MOS	
Control and Status Register (parity only)		
Trap vector address:	114	
CSR addresses:	772 100 to 772 136	
UNIBUS loading:	1 bus load per control (max of 2 controls)	
Operating temperature:	0°C to 50°C	
Relative humidity:	10% to 80%	

Model No.	**Type**	**Description**
MS11-CC	bipolar	Control for 1 to 4 bipolar memories
MS11-CM	bipolar	1K memory
MS11-CP	bipolar	1K memory, with parity
MS11-BC	MOS	Control for 1 to 4 MOS memories, first group
MS11-BD	MOS	Control for 1 to 4 MOS memories, second group
MS11-BM	MOS	4K memory
MS11-BP	MOS	4K memory, with parity

HIGH SPEED PAPER TAPE READER/PUNCH PC11

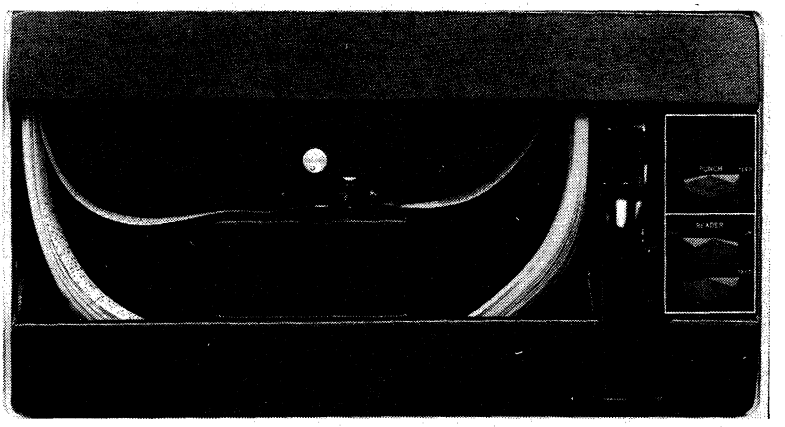
DESCRIPTION

The PC11 High Speed Reader & Punch is capable of reading eight-hole unoiled perforated paper tape at 300 characters per second, and punching tape at 50 characters per second. The system consists of a Paper Tape Reader/Punch and Control. A unit containing a reader only (PR11) is also available.

Operation

In reading tape, a set of photodiodes translate the presence or absence of holes in the tape to logic levels representing I's and O's. In punching tape, a mechanism translates logic levels representing I's and O's to the presence or absence of holes in the tape. Any information read or punched is parallel-transferred through the Control. When an address is placed on the UNIBUS, the Control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses have been selected, the Control determines whether an input or an output operation should be performed. An input operation from the reader is initiated when the processor transmits a command to the Paper Tape Reader Status register. An output operation is initiated when the processor transfers a byte to the Paper Tape Punch Buffer Register.

The Control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch, either device can be under direct program control or can operate without direct supervision through the use of interrupts, to maintain continuous operation.



High-Speed Paper Tape Reader/Punch

Paper tape is loaded into the reader as explained below.

1. Raise tape retainer cover.
2. Put tape into right-hand bin with channel one of the tape toward the rear of the bin.
3. Place several folds of blank tape through the reader and into the left-hand bin.
4. Place the tape over the reader head with feed holes engaged in the teeth of the sprocket wheel.
5. Close the tape retainer cover.
6. Depress the READER FEED button until leader tape is over the reader head.

CAUTION

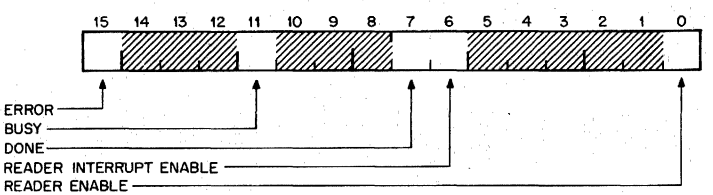
Oiled paper tape should not be used in the high-speed reader or punch. Oil collects dust and dirt which can cause reader or punch errors.

SWITCHES

PUNCH FEED		Punch leader tape.
READER	ON LINE	Allow reading of tape.
	OFF LINE	Disable reading of tape.
READER FEED		Manual feeding of tape through read station.

REGISTERS

Papertape Reader Status Register (PRS) 777 550



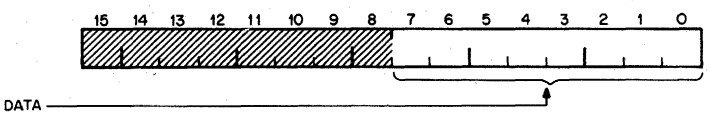
Effect of the Initialize (INIT) signal: clear bits 11, 7, and 6

Read only: bits 15, 11, and 7
Write only: bit 0

BIT	NAME	FUNCTION
15	Error	Set when an error occurs; no tape in reader, reader is off-line, or reader has no power.

11	Busy	Set when a character is being read. It is set when Reader Enable is set, and cleared when the present operation is complete (Done is set).
7	Done	Set when a character is available in the Reader Data Buffer. It is cleared by any program reference to the Reader Data Buffer, or by setting Reader Enable.
6	Interrupt Enable	Set to allow Error or Done = 1 to cause an interrupt.
0	Reader Enable	Set to allow the Reader to fetch one character. The setting of this bit clears Done, sets Busy, and clears the Reader Buffer (PRB). Operation of this bit is disabled if Error = 1; attempting to set it when Error = 1 will cause an immediate interrupt if Interrupt Enable = 1.

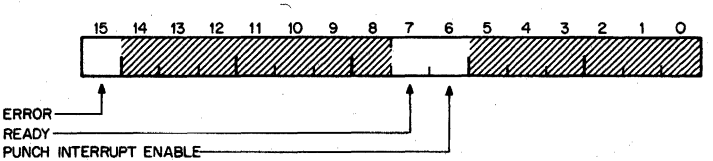
Papertape Reader Buffer (PRB) 777 552



Bits 7 through 0 hold the coded data for the character read. The bits are cleared when Reader Enable, bit 0 of PRS, is set. To the processor, the data is read only.

Any program reference to PRB (777 552 or 777 553) as a word or byte will clear Done, bit 7 of PRS.

Papertape Punch Status (PPS) 777 554



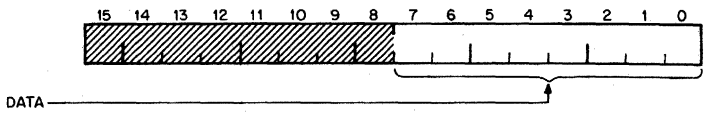
Effect of the Initialize (INIT) signal: clear bit 6, set bit 7

Read only: bits 15 and 7

BIT	NAME	FUNCTION
15	Error	Set when an error occurs; no tape in punch, or punch has no power.

7	Ready	Set when ready to punch a character. It is cleared when the Punch Buffer is loaded, and is set when punching is done.
6	Interrupt Enable	Set to allow Error or Ready = 1 to cause an interrupt.

Papertape Punch Buffer Register (PPB) 777 556



Bits 7 through 0 hold the coded data for the character to be punched. To the processor, the data is write only.

Any instruction that could modify PPB as a word or byte, clears Ready (bit 7 of PPS) and initiates punching. An immediate interrupt will occur when punching is initiated if Error = 1 and Interrupt Enable = 1.

PROGRAMMING

Program Control of the Reader

The sequence of instructions that follows reads one byte from the paper tape and deposits it in general register 0. If a reader error is sensed, the program branches to an error routine, which may type out a message and then wait for operator intervention.

```
READ:  INC   PRS          ;SET RDR ENB
LOOP:  TST   PRS          ;LOOK FOR ERROR
       BMI   ERR          ;BRANCH ON ERROR = 1
       TSTB  PRS          ;LOOK FOR DONE
       BPL   LOOP         ;WAIT IF DONE = 0
       MOV   PRB, R0      ;READ CHARACTER
```

A shorter form of the test loop is possible, as shown below:

```
READ:  INC   PRS
LOOP:  BIT   #100200, PRS ;TEST BITS 15 AND 7
       BEQ   LOOP         ;WAIT IF NO BITS SET
       BMI   ERR          ;ERROR IF BIT 15 SET
       MOV   PRB, R0      ;IF BIT THAT IS SET IS NOT BIT 15,
                          ;MUST BE BIT 7
```

Reader Interrupt Service

The PDP-11 System can combine PC11 operations with other processing by using the interrupt mode of device operation. When a device operation has been initiated, the PC11 continues without supervision until the operation is complete (or an error occurs); the remainder of the PDP-11 System is free to perform other operations. When the PC11 Control requires further service, the processor is notified by an interrupt.

The program that follows can be used to read a block of 128 characters from the paper tape to a buffer.

```
START:   MOV #-200,R0          ;INITIALIZE COUNTER
         MOV #101,PRS          ;SET INTR ENB AND RDR ENB
HANG:    BR HANG               ;HANG UP HERE UNTIL BLOCK IS
                               ;READ
70:      RDRINT                ;VECTOR TO INTERRUPT ROUTINE
72:      200                   ;SETS STATUS TO PRIORITY 4
RDRINT:  TST PRS               ;TEST FOR ERROR
         BMI ERR               ;TYPE OUT MESSAGE IF ERROR
         MOVB PRB,BUFEND(R0)   ;FILL BUFFER STARTING AT BUF-
                               ;END-200(OCTAL)
         INC R0                ;COUNT ONE BYTE AND MOVE
                               ;POINTER
         BEQ OUT               ;WHEN COUNT IS ZERO, EXIT
                               ;LOOP
         INC PRS               ;ENABLE READER AGAIN
         RTI                   ;RETURN FROM INTERRUPT
OUT:     ADD #4,SP             ;UNSTACK INTERRUPT PC AND PS
         CLR PRS               ;INHIBIT FURTHER INTERRUPTS
         JMP HANG + 2          ;CONTINUE MAIN PROGRAM
```

NOTE

The position of the buffer used by this program is specified by the end of the buffer, not the beginning. The indexed address uses the negative counter values to access bytes at decreasing distances from this base address.

Two operations performed by this program require caution. When a program accesses the same or contiguous locations, the program operating speed increases if the locations are addressed through a register. If this is done either no other use can be made of this register or: a) the interrupt service routine must stack the former contents of the register, b) the counter must be moved from a temporary storage location to the register, c) the register must be used, and d) the storage operations reversed. In this example where the processor does not do any other processing, no conflicts with the use of the register occur.

A second caution refers to the terminating exit from the service routine. When the exit does not occur through an RTI instruction, the main pro-

gram PC (Program Counter) and PS (Processor Status) words that are stacked by the interrupt must be removed from the stack. The ADD instruction at OUT performs the operation. If this operation is not performed, the values stacked by other operations previous to the interrupt are not properly accessible.

Punch Programmed Service
The sequence of instructions that follows transfer one byte from register 0 to the paper tape. When controlling the punch, the READY bit of the PPS register is checked before the transfer; when controlling the reader, the DONE bit of the PRS register is checked after a command.

```
PUNCH:  BIT #100200,PPS     ;CHECK PUNCH STATUS
        BEQ PUNCH           ;IF NOT READY OR ERROR, WAIT
        BMI ERROR           ;PROCESS ERROR IF ANY
        MOV R0,PPB          ;OUTPUT CHARACTER
```

Punch Interrupt Service
This interrupt service routine outputs 8-bit codes to the paper tape, unless they are ASCII representations of the formatting characters Line Feed, Rubout, or Form Feed. Line Feeds and Rubouts are ignored (not punched), and the program stops punching when the character read from the buffer is a Form Feed. The Form Feed is not punched. The program transfers the contents of a buffer: a) starting at a preselected address to paper tape, b) stopping automatically when it reads an end-of-buffer character, and c) performing simple character editing.

The interrupt service routine is called into operation when the following sequence of instructions is encountered in the main program:

```
R0 = %0                 ;REGISTER ZERO
SP = %6                 ;REGISTER SIX
PC = %7                 ;REGISTER SEVEN
PS = 777776             ;PROCESSOR STATUS WORD
CLR PUNDON              ;CLEAR SOFTWARE FLAG
MOV #BUFFER,POINTER     ;SET UP BUFFER POINTER
MOV #100,PPS            ;SET PUNCH INTR ENB
```

This instruction sequence sets up the system by initializing the service routine and enabling interrupts from the punch.

If the punch is idle, an interrupt occurs immediately; otherwise, the first interrupt is delayed until the current operation is completed. The software flag is used by the main program to provide a check on the progress of the output. This occurs in the following manner: The main program continues with other processing until the use of the punch is re-

quired, or further processing is dependent on completion of the output. At this point the sequence of instructions shown below is executed.

```
LOOP:  TST PUNDON      ;CHECK SOFTWARE FLAG
       BPL LOOP
```

If the interrupt service routine has not set the flag, the processor stays in this wait loop, allowing interrupts for further output operations, until the routine signals that it is finished.

In this example, the interrupt routine to service the punch requires the following sequence of instructions:

```
74:      PCHINT          ;VECTOR TO ROUTINE
76:      200             ;NEW STATUS WORD
PCHINT:  MOV R0,-(SP)    ;SAVE REGISTER ZERO
         MOV POINTER,R0  ;SETUP REGISTER
         TST PPS         ;CHECK NO ERRORS
         BMI ERROR       ;IF ERROR, EXIT WITH LAST BUFFER
                         ;POSITION IN R0
RETEST:  CMPB (R0),#212  ;LINE FEED?
         BNE TEST2       ;NO, CONTINUE
         INC R0          ;YES, IGNORE CHARACTER
         BR RETEST       ;AND TEST NEXT CHARACTER
TEST2:   CMPB (R0),#377  ;RUBOUT?
         BNE TEST3       ;NO, CONTINUE
         INC R0          ;YES, IGNORE
         BR RETEST
TEST3:   CMPB (R0),#214  ;FORM FEED?
         BEQ OUT         ;YES, EXIT
         MOVB (R0)+,PPB  ;NO, OUTPUT CHARACTER
         MOV R0,POINTER  ;SAVE REGISTER
         MOV (SP)+,R0    ;UNSTACK PREVIOUS CONTENTS
         RTI             ;NORMAL RETURN
OUT:     MOV (SP)+,R0    ;RESTORE TO PREVIOUS STATUS
         COM PUNDON      ;SET SOFTWARE FLAG
         CLR PPS         ;CLEAR INT ENB
         RTI
```

POINTER: 0

PUNDON: 0

SPECIFICATIONS

Main Specifications

Storage medium:	8-hole paper tape, unoiled
Reader speed:	300 char/sec
Punch speed:	50 char/sec
Paper type:	fanfold
Data format:	8-bit characters

Register Addresses

Reader Status (PRS)	777 550
Reader Buffer (PRB)	777 552
Punch Status (PPS)	777 554
Punch Buffer (PPB)	777 556

UNIBUS Interface

Interrupt vector address:	70 (for reader) 74 (for punch)
Priority level:	BR4 (reader has precedence over punch)
Bus loading:	1 bus load

Mechanical

Mounting:	1 panel mounted unit + 1 SPC slot
Size:	10½" front panel height + quad module
Weight:	50 lbs

Power

Input current:	3 A at 115 VAC 1.5 A at +5 V
Heat dissipation:	350 W

Environment

Operating temperature:	13°C to 38°C
Relative humidity:	20% to 95%

Models

PC11:	Reader/punch and control, 115 VAC, 60 Hz
PC11-A:	" , 230 VAC, 50 Hz
PR11:	Reader and control
H722:	Transformer (required for 230 VAC, 50 Hz operation of PC11-A or PR11)

DEC DISK, RC11

DESCRIPTION

The RC11 is a fast, low-cost, random access, bulk storage system. An RC11 provides 65,536 16-bit words of storage. Up to four RS64 disks can be controlled by one RC11 Control for a total of 262,144 words of storage. Disk functions include: look ahead, read, write, and write check, as well as a "look ahead" register which indicates current disk position. An RC11 includes a Control Unit and the first Disk Drive.

Operation

The disk stores data in a 32 x 16-bit word block format. Cyclic Redundancy Check (CRC) error detection is performed automatically by the Control on a block basis, the blocks being randomly addressable. A self-synchronizing, phase-lock clock recovery system is used to ensure exceptional data reliability. This technique facilitates data recovery in the event of restart after a power failure or during periods of high shock or vibration.

Fast track switching time permits spiral read and write. Data may be read or written as 32-word blocks. From 1 to 2,048 blocks can be accessed at a time. When the last address on a track or surface has been used, the Control will automatically advance to the next track or to the first track of a new disk surface.

Each RS64 disk unit has a set of switches for Write protecting the disk. The Write Lock ENABLE/DISABLE switch determines whether protection is desired or not. If this switch is in ENABLE position, writing data on tracks selected by five switches is not allowed. The setting of five switches below the ENABLE/DISABLE switch forms a binary number that corresponds to the number of a track; when write protection is in effect, all tracks numbered from zero to the selected number (both inclusive) are write protected. Any attempt to write in a write protected area will result in an error indication by the Control.

There are 3 timing tracks plus 3 spare (pre-recorded) that can be used for data recovery if primary timing tracks are lost.

Real-time look ahead is provided by the Control for the processor. This feature lets the processor continuously monitor the current position of the disk and minimize latency.

CONTROLS

Power Controls

Each RS64 Disk Unit has a circuit breaker to control the application of primary power and a three position (REMOTE/OFF/LOCAL) slide switch to turn on the logic power. In general, the main circuit breaker is left in the ON position with the power cord plugged into an uninterrupted ac outlet to run the motor. The slide switch is left in the REMOTE position to allow application of logic power when the PDP-11 is turned on through the remote power control circuit.

Write Protection Facilities

Each RS64 Disk Unit has a set of write lock switches mounted on the back. The WRITE LOCKOUT ENABLE/DISABLE switch determines whether any of the tracks are protected from write access. If this switch is in the ENABLE position, the RS64 Unit prohibits the transfer of data to tracks selected by the five write lock switches, but allows transfers of data from any track. That is, any data track may be read, but only tracks that are not write locked may be written.

The settings of the five write lock switches form a binary number that corresponds to the number of a track. When the write lock function is enabled, all tracks numbered from 0 to the selected number, inclusive, are protected from write access. For example, if the switches are set to 00111, eight tracks numbered from 0 to 7 (track numbers are in octal) are write locked, and 24 tracks numbered from 10_8 to 37_8 are write enabled. If the WRITE LOCKOUT ENABLE/DISABLE switch is in the DISABLE position, all 32 tracks numbered from 0_8 to 37_8 are write enabled.

Unit Number Assignment

Each disk unit has an assigned number and a five-position unit select switch (see Figure) that is used to set up this number assignment. A disk unit may have one of four unit numbers (numbered 0-3) or may be off-line, that is, not responding to any unit number.

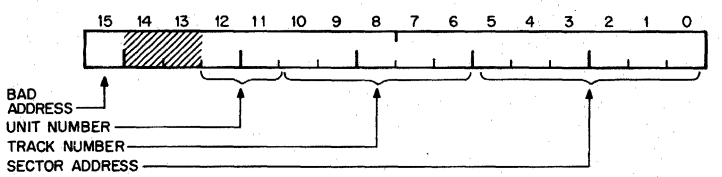
When the RC11 Control asserts a unit select signal, any disk unit that has been set to that unit number responds. The RC11 Control cannot respond to a number if multiple RS64 Units are assigned the same unit number. This situation must be avoided for proper operation of the disk system.

REGISTERS

Look Ahead Register (RCLA) 777 440

This register always points to the sector address currently passing under read/write heads. Track number and unit numbers are copied from the disk address register (RCDA) into this register. RCLA is a real time register and the controller constantly updates it with new sector address read from the disk at appropriate times.

In order to insure that its contents do not change while being read by the processor the controller may skip updating RCLA when necessary. All sector address codes recorded on the disk are sequential and should appear in RCLA sequentially. However, if the time of update happens to coincide with the time of reading this register, the controller will skip updating and will correct itself at the next sector.



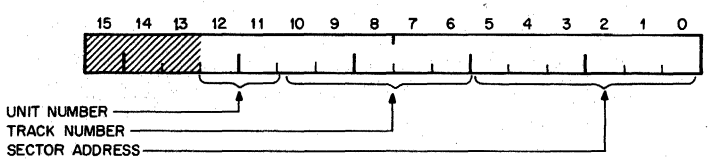
Effect of the Initialize (INIT) signal: clear bits 12 through 6.
Read only: all bits

BIT	NAME	FUNCTION
15	Bad Address	Set at the time of sector address update if unit or track switching is in progress or an address error is encountered. RC11 takes approximately 8 milliseconds to switch from unit to unit and 300 microseconds to switch from track to track on a unit.
12-11	Unit Number	Selects 1 of 4 disk units. BIT 11 — BIT 12 — UNIT 0 — 0 — 0 1 — 0 — 1 0 — 1 — 2 1 — 1 — 3 These bits are same as RCDA 12-11.
10-6	Track Number	Indicates which of the 32 tracks on currently selected disk is active. These bits are identical to RCDA 10-6.
5-0	Sector Address	Indicates the sector address just read from the selected disk.

Disk Address Register (RCDA) 777 442

Before any transfer between UNIBUS and RS64, RC11 must select and confirm a particular area on the disk. Each disk surface is divided into 64 sectors. Each sector has 32 data words. The disk address register is loaded with a number that selects one of four disk units, specific track and sector for transfer. To effect those transfers which require more than one sector, RCDA is incremented automatically after each sector has been transferred. After the last sector of a track $(77)_8$ has been operated on, first sector (sector 0) of the next track is selected due to incrementing. In a similar fashion after the last sector of the last track (track 37_8), first sector on the first track (track 0) of the next unit is selected automatically.

The program can specify or the Control may increment to a nonexistent disk unit. Response of the controller to such a situation is in the command and status register, RCCS.

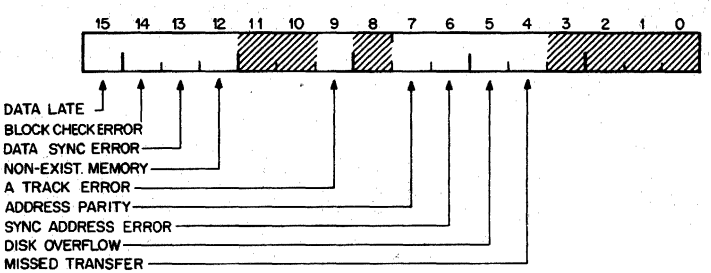


Effect of the Initialize (INIT) signal: clear all bits.

BIT	NAME	FUNCTION
12-11	Unit Number	Selects 1 of 4 disk units. Unit number is incremented by track number overflow. Unit number overflow sets disk overflow condition and indicates a non-existent disk status in RCCS if the word count did not overflow, i.e., desired number of transfers are not complete. This prevents wraparound transfers from disk 3 to disk 0.
10-6	Track Number	These bits are transmitted to the disk units for selecting a track; the track number is incremented by sector address overflow. When track number overflows, unit number in RCDA 12-11 is incremented.
5-0	Sector Address	Specifies a sector for transfers. After the sector has been transferred RCDA is incremented. Sector address overflow increments track number in RCDA 10-6.

Disk Error Status Register (RCER) 777 444

This register indicates error conditions that result from improper programming or equipment malfunction. When error conditions are sensed by the controller, any current operation in progress is aborted at appropriate time. This will cause an interrupt if interrupt enable bit (RCCS 6) is set. All error bits in this register are read only and cleared when a new RC11 operation is started. Initialize also clears this register.

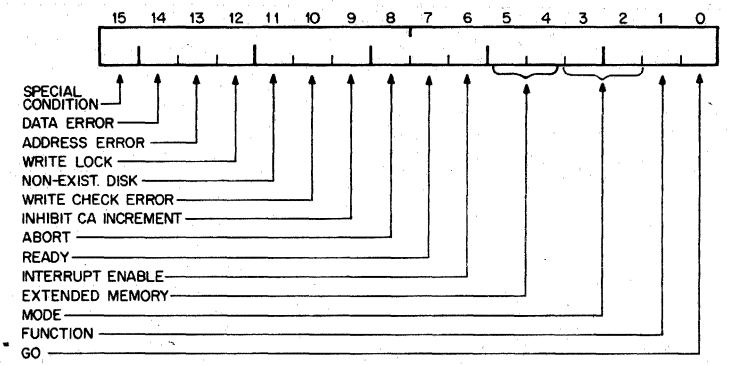


BIT	NAME	FUNCTION
15	Data Late (DRL)	RC11 requests control of the UNIBUS to conduct transfers. Such requests are made for each word. If, for any reason, request is not granted in time and RC11 requests another transfer, then this bit is set to indicate loss of data. Because RC11 operates on block structured data,

		word count and current address registers must be reinitialized and transfer restarted at the beginning of the sector.
14	Block Check Error	Set if the cyclic redundancy check (CRC) that is read back from the disk does not agree with the computed check on the data just read.
13	Data Sync. Error	Data formats on RC11 are chosen such that data block occurs between two markers on the mark track; data mark should be sensed first on mark track and data for that block should be complete before sensing an address mark on mark track. This bit is set if a violation is sensed by the controller.
12	Non-Existent Memory (NEM)	Set if RC11 initiates a UNIBUS data transfer and does not receive a slave sync. signal within a predetermined time after it asserted Master sync. This condition usually indicates no register or memory has been assigned to that address.
9	A Track Error	RS64 unit employs NRZI recording technique that can be used to determine if a bit has been lost or extra bit read. If this happens on the clock track (A-track) then bit is set.
7	Address Parity	Set to indicate parity failure of the sector address code.
6	Address Sync	Set to indicate that a data mark signal from Mark track is received and the controller still has not detected end of sector address assembly. This situation may be due to missing the sync mark which precedes all sector address codes or spurious response from the Mark track.
5	Disk Overflow	If the disk address register (RCDA) overflows, the unit number changes from 3 to 0. This bit is set to indicate this situation. If word count overflow did not occur (i.e. more data transfers are to be made), this bit will also indicate nonexistent disk (NED) condition by setting bit 11 in RCCS.

4	Missed Transfer	Set to indicate that RC11 did not make a non-processor request for data transfer since initiating a function and the disk revolved more than once.

Disk Control and Status Register (RCCS) 777 446



Effect of the Initialize (INIT) signal: clear bits 14 through 8, and 6 through 0; set bit 7

Read only: bits 15 through 10, 7
Write only: bits 8 and 0.

BIT	NAME	FUNCTION
15	Special Condition	Set to indicate that controller sensed an error condition. The exact error causing this bit to set can be found in bits 10-14 of this register and RCER.
14	Data Error	Set to indicate that controller sensed a data error. Data error may be due to sync or cyclic redundancy check (CRC). The exact error can be found in RCER.
13	Address Error	Set to indicate that controller sensed an address parity or sync error. The exact error can be found in RCER.
12	Write Lock	Set to indicate that a write attempt was made on a write-protected area of the disk.
11	Non-Existent Disk	Set to indicate that disk address register (RCDA) is pointing to a non-existent unit or the disk unit number in RCDA has overflowed. Note that this bit will be "1" only

		when the word count register did not overflow so that last sector of the last disk unit can be operated on without getting an error status.
10	Write Check Error	Set if data read from the disk does not compare with the data on the bus during a write check function. Incrementation of RCCA and RCWC are inhibited as soon as failure occurs. However, controller reads the whole block (32 words) for cyclic redundancy check (CRC).
9	Inhibit CA Increment	If set, data transfers with the UNIBUS will be performed without incrementing RCCA.
8	Abort	If set, any operation in progress is aborted.
7	Ready	Controller sets this bit to indicate completion (or abortion) of an operation and is ready for the next operation.
6	Interrupt Enable	Set to allow a program interrupt.
5-4	Extended Memory	Two most significant bits when 18 bit address is in effect. These two bits are logical extension of the current address register (RCCA).
3	Mode	If set, controller switches to maintenance mode. Signals received from RS64 are inhibited from activating the controller. Instead these signals will be taken from RCMN.
2-1	Function	Specify the desired operation. Controller decodes these bits as follows:

Bit 2	Bit 1	Function
0	0	Look Ahead
0	1	Write
1	0	Read
1	1	Write Check

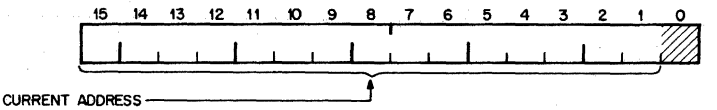
0	Go	Set to initiate the function specified.

Word Count Register (RCWC) 777 450

Before an RC11 operation begins, the word count register is loaded with the 16-bit 2's complement negative value corresponding to the number of words to be transferred or checked. After each UNIBUS transfer, the RC11 Control increments the RCWC register; when the register overflows, no further UNIBUS transfers occur, but the RC11 continues the operation to the end of the current block to read or write the block check, or CRC word. These bits are read/write, and are cleared by

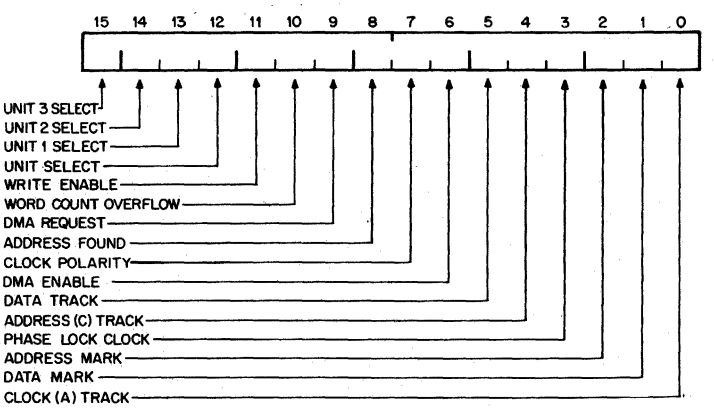
initialization. The RCWC is normally clear (contains 0) at the termination of an operation, but if the operation is stopped by an error or an abort, the RCWC may be nonzero.

Current Address Register (RCCA) 777 452



Before initiating an RC11 function the program declares the address of the UNIBUS location where the Control should start data transaction. All data transfers take place at even address boundaries (no byte capability). After each data transfer this register is incremented by two. When this register overflows, extended memory bits in RCCS are incremented. Bit 0 of this register is not used and remaining bits are read/write. Initialization clears this register.

Maintenance Register (RCMN) 777 454



This register is provided for diagnostic purposes only and does not participate in normal disk operations.

The maintenance register provides indicators and control signals used to test the Control without using a Disk. All the signals that communicate between the Disk and the Control are simulated by logic within the Control or by inputs through the maintenance register. Time-out logic is disabled to allow a slow simulation, and the response to UNIBUS transfer is altered to allow examination of the registers during operation. Bits 6 and 7 of the maintenance register are buffered and provide a level when loaded; the rest of the bits provide a pulse when loaded with 1.

BIT	NAME	FUNCTION
15-12	UNIT SELECT 3-0	Indicates the state of the four unit select lines on the RS64 Bus. These bits are read-only and always reflect the state of the signal lines.
11	WRITE ENABLE	Indicates the state of the write enable line on the RS64 Bus. During maintenance mode this bit appears to be on the bus but is not active to preserve data. If the bit is a 1, the RC11 Control is attempting to write on the selected disk. This bit is read-only.
10	WORD COUNT OVERFLOW	Indicates when the word count register (RCWC) overflows; it is set by the carry out of RCWC15. This bit is read-only; it is cleared by initialization.
9	DMA REQUEST	Set when the RC11 Control requires a UNIBUS data transfer and is ready to assert an NPR signal. When the RC11 is in maintenance mode (RCCS3 is set), the ENABLE DMA bit (maintenance register bit 6) must be set to allow the UNIBUS transfer. This bit is read-only; it is cleared by initialization.
8	MATCH FOUND	Set when the RC11 determines that the unit and track selections are valid and that the selected sector is passing under the read/write head. This bit is read-only.
7	CLOCK POLARITY	Simulates the RS64 CLK P signal when the MAINTENANCE bit (RCCS3) is set. The bit must be toggled in. This signal is used by the RC11 to detect missing or extra pulses in the RS64 CLK signal, which is simulated by maintenance register bit 0. This bit is read/write; it is cleared by initialization.
6	ENABLE DMA REQUEST	Used to inhibit (when 0) or enable (when 1) the assertion of NPR during RC11 controlled transfers. This enables the PDP-11 Processor to examine the RC11 registers before and after a UNIBUS transfer. This bit is read/write; it is cleared by initialization. This bit is active only in the maintenance mode, otherwise it is always a 0.

5	DATA TRACK	Simulates the data strobe signal from the RS64 that indicates the polarity of the detected pulse. This bit is write-only; it always reads as 0.
4	C (ADDRESS) TRACK	Simulates the address strobe signal that indicates the polarity of the detected pulse on the address track. This bit is write-only; it always reads as 0.
3	PHASE LOCK CLOCK	Simulates the RS64 phase-lock clock signal that provides the timing for the self-clocking feature during read operations. The timing is 3 times the speed of A (clock) track pulse. This bit is write-only; it always reads as 0.
2	ADDRESS MARK	Simulates the address mark signal that the RC11 receives from the RS64 before reading the sector address from the address track. This bit is write-only; it always reads as 0.
1	DATA MARK	Simulates the data mark signal that the RC11 receives from the RS64 before reading the data. This bit is write-only; it always reads as 0.
0	A (CLOCK) TRACK	Simulates the pulses from the clock track. These pulses provide the basic timing within the RS64 and the RC11. This bit is write-only; it always reads as 0.

Data Buffer Register (RCDB) 777 456
All data transaction between RC11 and the UNIBUS take place through this register. All data read from the disk appears in this register either for transfer to the bus during read or comparison during write check. During write, data from the UNIBUS is first loaded into this register prior to writing on the disk.

As the last word obtained from the disk during read or write check operation is the block check or CRC word, this register contains the CRC word of the last block read when the operation is complete. This register is read only and cleared by initialize.

SPECIFICATIONS FOR RC11

Main Specifications

Storage medium:	fixed head disk
Capacity/disk:	65,536 words (64K)
Data transfer speed:	16 μsec/word (19.2 μsec at 50 Hz)
Avg access time ($\frac{1}{2}$ rev):	17 msec (20.3 at 50 Hz)

Disk rotation speed:	1800 RPM
Disks/control, max:	4

Data Organization

Tracks:	32
Sectors/track:	64
Words/sector:	32
Bits/word:	16
Recording method:	NRZI
Recording density:	1800 bits/inch, max

Register Addresses

Look Ahead	(RCLA)	777 440
Disk Address	(RCDA)	777 442
Disk Error Status	(RCER)	777 444
Command and Status	(RCCS)	777 446
Word Count	(RCWC)	777 450
Current Address	(RCCA)	777 452
Maintenance	(RCMN)	777 454
Data Buffer	(RCDB)	777 456

UNIBUS Interface

Interrupt vector address:	210
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	panel mounted units
Size (disk):	10½" front panel height, Control mounts behind first disk drive.
Weight:	115 lbs

Power

Starting current:	6 A at 115 VAC
Running current:	2.2 A at 115 VAC
Heat dissipation:	250 W

Environment

Operating temperature:	17°C to 50°C
Relative humidity:	20% to 80%

Models

RC11-A:	Disk drive and control, 115 VAC, 60 Hz
RC11-B:	" , 230 VAC, 50 Hz

SPECIFICATIONS FOR RS64

Mechanical

Mounting:	mounts in a standard PDP-11 cabinet
Size:	10½" front panel height
Weight:	65 lbs

Power

Starting current:	6 A at 115 VAC
Running current:	2.2 A at 115 VAC
Heat dissipation:	250 W

Prerequisite: RC11

Models

RS64-A:	Disk drive, 115 VAC, 60 Hz
RS64-B:	" , 230 VAC, 50 Hz

FIXED HEAD DISK, RF11-A

DESCRIPTION

The RF11-A is a fast, low-cost, random-access bulk-storage system. An RF11-A provides 262,144 17-bit words (16 data bits and 1 parity bit) of storage. Up to eight RS11 disks can be controlled by one RF11 Control for a total of 2,047,152 words of storage. An RF11-A includes a Control Unit and the first Disk Drive.

The RF11-A is unique in fixed head disks because each word is addressable. Data transfers may be as small as one word or as large as 65,536 words. Individual words or groups of words may be read or rewritten without any limits of fixed blocks or sectors, providing optimum use of both disk storage and main memory in the PDP-11 system.

The RS11 disk contains a nickel-cobalt-plated disk driven by a hysterisis synchronous motor. Data is recorded on a single disk surface by 128 fixed read/write heads.

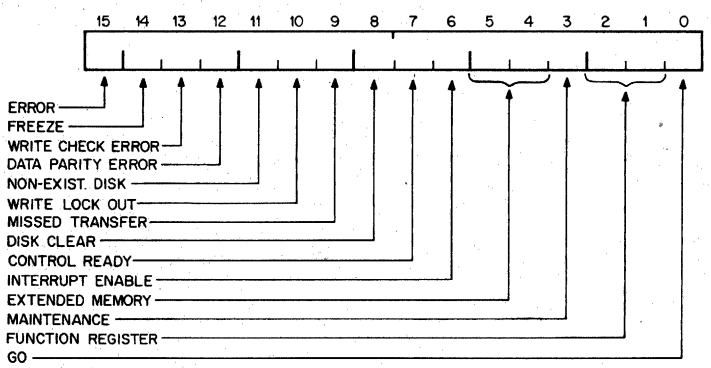
Operation

Fast track switching time permits spiral read or write. Data may be written in blocks from 1 to 65,536 words. The RF11 Control automatically continues on the next track, or on the next disk surface, when the last address on a track or surface has been used.

The Disk stores data words in a 22-bit format which includes guard bits and a sync bit to operate the self-clocking logic. The sync bit adjusts the timing of the data strobing to ensure proper recovery of each word of data. The RS11 has a redundant set of timing tracks, recorded exactly in phase with the primary timing tracks.

REGISTERS

Disk Control Status Register (DCS) 777 460



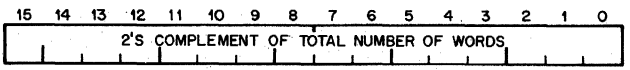
Read only: bits 15 through 9, and 7.
Write only: bits 8 and 0.

BIT	NAME	FUNCTION
15	Error (ERR)	Logical OR of DCS 14-9
14	Freeze (FRZ)	Logical OR of DAE 15-10
13	Write Check Error (WCE)	Set if the word read from memory and the word read from the disk differ during a Write Check.
12	Data Parity Error (DPE)	Set if the parity bit computed for a word does not agree with bit read from the disk.
11	Non Existent Disk (NED)	Set if DAE 4-2 are set (by the program or by sequencing from the previous value) to an address for which no disk is implemented, or if the disk address overflows (DAE 5 is set).
10	Write Lock Out (WLO)	Set if the control attempts to write into a disk segment with the write lock switch ON.
9	Missed Transfer (MXF)	Set if the control has held NPR asserted for 3 revolutions and has not received bus control.
8	Disk Clear	Initializes (PWR CLR) the disk control. Clears all bits of DCS, CMA, WC, DAT, DAE, and DBR.
7	Control Ready (RDY)	Set if the control is ready to perform function. Can be examined by a TSTB instruction.
6	Interrupt Enable (INTR ENB)	Set to allow ERR (DCS 15) or Ready = 1 to cause an interrupt.
5-4	Extended Memory (XM)	Drive BUS A 17-16 to select memory locations not in the first 32K words (64K locations).
3	Maintenance (MA)	Set to cause the control to accept inputs from maintenance register instead of from disk.
2-1	Function Register (FR)	Selects one of three functions as shown in table. Remains unchanged during error halt for restarting.

Bit 2	Bit 1	Function
0	0	No operation
0	1	Write
1	0	Read
1	1	Write Check

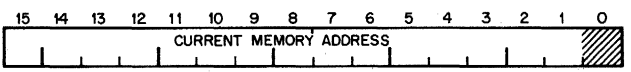
0 Go — Causes the processor to execute the function selected by the function register. Clears DCS15 unless FRZ (DCS 14) is set, and clears DCS(13-9).

Word Count Register (WC) 777 462



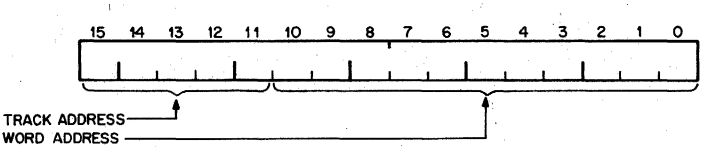
BIT	NAME	FUNCTION
15-0	Word Count (WC)	Loaded with the 2's complement of the block length and incremented by 1 before each transfer. Overflow ends the function and causes Ready to be set. Limits block size to 65,536 words. Read/write.

Current Memory Address (CMA) 777 464



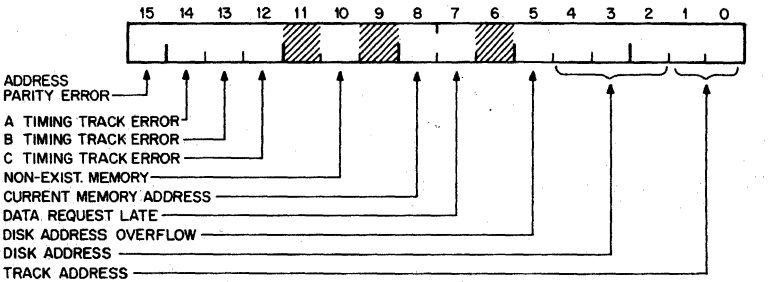
BIT	NAME	FUNCTION
15-1	Current memory Address (CMA)	Selects the UNIBUS locations for the next data transfer. Must point to an even (word) location, so CMA00 is unimplemented and CMA01 is incremented after each transfer. Extended to full 18-bit addresses by XM bits (DCS 5-4.) Initially loaded with the starting address minus two. Read/Write.

Disk Address Register (DAR) 777 466



BIT	NAME	FUNCTION
15-11	Track Address (TA)	Selects track on disk for current transfers. Initially set by program and incremented by WA overflow. Extended by TA 6-5 (DAE 1-0) to select one of 128 tracks. Read/Write.
10-0	Word Address (WA)	Selects word on disk track for next transfer. Incremented after each transfer. Overflows into TA0 to cause spiral read or write last word of one track followed by the first word of the next track. Read/Write.

Disk Address Extension Error Register (DAE) 777 470



Read only: bits 15 through 12, 10, and 5.

BIT	NAME	FUNCTION
15	Addr. Parity Error (APE)	Set if the computed address parity differs from the address parity read from the disk.
14	A Timing Track Error (ATER)	Set if missing or extra bits are detected on timing track A.
13	B Timing Track Error (BTER)	Same as ATER (DAE14) for timing track B.
12	C Timing Track Error (CTER)	Same as ATER (DAE14) for timing track C.

NOTE

The NRZI recording method provides two-bit streams from each read head. In normal operation, bits are read alternately in the two streams; however. if a bit is dropped or an extra bit is read, two bits will appear in sequence in the same bit stream. DAE 14-12 indicates such an error on the corresponding tracks.

10	Non-Existent Memory (NEM)	Set when UNIBUS data transfer is made to a non-existent memory location or when the bus address register sequenced to a non-existent memory location and did not receive SSYN within 10μs.
8	Current Mem. Addr. (CMA INH)	Prevents CMA from incrementing to allow transfers to single-address devices.
7	Data Request Late (DRL)	Set when the RF11 control is ready to transfer data and the previous data has not been transferred (the RF11 has had NPR asserted for 12 sec but is not Bus Master). Cleared when the control becomes Bus Master, or may be set or cleared by the program. DRL does not stop the current function and does not cause an interrupt; it is an indicator only.
5	Disk Addr. Overflow (DA OVFL)	Set if DA <02:00> overflows (Disk Address = 10). Causes NED (DCS11) to be set.
4-2	Disk Address (DA)	Select one of eight disks. Incremented when TA 6-0 overflow, to continue spiral transfers on next disk.
1-0	Track Address (TA)	Extend TA 4-0 (DAR 15-11).

Data Buffer Register (DBR) 777 472

BIT	NAME	FUNCTION
15-0	Data Buffer Register (DBR)	Under RF11 control, used to transfer data on the UNIBUS. Accessible for program transfers for maintenance programs only.

Maintenance Register (MA) 777 474

This register is provided for diagnostic purposes only and does not participate in the normal disk operations.

Write only: all bits

BIT	NAME	FUNCTION
12	MAINTENANCE DATA (MDT)	Simulates the disk head signal to the data track read amplifier.
11	MAINTENANCE C TIMING (MCT)	Simulates the disk head signal to the C Timing Track read amplifier.
10	MAINTENANCE B TIMING (MBT)	Simulates the disk head signal to the B Timing Track read amplifier.
9	MAINTENANCE A TIMING (MAT)	Simulates the disk head signal to the A Timing read amplifier.

GENERAL: The above signals cause the control to generate analog signals that simulate the disk head signals as received directly from the head. The diagnostic program determines the sequence and the bit rate of the signals. Each transfer is treated as if it was one cell space on the disk.

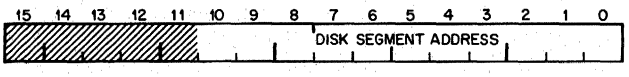
7-6	DATA TRACK MAINTENANCE (DTM)	Simulates Data Track disk interface.
5-4	C TIMING MAINTENANCE (CTM)	Simulates C Timing Track disk interface.
3-2	B TIMING MAINTENANCE (BTM)	Simulates B Timing Track disk interface.
1-0	A TIMING MAINTENANCE (ATM)	Simulates A Timing Track disk interface.

GENERAL: The above are simulated disk interface signals within the control. No disk is necessary. The diagnostic program determines the sequence of pulses and the bit rate.

NOTE

When a maintenance function is performed and the MA (DCS bit 2) is set, the effect of the disk control time outs is inhibited because of the lower bit rates encountered during maintenance.

Address of Disk Segment Register (ADS) 777 476 (Look Ahead)



BIT	NAME	FUNCTION
10-0	Address of ADS	This register allows the user to read the real-time word address of the disk. The contents of the ADS will indicate the address or the address + 1 of the data passing under the heads. The ADS register will contain the last address of the track while the disk is passing through the gap and buffer region. Read only.

PROGRAMMING EXAMPLES

Program control of the RF11/RS11 Disk is accomplished by loading the disk control registers. The disk performs the specified function and when the function is done or when an error occurs, it will cause an interrupt to the routine whose starting address is in location 204, if the interrupt enable bit (DCS06) is set; otherwise the program may test the word count register and the error bit (DCS15) to determine completion.

A common technique is to use a subroutine to load the registers. The values to be placed in the registers can be assembled following the sub-

routine call using the .WORD assembler directive. The disk control begins operation when the GO bit in the DCS register is loaded, so a WAIT instruction follows the subroutine call. Note that the WAIT instruction is in the main program, not the register-loading subroutine; this enables the interrupt routine to provide a separate error return for each disk operation.

In the following example, the DISKIO subroutine and the DSKHNDLR interrupt routine are used by the subroutine calls shown to write a 256-word block on disk 0 and then do a write check of the same block.

The subroutine calls and additional codes which are included in the main program are written as follows:

```
MAINPROG:

        JSR       R5,DISKIO       ;SUBROUTINE CALL
        .WORD     DISK ADDRESS    ;DISK ADDRESS TO
                                  ;WRITE TO
        .WORD     DATA ADDRESS    ;MEMORY ADDRESS TO
                                  ;WRITE FROM
        .WORD     -256            ;WORD COUNT
        .WORD     103             ;WRITE FUNCTION AND
                                  ;INTR ENB
        WAIT                      ;PROCESSOR WAITS FOR
                                  ;DISK HERE
        JSR       PC,ERROR        ;ERROR RETURN
        JSR       R5,DISKIO       ;NON ERROR RETURN IS
                                  ;A NEW CALL
        .WORD     DISK ADDRESS    ;THE ASSEMBLED CODE
                                  ;IS THE
        .WORD     DATA ADDRESS    ;SAME AS THE FIRST
                                  ;CALL
        .WORD     -256            ;EXCEPT FOR THE
                                  ;FUNCTION,
        .WORD     107             ;WHICH IS A WRITE-
                                  ;CHECK
        WAIT                      ;PROCESSOR WAITS
                                  ;HERE
        JSR       PC,ERROR2       ;ERROR RETURN,
                                  ;DIFFERENT ROUTINE
                  .
                  .
                  .
DISK DCS  777460
DISK WC   777462
DISK CMA  777464
DISK DAR  777466
```

The subroutine is assembled from the following code:

```
DISKIO:   BIS    #400, DISK DCS   ;DISK CLEAR
          MOV    (R5)+, DISKDAR   ;LOAD DAR REGISTER
          MOV    (R5)+, DISKCMA   ;LOAD CMA REGISTER
          MOV    (R5)+, DISKWC    ;LOAD WC REGISTER
          MOV    (R5)+, DISKDCS   ;LOAD DCS REGISTER
          RTS    R5               ;RETURN TO CALL,
                                  ;LOADING
                                  ;DCS STARTS DISK
                                  ;FUNCTION
```

The interrupt handling routine is assembled from the following code:

```
DSKHNDLR: TST    DISKDCS          ;TEST DCS15 (ERROR)
          BPL    NORMAL           ;BYPASS ERROR
                                  ;RETURN IF CLEAR
          RTI                     ;ERROR RETURN
NORMAL:   ADD    #4, (SP)         ;MOVE OLD PC PAST
                                  ;ERROR CALL
          RTI                     ;NORMAL RETURN
```

The interrupt vector for this routine is assembled from the following code:

```
          .204
          .WORD  DSKHNDLR         ;ADDRESS OF
                                  ;INTERRUPT ROUTINE
          .WORD  340              ;INTERRUPT ROUTINE
                                  ;PRIORITY
```

The only change necessary to read the same block from the disk is to replace the statement .WORD 103 in the first subroutine call with the statement .WORD 105 (which sets the function to READ).

SPECIFICATIONS FOR RF11

Main Specifications

Storage medium:	fixed head disk
Capacity/disk:	262,144 words (256K)
Data transfer speed:	16 μsec/word (19.2 μsec at 50 Hz)
Avg access time (½ rev):	17 msec (20.3 msec at 50 Hz)
Disk rotation speed:	1800 RPM
Disks/control, max:	8

Data Organization

Tracks:	128
Words/track:	2048
Bits/word:	22
Recording method:	NRZI
Recording density:	1900 bits/inch, max
Access with single R/W:	1 to 65,536 words

Register Addresses

Disk Control Status	(DCS)	777 460
Word Count	(WC)	777 462
Current Mem Address	(CMA)	777 464
Disk Address	(DAR)	777 466
Disk Adrs Ext & Error	(DAE)	777 470
Disk Data Buffer	(DBR)	777 472
Maintenance	(MA)	777 474
Adrs of Disk Segment	(ADS)	777 476

UNIBUS Interface

Interrupt vector address:	204
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load
NPR latency:	12 μsec, max allowable
Max delay:	3 disk revolutions

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	16" panel height for disk, 16" for Control unit
Weight (incl cab):	500 lbs.

Power

Starting current:	14 A at 115 VAC
Running current:	6.5 A at 115 VAC
Heat dissipation:	750 W
Frequency stability:	0.1 Hz/sec, max drift

Environmental

Operating temperature:	17°C to 33°C
Relative humidity:	20% to 55%

Models

RF11-AA: Disk drive and control, 115 VAC, 60 Hz
RF11-AB: " , 230 VAC, 50 Hz

SPECIFICATIONS FOR RS11

Mechanical

Mounting:	mounts in a standard PDP-11 cabinet
Size:	16" front panel height
Weight:	100 lbs.

Prerequisite: RF11-A

Models

RS11: Disk drive, 115 VAC, 60 Hz
RS11-A: " , 230 VAC, 50 Hz

Miscellaneous

RS11 Motor Power

Voltage: 117/235 ± 10%VAC 117 VAC

(A stepdown autotransformer is provided for 235-VAC operation.)

Phase:	Single
Frequency:	50 ± 2Hz or 60 ± 2Hz
Frequency Stability:	0.1 Hz/sec maximum drift (A constant-frequency motor-generator set or static AC/AC inverter should be provided for installation with unstable power sources.)
Current:	For a 1-disk system: Starting current, 14 Amps; Nominal current, 6.5 Amps. For an 8-disk system: Starting current, 81 Amps; Nominal current, 21 Amps. Lower starting currents can be realized if disks are sequenced.
Power Supplies:	Self contained in cabinet with controller. Also includes line filter with each disk.
Self Clocking:	The RS11 disk employs self-clocking logic for reliable data recovery. Each word is logically located relative to the timing track.
Timing Tracks:	3 plus 3 spare (pre-recorded; can be used for data recovery if the primary timing tracks are lost).
Write Lock Switches:	Sixteen switches on each RS11. Each switch controls the write protection for one 8-track (16,384 word) segment. WLO (DCS 10) is set if a write function addresses a locked-out segment.

DECPACK DISK CARTRIDGE, RK11-D

DESCRIPTION

The RK11-D DECpack cartridge disk drive and control is a complete mass storage system, offering an economical solution for large volume, random-access data storage. The system includes a modular mass storage device utilizing removable disk cartridges and a complete easy-to-program control.

A disk cartridge holds over 1.2 million words. The DECpack is ideal where a large volume of programs and data are developed and maintained for one or more users. The system is expandable up to 9.6 million words per Control (8 disks).

An RK11-D includes a Control Unit and the first Disk Drive.

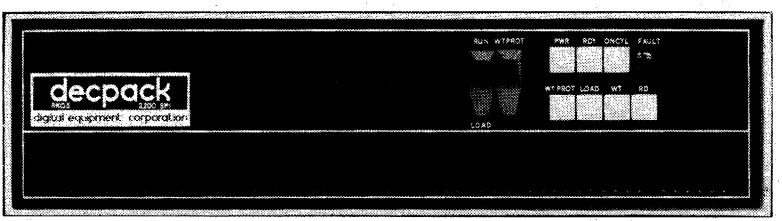
Operation

The removable disk cartridge offers the flexibility of virtually unlimited off-line capacity with rapid transfers of files between on-line and off-line without copying operations. It utilizes a cartridge similar to the IBM 2315, but with 12 sectors and twice the bit density.

Average total access time on each drive is 70 milliseconds. On expanded systems, operations are overlapped for efficiency; one drive may read or write while one or more additional drives are seeking new head positions for the next transfer. All data transfers utilize the Non-Processor Request facility during transfers.

Each disk is permanently mounted inside a protective case that automatically opens when inserted in the disk drive. While on-line, dust contamination is prevented by a highly-efficient continuous "absolute" air filtration system.

The DECpack provides accurate data storage and transfers by means of a write check function, correct cylinder verification by hardware, hardware checksum, and hardware maintenance features. There are no mechanical detents, thus a major source of wear and critical adjustment is eliminated.



CONTROLS & INDICATORS

RUN/LOAD (rocker switch)

Placing this switch in the RUN position (providing all interlocks are safe):

a. locks the drive front door
b. accelerates the disk to operating speed
c. loads the read/write heads
d. lights the RDY indicator.

Placing this switch in the LOAD position:

a. unloads the read/write heads
b. stops the disk rotation
c. unlocks the drive front door
d. lights the LOAD indicator.

CAUTION

Do not switch to the LOAD position during a write operation, as this results in erroneous data being recorded.

WT PROT (rocker switch—spring-loaded off)

Placing this momentary contact switch in the WT PROT position lights the WT PROT indicator and prevents a write operation as well as turns off the FAULT indicator if lit.

Placing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation.

PWR (indicator)

Lights when operating power is present. Goes off when operating power is removed.

RDY (indicator)

Lights when:

a. the disk is rotating at the correct operating speed
b. the heads are loaded
c. no other conditions are present (all interlocks safe) to prevent a seek, read, or write operation.

Goes off when the RUN/LOAD switch is set to the LOAD position.

ON CYL (indicator)

Lights when:

a. the drive is in the Ready condition
b. a seek or restore operation is not being performed
c. the read/write heads are positioned and settled.

Goes off during a seek or restore operation.

FAULT (indicator)

Lights when:

a. erase or write current is present without a WRITE GATE or,
b. the linear positioner transducer lamp is inoperative.

Goes off when the WT PROT switch is pressed or when the drive is recycled through a RUN/LOAD sequence.

WT PROT (indicator)

Lights when:

a. the WT PROT switch is pressed (every other time) or,
b. the operating system sends a Write Protect command.

Goes off when the WT PROT switch is pressed a second time or when the drive is recycled through a RUN/LOAD sequence.

LOAD (indicator)

Lights when the read/write heads are fully retracted and the spindle has stopped rotating.

Goes off when the RUN/LOAD switch is set to the RUN position.

WT (indicator)

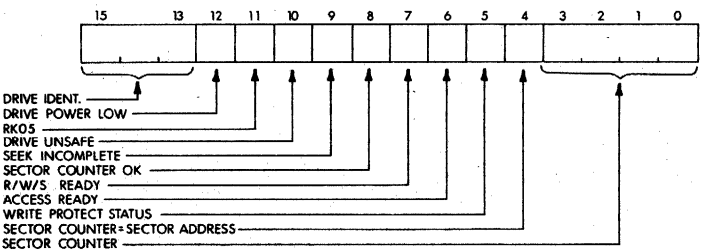
Lights when a write operation occurs. Goes off when the write operation terminates.

RD (indicator)

Lights when a read operation occurs. Goes off when the read operation terminates.

REGISTERS

Drive Status Register (RKDS) 777 400
Contains the current selected drive status and current sector address.



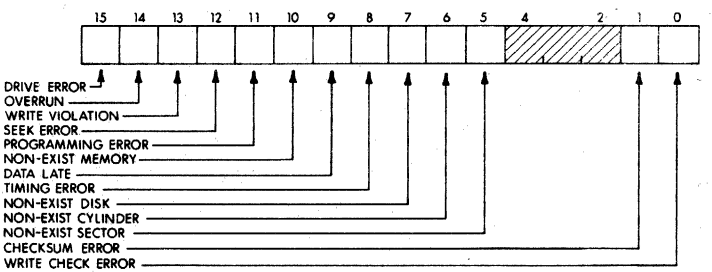
Read only: all bits

BIT	NAME	FUNCTION
15-13	Ident. of Drive (ID)	If an interrupt is caused as a result of a SEARCH COMPLETE (Bit 13 RKCS) or a SEEK INCOMPLETE (Bit 9 RKDS) these bits will contain the binary representation of the logical drive number that caused the interrupt.
12	Drive Power Low (DPL)	Set when an attempt is made to initiate a new function or a function was actively in progress when the control sensed a loss of power to one of the disk drives. This bit can be accompanied by bit 15 RKER (DRE) and is reset by a BUS INIT or a CONTROL RESET function.
11	RK05	Set to identify the selected disk drive as an RK05.
10	Drive Unsafe (DRU)	Set to indicate that an unusual condition has occurred in the drive and it is unable to properly perform any operations. Putting the RUN/LOAD switch in the LOAD position will reset the condition. If, upon putting the RUN/LOAD switch back to the RUN position the condition reoccurs the drive or associated power supply is inoperative and corrective maintenance procedures should be begun. Can be accompanied by bit 15 RKER.
9	Seek Incomplete (SIN)	Set to indicate that due to some unusual condition a SEEK function was not completed within 180ms of initiation. A DRIVE RESET function clears this condition. This bit can be accompanied by bit 15 RKER
8	Sector Counter OK (SOK)	Indicates that the selected drive sector counter (Bits 0-3 RKDS) is not in the process of changing and is ready for examination.
7	Drive Ready (DRY)	Set to indicate that the selected disk drive complies with the following conditions: a) properly supplied with power b) loaded with a disk cartridge c) door is closed

d) LOAD/RUN switch is in the RUN condition
e) the disk is spinning
f) the heads are properly loaded
g) the disk is not in a DRU condition (Bit 10 RKDS)

6	Read/Write/Seek Ready	Set when the selected drive head mechanism is not in motion and the drive is ready to accept a new function.
5	Write Protect Status (WPS)	Set when the selected disk is in WRITE PROTECTED mode
4	SC = SA	Set when the disk heads are currently positioned over the disk addresses currently held in bits 0-3 RKDA.
3-0	Sector Counter (SC)	Indicates the current sector address of the selected drive. This is the look ahead. Sector address 00 is defined as the sector which follows the sector that contains the index pulse.

Error Register (RKER) 777 402



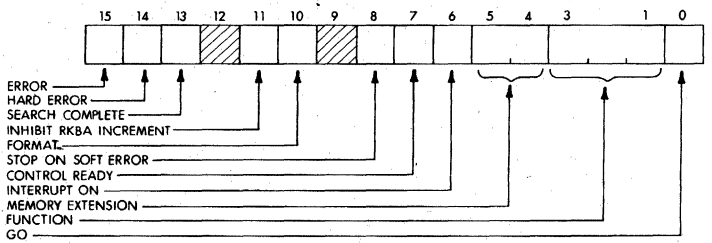
Read only: all bits.

BIT	NAME	FUNCTION
15	Drive Error (DRE)	Set when an attempt is made to initiate a function, or when a function is actively in progress, while the selected drive is not ready or in some error condition or if any of the drives in the system senses a loss of either AC or DC power. If this bit is found set the RKDS should immediately be referenced to discover the cause of the condition.

14	Overrun (OVR)	Set if during a READ, WRITE, RD/CHK or WT/CHK, operations on sector 13_8 surface 1 of cylinder address 312_8 were finished and the RKWC had not yet overflowed. This essentially is an attempt to overflow out of a disk drive.
13	Write Lock Out Violation (WLO)	Set if an attempt is made to write on a disk which is currently being write protected.
12	Seek Error (SKE)	Set if the disk head mechanism is not properly positioned while executing a normal READ, WRITE, RD/CHK or WT/CHK function.
11	Programming Error (PGE)	Set if the FMT bit (Bit 10 RKCS) is set while initiating some function other than a READ or WRITE.
10	Non-Existent Memory (NXM)	Set if memory does not respond within 20 μs of the time when the RK11 becomes Bus Master during a DATI or DATO NPR sequence. Because of the speed of the disk drive, it is possible that if a NXM does occur it will be accompanied by a DLT (Bit 7 RKER).
9	Data Late (DLT)	Set when an NPR sequence is required before the previous one has completed.
8	Timing Error (TE)	Set if a loss of timing pulses for 5 μsec has been detected.
7	Non-Existent Disk (NXD)	Set if an attempt was made to initiate a function on a non-existent drive.
6	Non-Existent Disk (NXC)	Set if an attempt was made to initiate a function on a cylinder larger than 312_8.
5	Non-Existent Cylinder (NXS)	Set if an attempt was made to initiate a transfer on a sector larger than 13_8.
1	Checksum Error (CSE)	Set while performing a RD/CHK or READ function as a result of faulty recalculation of the checksum. Cleared at the initiation of any new function. This is a soft error.
0	Write Check Error (WCE)	Set if an error was encountered during a WT/CHK function as a result of faulty bit comparison between disk data and memory data. Clears at the initiation of a new function. This is a soft error.

Note: Bits 5 through 15 are all hard errors. They are cleared only by a BUS INIT or a CONTROL CLEAR function.

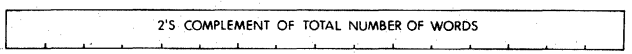
Control Status Register (RKCS) 777 404



BIT	NAME	FUNCTION
15	Error	Set when any bit in the RKER is set. Processor reaction is dictated by Bits 6 and 8 RKCS. This read-only bit clears if all the bits in RKER are cleared and if Bit 14 RKCS is cleared.
14	Hard Error (H.E.)	Set when any of Bits 5-15 RKER are set by the control. Stops all controller action and processor reaction as dictated by bit 6 RKCS. This READ ONLY bit, along with bits 5-12 RKER, is cleared only by a BUS INIT or a CONTROL RESET function.
13	Search Complete (SCP)	Signifies that the previous interrupt was caused as a result of some previous SEEK or DRIVE RESET function. READ ONLY bit. Clears at the initiation of any new function.
11	Inhibit Inc. (INH BA)	Setting this bit inhibits incrementing the RKBA during a data transfer. This allows data to be transferred to or from any one bus address for the entire operation.
10	Format (FMT)	FORMAT Mode must be used only in conjunction with the normal READ and normal WRITE function. This mode is used to format a new disk pack or to reformat any sector that may have been erased or damaged due to control or drive failure. In the FORMAT mode the normal WRITE operation is altered only in that the servo positioner is not checked for proper position before the write operation. During a WRITE the header is re-written each time

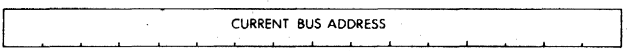
		the associated sector is written. In this mode, the normal READ operation is altered in that only one word is transferred to memory per sector; the header word. Therefore, a 3-word READ function in the FORMAT mode will transfer 3 contiguous header words to 3 consecutive memory locations for software checking. For a 200-word transfer, 200 consecutive header words from 200 consecutive sectors will be read, and so on.
8	Stop on Soft Error (SSE)	If a soft error is encountered while this bit is set: a. and Bit 6 RKCS (IDE) is reset, all controller action will stop at the end of the current sector. b. and Bit 6 RKCS (IDE) is set, all controller action will stop and a Bus Request will occur at the end of the current sector.
7	Control Ready (RDY)	Signifies that the control is no longer engaged in actively executing a function and is ready to accept a command.
6	Int. on Done Enable (IDE)	The control will issue a Bus Request and interrupt to vector address 220 if: 1. A function has completed its activity; 2. A hard error is encountered; 3. A soft error is encountered and bit 8 RKCS is set.
5-4	Memory Extension (MEX)	Reserved for extended bus addresses and is used in conjunction with the RKBA. These bits make up a two-bit counter that increments each time the RKBA overflows. A bus DATO to these bits overrides any overflow from the RKBA.
3-1	Function	These bits indicate the binary representation of the function to be performed. The functions are: CONTROL RESET (000) WRITE (001) READ (010) WRITE CHECK (011) SEEK (100) READ CHECK (101) DRIVE RESET (110) WRITE LOCK (111)
0	Go	Initiates the function encoded in bits 1 through 3 of RKCS. Write only bit.

Word Count Register (RKWC) 777 406



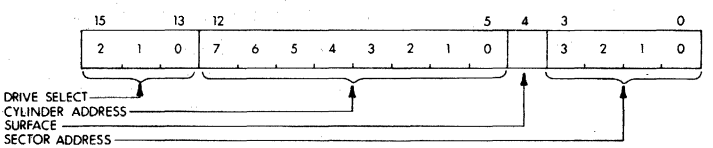
Contains the two's complement of the total number of words to be affected by a given function. It increments by one after each word transfer.

Current Bus Address Register (RKBA) 777 410



Contains the Bus Address to or from which data will be transferred. The register is incremented by two at the end of each transfer.

Disk Address Register (RKDA) 777 412



NOTE

All RKDA bits are loaded from the bus data lines only in RK11 READY state, and cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.

BIT	NAME	FUNCTION
15-13	Drive Select (DR SEL)	These bits contain the binary representation of the logical drive number currently being selected.
12-5	Cylinder Address (CYL ADD)	Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312_8.
4	Surface (SUR)	When set, the lower disk head is enabled and operation is performed on the lower surface. When clear, the upper disk head is enabled.
3-0	Sector Address (SC)	Binary representation of the disk sector to be addressed for the next function.

Data Buffer Register (RKDB) 777 416

BIT	NAME	FUNCTION
15-0	Data	This register is a general data handler. It is loaded from the bus only while the RK11 is bus master during an NPR sequence. The RKDB is constructed of a 6-word register file capable of sustaining a UNIBUS NPR latency of 55 μsec every 85 μsec.

Cross Cylinder Operation

Surface 0 is defined as the upper surface and is active when RKDA 04 is reset. If a transfer is initiated that requires an overflow from surface 0, the control will automatically change to sector 0 of surface 1 with no time loss. If a transfer is initiated that requires an overflow from surface 1, the control will automatically move the heads to the next cylinder, check for proper head positioning, and continue the transfer on sector 0 and surface 0 of the new cylinder. An attempt to overflow out of the last sector of the last cylinder will result in an error condition.

At the end of each sector of data transfer the RKDA is automatically incremented.

Hardware Poll

The control is capable of having any or all of the drives performing a SEEK or DRIVE RESET operation at any one time. A HARDWARE POLL feature will identify the logical drive number in bits 13, 14 and 15 of the RKDS of any drive that has completed a SEEK or DRIVE RESET operation and cause an interrupt if bit 6 RKCS is set (IDE) and the control is in the READY state (bit 7 RKCS is set) and the control was not already attempting to cause an interrupt as a result of some other operation. This will occur even if Bit 6 RKCS (IDE) was not set when first initiating the SEEK or DRIVE RESET function. If two or more drives complete the function simultaneously, the control will interrupt once for each drive and identify each one in turn in the RKDS. Care should be taken in this situation to raise the processor interrupt status to a level equal to or greater than that currently held by the RK11 or else a second interrupt will occur immediately after the first and the end result will be that the interrupt service routine has been interrupted. This situation will also occur if an attempt is made to initiate a SEEK to an address that the drive is already at since one interrupt will occur as a result of the SEEK function having been successfully initiated and another to report that the heads have reached their destination, which will occur immediately because the heads are already there.

Interrupts

Because of the format structure of the RK11, any interruption of a write sequence cannot be tolerated until the end of the sector because this would result in essentially an unformatted disk. Therefore, any outside intervention of this operation is held off until the end of the current sector, which includes the CONTROL RESET function and the PROCES-

SOR or BUS INITIALIZE signals. Therefore, all those functions, such as CONTROL RESET, SEEK and WRITE LOCK, which normally take only a few microseconds to initiate can actually take up to 3.3ms if initiated while writing. For this reason the SEEK and WRITE LOCK functions will cause an interrupt (if bit 6 RKCS is set) as soon as the function has been successfully initiated. The CONTROL RESET, which cannot cause an interrupt under any circumstances, can, therefore, take up to 3.3ms to complete.

SPECIFICATIONS FOR RK11-D

Main Specifications

Storage medium:	disk cartridge
Capacity/cartridge:	1,228,800 words
Data transfer speed:	11.1 μsec/word
Time for ½ revolution:	20 msec
Disk rotation speed:	1500 RPM
Drives/control, max:	8

Track Positioning Time

One track move:	10 msec
Average:	50 msec
Maximum:	85 msec

Data Organization

Surfaces/drive:	2
Tracks/surface:	200 + 3 spare
Sectors/track:	12
Words/sector:	256
Recording method:	double frequency
Recording density:	2040 bits/inch, max
Access with single R/W:	1 to 65,536 words

Register Addresses

Drive Status	(RKDS)	777 400
Error	(RKER)	777 402
Control Status	(RKCS)	777 404
Word Count	(RKWC)	777 406
Current Bus Address	(RKBA)	777 410
Disk Address	(RKDA)	777 412
Data Buffer	(RKDB)	777 416

UNIBUS Interface

Interrupt vector address:	220
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	A standard cabinet is supplied for the drive
Disk drive:	Panel mounted, 10½" high
Disk control:	1 System Unit (SU)

Power

Starting current:	10 A at 115 VAC for 2 seconds
Running current for drive:	2 A at 115 VAC
Current for control:	7.5 A at + 5 V
Heat dissipation:	160 W

Environmental

Operating temperature:	15°C to 43°C
Relative humidity:	20% to 80%

Models

RK11-DE:	Disk drive and control, 115 VAC, 60 Hz
RK11-DJ:	" 230 VAC, 50 Hz

SPECIFICATIONS FOR RK05

Mechanical

Mounting:	mounts in a standard PDP-11 cabinet
Size:	10½" front panel height
Weight:	110 lbs.

Power

Starting current:	10 A at 115 VAC for 2 seconds
Running current:	2 A at 115 VAC
Heat dissipation:	160 W

Prerequisite: RK11-D

Models

RK05-AA:	Disk drive, 115 VAC, 60 Hz
RK05-BB:	" 230 VAC, 50 Hz
RK05-KA:	Disk cartridge

DISK PACK, RP11-C

DESCRIPTION

The RP11-C is a complete mass storage system using a magnetic disk pack with 20 data surfaces and a moving read/write head. The RP11-C includes a Control Unit and the first Disk Pack Drive. The system is expandandable up to 8 drives, each having a capacity of 20,480,000 16-bit words. Access times are 29 msec. average lateral (cylinder to cylinder) and 12.5 msec. half rotational. Record lengths of 1 to 65,536 words may be accessed with one read, write, or write check command. The RP11-C will read and write disk packs compatible with the PDP-10 and PDP-15 disk pack format.

The RP11-C provides hardware for execution of eight different functions.

Function	Code	Type
Idle	0	initiate
Write	1	execute
Read	2	execute
Write Check	3	execute
Seek	4	initiate
Write (no seek)	5	execute
Home Seek	6	initiate
Read (no seek)	7	execute

Initiate functions require only a small portion of the controller's time. For example, Home Seek and Seek require only 16 μsec. of controller time for their execution. For this period of time, the controller is busy. Initiate commands require that the target unit be selected only for this busy period, i.e., although a Seek may require 50 msec. for completion, the unit need only be selected for the busy period. Idle (reset) requires only 4 μsec. of RP11-C time. Execute instructions, however, require all the controller's time necessary to complete the function. The controller is busy for the entire operation and, therefore, cannot be interrupted for Initiate-type functions.

Functions are selected by loading a 3-bit FUNCTION REGISTER with an octal number equal to the function code.

There are three data registers and a silo memory in the RP11-C which provide compatibility between disk packs read and/or written by the RP10 or RP15 (PDP-10 and PDP-15 counterparts of the RP11-C). These registers are each 36-bits in length and provide multi-buffering between the PDP-11 and the RP03.

Silo Memory—The first-in first-out silo memory provides 64 words of buffering between the UNIBUS and the Disk. During write operations, the silo is loaded at UNIBUS rates with up to 64 16-bit data words. These are unloaded asynchronously into the 36-bit buffer register in

synchronism with the shift register load commands. During read operations, the silo is loaded in two or three separate cycles from the buffer register and initiates a UNIBUS memory cycle whenever a new data word "bubbles" to the output.

Buffer Register—During Write operations, data is transferred from the silo memory in two or three 16-bit memory cycles.

During Read operations, the contents of the buffer register is broken into two or three 16-bit bytes which are transferred to the silo memory in two or three consecutive operations.

Shift Register—For Write Operations, the contents of the buffer register are loaded into the shift register where it is serialized and transferred to the disk.

During Read operations, the serial data from the disk is assembled in the shift register and then transferred to the buffer register.

A 37th bit, which works in conjunction with the shift register, generates and checks odd word parity for Write and Read operations.

Longitudinal Parity Register—During Write operations, each 36-bit word of the buffer register is Exclusive ORed into the longitudinal parity register. At the end of each sector the contents of the longitudinal parity registers are written on the disk. This word is actually a bit position parity check.

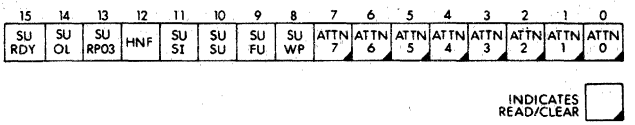
During Read operations, each assembled word of the shift register is Exclusive ORed into the longitudinal parity register. At the end of each sector, the longitudinal parity register is checked for comparison with the longitudinal parity word written. Note that the RP11-C generates and checks both row and column parity in each sector.

REGISTERS

Device Status Register (RPDS) 776 710

The Device Status Register (RPDS) holds the current state of the selected drive and the Attention signals from each of the eight possible drives. The eight attention bits are read/clear. They can be selectively cleared by moving a 1 to the desired bit location(s). The other bits of RPDS are read only. The RPDS bits are shown with the significance of each bit when set.

RPDS 776 110



Device Status Register (RPDS)

Bit	Function
00-07	DRIVE 00-07 ATTENTION. ATTENTION is set by a drive when a Seek is successfully completed or a 100-ms period elapses after Seek initiation indicating an incomplete Seek.
08	SELECTED UNIT WRITE PROTECTED. This bit is set when the WRITE PROTECT switch on the selected drive is set and when contents of RPCA and RPDA fall within the bounds of the selected address lockout if the WRITE LOCKOUT switch is set.
09	SELECTED UNIT FILE UNSAFE. The selected drive has detected a self-error condition and is prohibiting all operations.
10	SELECTED UNIT SEEK UNDERWAY. The selected drive has initiated a Seek operation, but the Attention signal has not yet been returned.
11	SELECTED UNIT SEEK INCOMPLETE. The selected drive has failed to successfully complete a Seek operation.
12	HEADER NOT FOUND. The selected drive has completed a full revolution without locating the addressed sector.
13	SELECTED UNIT RP03. The selected drive is an RP03.
14	SELECTED UNIT ON LINE. The selected drive ENABLED/DISABLE switch is set to ENABLE.
15	SELECTED UNIT READY. The selected drive is capable of performing another operation.

Error Register (RPER) 776 712

The Error Register (RPER) contains all error conditions generated within the RP11-C controller. In the normal mode, RPER is a read only register; in the maintenance mode, Write into RPER capability is provided.

RPER 776 712

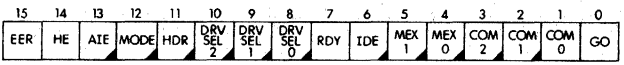
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPV	FUV	NXC	NXT	NXS	PROG	FMTE	MODE	LPE	WPE	CSME	TIMEE	WCE	NXME	EOP	DSK ERR

Error Register (RPER)

Bit	Function
00	DISK ERROR. OR condition of header has not been found and the selected unit Seek is incomplete.
01	END OF PACK. Data transfer (Read or Write) is attempted across the end of the last sector of the pack.
02	NON-EXISTENT MEMORY. More than 10 μs were required to complete a UNIBUS transaction.
03	WRITE CHECK ERROR. Data read from the disk pack does not compare with data read from memory during the Write Check operation.
04	TIMING ERROR. Data is lost because the UNIBUS did not respond in time to meet disk requirements.
05	CHECKSUM ERROR. Calculated checksum does not compare with that read from the disk.
06	WORD PARITY ERROR. Calculated word parity does not compare with that read from the disk.
07	LONGITUDINAL PARITY ERROR. Calculated longitudinal parity does not compare with that read from the disk.
08	MODE ERROR. Header operation was attempted while the RP11-C is in the PDP-11 mode.
09	FORMAT ERROR. Parity error was detected in a sector's header word.
10	PROGRAM ERROR. Data transfer operation was attempted with the content of the RPWC equal to zero, or an operation was attempted on an off-line drive, or while another instruction was still in progress.
11	NON-EXISTENT SECTOR. Disk operation was attempted when the content of the Sector Address Register was not within the 0 through 9_{10} range.
12	NON-EXISTENT TRACK. Disk operation was attempted when the content of the Track Address Register was not within the 0 through 19_{10} range.
13	NON-EXISTENT CYLINDER. Disk operation was attempted when the content of the Cylinder Address Register was not within the 0 through 405_{10} range.
14	FILE UNSAFE VIOLATION. Disk operation was attempted when SUFU was true.
15	WRITE PROTECT VIOLATION. Disk Write operation was attempted when SUWP was true.

Control Status Register (RPCS) 776 714
The bit configuration loaded into the Control Status Register (RPCS) initiates and controls a disk function. All bits are read/write unless noted otherwise.

RPCS 776 714



Control Status Register (RPCS)

Bit	Function
00	GO. Set from the bus causes the RP11-C to initiate the operation encoded in bits 03 through 01 of the RPCS. This write-only bit is always read as a 0.
01-03	FUNCTION BITS. Specify the operation to be performed.
04-05	MEMORY EXTENDED ADDRESS. Specifies the 32K field of PDP-11 memory used in data transfer.
06	INTERRUPT ON DONE (ERROR) ENABLE. Causes the RP11-C to raise an interrupt request when a disk operation is complete, or if an error occurs.
07	READY. The RP11-C is in a condition to accept and execute a new operation. READY is a read-only bit.
08-10	DRIVE SELECT. Specify the disk drive which is to be the subject of any controller action.
11	HEADER. The function of the Function Register is a Header operation.
12	MODE. The RP11-C is conditioned to read or write disk packs in DECsystem-10 or PDP-15 format.
13	ATTENTION INTERRUPT ENABLE. Causes the RP11-C to raise an interrupt request whenever any drive raises its Attention line.
14	HARD ERROR. OR of all errors except data errors. This is a read-only bit.
15	ERROR. OR of all errors. This is a read-only bit.

NOTE
The RP11-C device handler software must include routines that will test the ERR and HE flags to validate the current operation before proceeding.

Word Count Register (RPWC) 776 716
The Word Count Register (RPWC) is loaded from the bus and specifies the number of words to be transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred and the RPWC, therefore, must be loaded with the 2's complement of the number of words to be transferred. The RPWC is a read/write register containing 16 bits.

NOTE

Because the disk pack system uses 36-bit disk words, the word count must be equal to a multiple of the number of PDP-11 memory words per disk word; i.e., in PDP-11 mode, there are two PDP-11 words per disk word and the word count must be a multiple of two. In PDP-10 or PDP-15 mode, there are three PDP-11 words per disk word, and the word count must be a multiple of three.

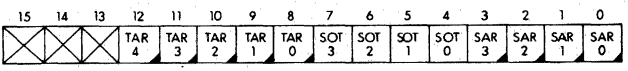
Bus Address Register (RPBA) 776 720
The Bus Address Register (RPBA) is loaded from the bus and specifies the bus address of data transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred. The RPBA, therefore, is loaded with the address of the first data word to be transferred (not first data word address minus one). The RPBA is a read/write register containing 16 bits.

Cylinder Address Register (RPCA) 776 722
Bits 08-00 of the Cylinder Address Register (RPCA) are loaded from the bus and specify the disk cylinder for any disk operation. Bits 08-00 are read/write bits. Bits 15-09 are not used.

Disk Address Register (RPDA) 776 724
Bits 03-00 of the Disk Address Register (RPDA) are loaded from the bus and specify the disk sector address for any operation other than Seek or Home Seek. Bits 03-00 are read/write. Bits 07-04 are read-only bits which contain the current physical sector (number of sectors past index) of the selected drive.

Bits 12-08 are loaded from the bus to specify the track address for any disk operation. Bits 12-08 are read/write.

RPDA 776 724



SAR= SECTOR ADDRESS
SOT= PHYSICAL SECTOR
TAR= TRACK ADDRESS

Selected Unit Cylinder Address (SUCA) 776 734
The Selected Unit Cylinder Address (SUCA) register stores the contents of the selected RP03 cylinder address register in bits 08-00.

Maintenance 1 Register (RPMI) 776 726
The Maintenance 1 Register (RPMI) is read-only and provides a means for the PDP-11 to examine the state of the RP11-C's interface to the RP03 Disk Pack Drive. This register may be read at any time, but because of the asynchronous operation of the interface, meaningful results cannot be expected unless the RP11-C is in the maintenance mode.

Maintenance 1 Register, Address 776 726

Bit	Function
00-07	BUS OUT 00-07. BUS OUT 00-07 signals to the RP03 Disk Pack Drive.
08	SET CYLINDER. State of the control tag SET CYLINDER.
09	SET HEAD. State of the control tag SET HEAD.
10	CONTROL. State of the control tag CONTROL.
11	SILO IN READY. Silo is ready to receive data.
12	SILO OUT READY. Silo has data ready for output.

Maintenance 2 Register (RPM2) 776 730
The Maintenance 2 Register (RPM2) is write-only and, in conjunction with RPM3, allows the PDP-11 to simulate the RP03 Disk Pack Drive while in the maintenance mode. Loading this register in the normal mode has no effect.

Maintenance 2 Register

Bit	Function
00-07	MAINTENANCE ATTENTION 00-07. Simulate the Attention signals from the eight possible disk drives.
08-15	MAINTENANCE CYLINDER ADDRESS REGISTER. Set by the bus, simulate the lower eight bits of the Cylinder Address Register signals from the selected drive.

Maintenance 3 Register (RPM3) 776 732
The maintenance 3 Register (RPM3) is write-only and, in conjunction with RPM2, allows the PDP-11 to simulate the RP03 Disk Pack Drive

while in the maintenance mode. Loading this register in the normal mode has no effect.

Maintenance 3 Register

Bit	Function
00	MAINTENANCE CLOCK. When set by the bus causes one cycle of the RP11-C control clock to be generated.
01-07	Not Used
08	MAINTENANCE SECTOR. When set by the bus simulates a Sector Pulse from the selected drive.
09	MAINTENANCE END OF CYLINDER. When set by the bus simulates the selected drive signal End of Cylinder.
10	MAINTENANCE SEEK INCOMPLETE. When set by the bus simulates the selected drive signal Seek Incomplete.
11	MAINTENANCE FILE UNSAFE. When set by the bus simulates the selected drive signal File Unsafe.
12	MAINTENANCE INDEX. When set by the bus simulates an Index Pulse from the selected drive.
13	MAINTENANCE ON LINE. When set by the bus simulates the selected drive signal On Line.
14	MAINTENANCE READY. When set by the bus simulates the selected drive signal Ready.
15.	MAINTENANCE READ ONLY. When set by the bus simulates the selected drive signal Read Only.

Silo Memory (SILO) 776 736

The Silo Memory is a 64-word, 16-bit, first-in/first-out (FIFO) MOS storage device. It can be loaded from the UNIBUS whenever the SILO IN READY bit in the Maintenance 1 Register is logic 1. If no readout is performed, the silo will accept 64 words before dropping SILO IN READY. The silo may be read whenever the SILO OUT READY bit in the Maintenance 1 Register is logic 1. As soon as all words previously stored have been read out, SILO OUT READY will go low and remain low until further data is stored. A transit time of 32 μs maximum is required for an input word to "bubble" to the output.

For maintenance purposes, the Silo Memory is assigned a Unibus device register address, 776736. This allows maintenance personnel to check out that portion of the RP11-C by moving a data word to and from the Silo Memory.

SPECIFICATIONS FOR RP11-C

Main Specifications

Storage medium:	disk pack
Capacity/pack:	20,480,000 words
Data transfer speed:	7.5 usec/word
Time for ½ revolution:	12.5 msec
Disk rotation speed:	2400 RPM
Drives/control, max:	8

Track Positioning Time

One track move:	7.5 msec
Average:	29 msec
Maximum:	55 msec

Data Organization

Surfaces/drive:	20
Tracks/surface:	400 (plus 6 spares)
Sectors/track:	10
Words/sector:	256
Bits/word:	16
Recording method:	double frequency, NRZ
Recording density:	2200 bits/inch, max
Access with single R/W:	1 to 65,536 words

Register Addresses

Device Status	(RPDS)	776 710
Error	(RPER)	776 712
Control Status	(RPCS)	776 714
Word Count	(RPWC)	776 716
Bus Address	(RPBA)	776 720
Cylinder Address	(RPCA)	776 722
Disk Address	(RPDA)	776 724
Maintenance 1	(RPM1)	776 726
Maintenance 2	(RPM2)	776 730
Maintenance 3	(RPM3)	776 732
Selected Unit Cyl Adrs	(SUCA)	776 734
Silo Memory	(SILO)	776 736

UNIBUS Interface

Interrupt vector address:	254
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

	Disk	Control
Mounting:	1 free-standing unit	1 std PDP-11 cab. (supplied)
Size:	40"H x 30"W x 24"D	
Weight:	415 lbs	325 lbs

Power

Input current:	7 A at 115 VAC 6 A at 230 VAC
Heat dissipation:	2100 W

Environment

Operating temperature:	15°C to 33°C
Relative humidity:	10% to 80%

Models

RP11-CE:	Disk pack drive and control,	115 VAC, 60 Hz (for control)
RP11-CJ:	" "	230 VAC, 50 Hz

SPECIFICATIONS FOR RP03

Mechanical

Mounting:	1 free-standing unit
Size:	40" H x 30" W x 24"D
Weight:	415 lbs

Power

Starting current:	30 A at 230 VAC, 60 Hz
Running current:	6 A at 230 VAC, 60 Hz
Heat dissipation:	1300 W

Prerequisite: RP11-C

Models

RP03-AS:	Disk pack drive,	230 VAC, 60 Hz
RP03-BS:	" "	230 VAC, 50 Hz

TAPE CASSETTE, TA11

DESCRIPTION

The TA11 Magnetic Tape Cassette System is a reliable, inexpensive, dual-drive, reel-to-reel unit designed to replace paper tape. Its two drives run non-simultaneously using proprietary Digital Equipment Corporation Philips-Type cassettes. Engineered to provide users with optimum price/performance, the system offers the following features:

- 1 MIL TAPE. Heavy mylar backing eliminates edge damage and resultant tape failure.
- REEL-TO-REEL DRIVE. Increases tape life. Only two driving elements. No pinch rollers, capstans, brakes, clutches, pulleys or belts.
- SINGLE TRACK RECORDING. Differentially balanced head eliminates external noise sensitivity. Low density and wide track recording ensure reliability.
- DC MOTORS. Linear servos provide precise, gentle tape acceleration and deceleration. Eliminate stretching and guarantees gap spacing.
- SOLID-CASTING DRIVE. All elements needed to control tape position, skew and motion are mounted on precision solid casting.
- MODIFIED HUB. Optimizes data capacity, simplifies loading.
- LEADER DETECTION. Optical, foolproof, failsafe.
- CASSETTES INTERCHANGEABLE. Assured by precision construction and frequency-independent read electronics.
- ERROR CHECKING CIRCUITS. 16-bit cyclic redundancy check.
- PHASE-ENCODED RECORDING. Read by sensitive, noise-immune peak detection circuits and phase lock loop.
- SERVICEABLE. Electronics, drives and power supply are easily accessible plug-in subassemblies.

The TA11 includes a Control Unit and a Dual Tape Transport.

Data Organization

In the TA11 Cassette System, data is recorded on tape in a single bit-serial track of data. Since there is no prerecorded timing or format track (such as in DECtape), data must be sequentially recorded and retrieved as in conventional magnetic tape systems.

The cassette medium is an oxide coated tape with sections of clear leader (no oxide) appended to both ends. Data can not be recorded in these clear leader sections, but they identify BOT (beginning of tape) and EOT (end of tape). Placement of data onto the recordable region of the cassette tape is organized into units called files. Adjacent files are separated by file gaps, which are generated under software control. Each file consists of one or more blocks separated by block gaps. Block gaps are generated automatically. Each block consists of one or more bytes of data and two cyclic redundancy check (CRC) bytes. Under program control, the CRC bytes are appended when a block is written and checked when a block is read. Each byte consists of eight bits (no parity). The number of files, blocks per file, and bytes per block is unrestricted, ex-

cept for tape capacity. Tape capacity is 92,000 bytes, minimum. This is reduced by 300 bytes per file gap and 46 bytes per block gap.

CONTROLS & INDICATORS

There are three manual controls on the tape drive. Each drive contains a separate REWIND pushbutton and a Power-On indicator. The Power ON/OFF toggle switch for the entire transport is located on the chassis rear panel. These manual controls and indicators perform the following functions:

REWIND—Pressing this momentary contact pushbutton on one of the two drives, rewinds the tape on that drive, at high speed, to the Beginning-of-Tape (BOT) marker provided:

a. a cassette is loaded.

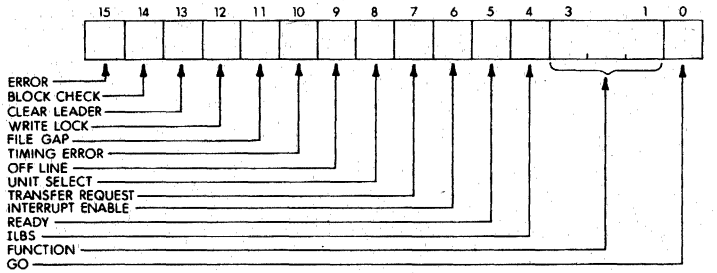
b. tape is not moving under program control.

Pressing this switch during a program controlled operation has no effect. thick, mylar substrate

Power ON/OFF—Placing this switch in the ON position lights both Power-On indicators (located opposite the REWIND pushbuttons on the lower door of each drive) and activates the internal dc power supply. Conversely, placing this switch in the OFF position de-activates the power supply and turns off both Power-On indicators.

REGISTERS

Control and Status Register (TACS) 777 500



Effect of the Initialize (INIT) signal: clear bits 8 to 6, 4 to 1; set bit 5

Read only: bit 15 through 9, 7, and 5
Write only: bit 0

BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition determined by the current status indicators of TACS, bits 14 through 9 and the current function, bits 3 through 1. Error bit is valid only when ready is set.

BIT	NAME	FUNCTION
14	Block Check	Set to indicate a CRC error for READ and SFB. During a READ function, Block Check sets Error. During an SFB function, the bit is normally expected and does not set Error. Cleared when the next function is successfully initiated.
13	Clear Leader	Set when the currently selected cassette is at EOT or BOT. The bit sets Error for all functions except REWIND.
12	Write Lock	Set to indicate that the currently selected cassette is write-protected if and only if the current function bits are set for WRITE or WFG. The bit sets Error.
11	File Gap	Set when a file gap has been entered during a READ, SFB, SRF or SFF function. The bit sets Error only on READ and SFB. Cleared when the next function is successfully initiated.
10	Timing Error	Set when the program's response to Transfer Request was not quick enough and signifies loss of data during READ or WRITE function. The bit sets Error. Cleared when the next function is successfully initiated.
9	Off Line	Set when the currently selected cassette is not present or when there is no power in the cassette transport. The bit sets Error on all functions.
8	Unit Select	Specifies which transport is under program control 0 for left (unit 0); 1 for right (unit 1).
7	Transfer Request	Set when data is available in Data Buffer, TADB, during READ, or request for data during WRITE. Cleared when TADB is addressed. The bit is held clear by ILBS. It inhibits Ready from setting and must be serviced prior to Ready.
6	Interrupt Enable	Set to enable Ready or Transfer Request = 1 to cause an interrupt.
5	Ready	Set when the Cassette is ready to accept and execute a command. It is cleared when a function is initiated and set when the function is completed as long as Transfer Request is clear.
4	ILBS	Initiate Last Byte Sequence. Set to terminate WRITE function by causing the transport to write the CRC bytes, and to terminate READ function by causing the transport to read and check the next two bytes on tape as CRC characters. For an n-byte block, ILBS is set in response to the n + 1 Transfer Request. The bit holds Transfer Request clear.

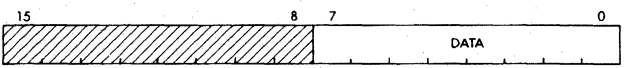
BIT	NAME	FUNCTION
3-1	Function	Indicates function to be performed.

BIT

3	2	1	Function	
0	0	0	WRITE FILE GAP	WFG
0	0	1	WRITE	WRITE
0	1	0	READ	READ
0	1	1	SPACE REV. FILE	SRF
1	0	0	SPACE REV. BLOCK	SRB
1	0	1	SPACE FWD. FILE	SFF
1	1	0	SPACE FWD. BLOCK	SFB
1	1	1	REWIND	REWIND

0 Go — Set to initiate the function specified by bits 3 to 1.

Data Buffer Register (TADB) 777 502



The TADB register serves a dual function and actually comprises two separate registers in the control. One register is loaded with 8-bit data from the Cassette during the read function and this data can be retrieved by reading TADB. The other register is loaded from the UNIBUS and presented to the Cassette during the write function.

SPECIFICATIONS

Main Specifications

Storage medium:	0.150" wide magnetic tape (in a DEC cassette)
Capacity/cassette:	92,000 bytes
Data transfer speed:	562 bytes/sec, max
Drives/control:	2 (1 dual unit)

Data Organization

Number of tracks:	1 (full width)
Bytes/block:	1 to 92,000
Bits/byte:	8
Recording method:	phase encoding
Recording density:	350 to 700 bits/inch

Tape Motion

Read/write speed:	9.6 inches/sec, avg
Search speed:	22 inches/sec, avg
Start/stop time:	20 msec, max
Rewind time:	20 sec, typ (100 to 150 in/sec) 30 sec, max
Handling:	reel-to-reel drive

Tape Characteristics

Length:	150 ft.
Type:	computer-grade, 100% certified, 1 mil thick, mylar substrate
Error rate, max:	1 in 10^8 bits (assuming 3 retries on a read error)

Register Addresses

Command and Status	(TACS)	777 500
Data Buffer	(TADB)	777 502

UNIBUS Interface

Interrupt vector address:	260
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	1 panel mounted unit + 1 SPC slot
Size:	5¼" front panel height + quad module
Cable:	15 ft., supplied; 25 ft., max.

Power

Input current:	1 A at 115 VAC 1.5 A at + 5 V
Heat dissipation:	120 W

Environmental

Operating temperature:	10°C to 40°C
Relative humidity:	20% to 80%

Models

TA11-AA:	Dual cassette unit and control, 115 VAC, 60 Hz
TA11-AB:	" 230 VAC, 50 Hz
TU60-K:	Cassette with 150 ft. of certified tape

Miscellaneous

Error control: 16-bit cyclic redundancy check (CRC), hardware generated and appended to data at time of writing. Tested during read by hardware via program command.

Read electronics: Peak detection/phase lock loop (low threshold read).

Typical block format:

Pre-Gap	Pre-amble	"N" Data Bytes	CRC Character	Post-Gap
.25"	32 bit		$(x^{16} + x^{15} + x^2 + 1)$	.25"

DECTAPE, TC11-G

DESCRIPTION

The TC11-G is a dual-unit, bidirectional magnetic-tape transport system for auxiliary data storage. Low cost, low maintenance and high reliability are assured by:

- Simply designed transport mechanisms which have no capstans and no pinch rollers.
- Hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion)
- Redundant recording
- Manchester phase recording techniques (virtually eliminate drop outs)

Each transport has a read/write head for information recording and playback on five channels of tape. The system stores information at fixed positions on magnetic tape as in magnetic disk or drum storage devices, rather than at unknown or variable positions as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

A DECtape system consists of up to 4 dual transports, a Control Unit (which will buffer and control information for up to four dual transports) and DECtape 3/4-inch magnetic tape on 3.9-inch reels. A TC11-G includes a Control Unit and the first dual Tape Transport.

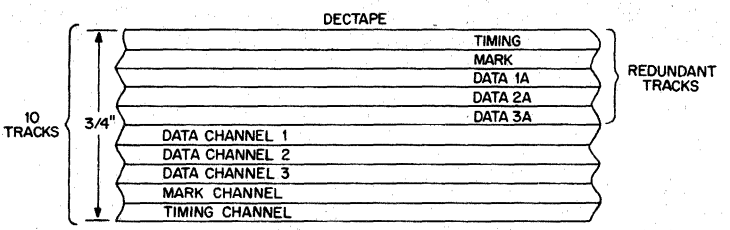
Operation

The system utilizes a 10-track read/write head. The first five tracks on the tape include a timing track, a mark track, and three data tracks. The other five tracks are identical counterparts and are used for redundant recording to increase system reliability. The redundant recording of each character bit on non-adjacent tracks materially reduces bit dropouts and minimizes the effect of skew. The use of Manchester phase recording, rather than amplitude sensing techniques, virtually eliminates dropouts.

The timing and mark channels control the timing of operations within the Control Unit and establish the format of data contained on the information channels. The timing and mark channels are recorded prior to all normal data reading and writing on the information channels. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing channel. Therefore, wide variations in the speed of tape motion do not affect system performance.

The standard format tape is divided into 578 blocks. The structure of

each block is symmetric: block numbers and checksums are recorded at both ends of a block and thus searching, reading, or writing can occur in either direction. However, a block read in the opposite direction than it was written will have the order of the data words reversed.



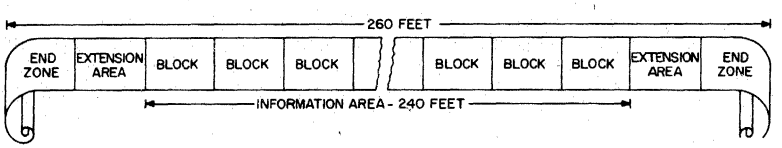
DECtape Format

Information read from the mark channel is used during reading and writing data to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control mode. The data tracks are located in the middle of the tape where the effect of skew is minimum. The data in one bit position of each track is referred to as a line or as a character. Since six lines make up a word, the tape can record 18-bit data words. During normal data writing, the Control disassembles the 18-bit word and distributes the bits so they are recorded as six 3-bit characters. Since PDP-11 words are 16-bits long, the Control writes the extra two bits as 0's and ignores them when reading. However, during special modes, the extra two bits can be written and recovered.

A 260-foot reel of DECtape is divided into three major areas: end zones (forward and reverse), extension zones (forward and reverse), and the information zone. The two end zones (each approximately 10 feet) mark the end of the physical tape and are used for winding the tape around the heads and onto the take-up reel. These zones never contain data.

The forward and reverse extension areas mark the end of the information region of the tape. Their length is sufficient to ensure that once the end zone is entered and tape motion is reversed, there is adequate distance for the transport to come up to proper tape speed before entering the information area.

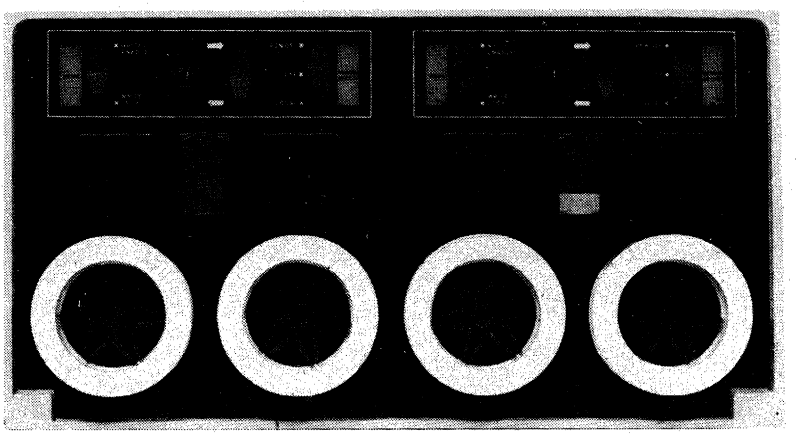
The information area, consists of blocks of data. The standard is a nominal 578 blocks, each containing 256 data words (nominally). In addition each block contains 10 control words.



DECtape Block Arrangement

The blocks permit digital data to be partitioned into groups of words which are interrelated while at the same time reducing the amount of storage area that would be needed for addressing individual words. A simple example of such a group of words is a program. A program can be stored and retrieved from magnetic tape in a single block format because it is not necessary to be able to retrieve only a single word from the program. It is necessary, however, to be able to retrieve different programs which may not be related in any way. Thus, each program can be stored in a different block on the tape.

Since DECtape is a fixed address system, the programmer need not know accurately where the tape has stopped. To locate a specific point on tape he must only start the tape motion in the search mode. The address of the block currently passing over the head is read into the DECtape Control and loaded into an interface register. Simultaneously, a flag is set and a program interrupt can occur. The program can then compare the block number found with the desired block address and tape motion continued or reversed accordingly.



DECtape Unit

CONTROLS & INDICATORS

REMOTE/OFF/LOCAL (rocker switch)	Placing this switch in one of the following positions accomplishes: a. REMOTE—disables the Fwd/Hold/Rev switch and places the transport under computer control (on-line).

b. LOCAL—enables the Fwd/Hold/Rev switch and removes the transport from computer control (off-line).

c. OFF—removes power from the reel motors and removes the transport from computer control.

→ ← Fwd/Hold/Rev (rocker switch: spring-loaded to Hold)	Placing this switch in the Fwd position (provided REMOTE/OFF/LOCAL is in LOCAL) moves the tape from left to right across the read/write head. When this switch is in the spring-loaded Hold position (provided REMOTE/OFF/LOCAL is in LOCAL), the tape remains stationary. Placing this switch in the Rev position (provided REMOTE/OFF/LOCAL is in LOCAL) moves the tape from right to left across the read/write head.
Address Select (0 to 7 thumbwheel switch)	Configures the transport logic to respond to the address indicated on the thumbwheel.
WRITE ENABLE/WRITE LOCK (rocker switch)	Placing this switch in the WRITE ENABLE position lights the WRITE indicator and allows a write operation. Placing this switch in the WRITE LOCK position turns off the WRITE indicator and prevents a write operation.
REMOTE SELECT (indicator)	Lights when the transport is in the remote (on-line) mode and is selected by the controller. Goes off when the transport is in the off or local (off-line) modes or is deselected by the controller.
WRITE (indicator)	Lights when the WRITE ENABLE/WRITE LOCK switch is in the WRITE ENABLE position. Goes off when the WRITE ENABLE/WRITE LOCK switch is in the WRITE LOCK position.

PROGRAMMING

All transport operations are controlled by the Control Unit from program instructions. The Control selects the transport, controls tape motion and direction, selects a read or write operation and buffers data transferred.

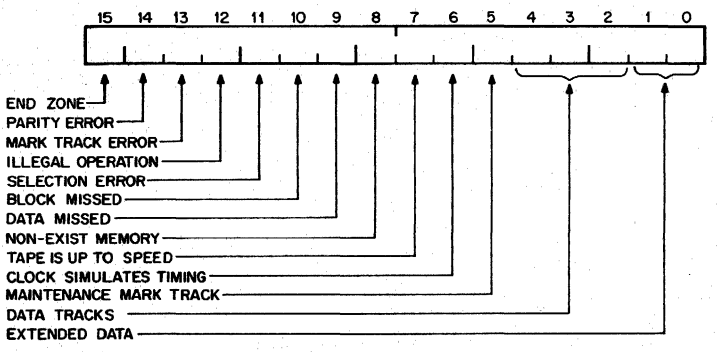
The Control can select any one of eight commands that control operation of the DECtape system. When the system is operated on-line, these commands are used for reading or writing data on the tape and for controlling tape motion. The desired command is selected by the program which sets or clears bits 3, 2, and 1 in the command register (TCCM) to specify an octal code representing the desired command.

The commands are:

OCTAL CODE	MNEMONIC	FUNCTION
0	SAT	Stops all tape motion.
1	RNUM	Finds the mark track code that identifies the block number on the tape in the selected tape unit. Block number found is available in the data register (TCDT).
2	RDATA	Assembles one word of data at a time and transfers it directly to memory. Transfers continue until word count overflow, at which time data is read to the end of the current block and parity is checked.
3	RALL	Reads information on the tape that is not read by the RDATA function.
4	SST	Stops all tape motion in selected transport only.
5	WRTM	Writes timing and mark track information on blank DECtape. Used for formatting new tape.
6	WDATA	Writes data into the three data tracks. 16 bits of data are transferred directly from memory.
7	WALL	Writes information on areas of tape not accessible to WDATA function.

All software control of the TC11 DECtape system is performed by means of five device registers. They can be read or loaded using any PDP-11 instruction that refers to their address.

REGISTERS
Control and Status Register (TCST) 777 340



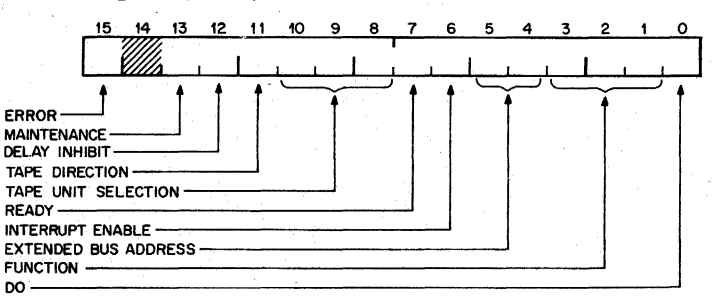
Effect of the Initialize (INIT) signal: clear bits 15, 14, 13, 10 through 7, 5, 1 and 0.

BIT	NAME	FUNCTION
15	End Zone (ENDZ)	Set to indicate that the selected tape unit is in an end zone region of the tape. It is cleared by loading a 0 into bit 15 (ERROR) of command register (TCCM), cleared by loading a 1 into bit 0 (DO) of the command register. Stops selected tape unit.
14	Parity Error (PAR)	Set to indicate a parity error. The parity error occurs during RDATA function if the calculated and written checksums disagree. Cleared in the same manner as ENDZ (bit 15).
13	Mark Track Error(MTE)	Set when an error occurred during decoding of the mark track. Stops selected tape unit. Cleared in the same manner as ENDZ.
12	Illegal Operation(ILO)	Set to indicate an illegal operation caused by a conflict in switch positions of the WRITE ALL, WRITE T&M, and WRITE ENABLE/WRITE LOCK switches. These conflicts are: a. WRITE LOCK on during WRTM, WALL, or WDATA modes

		b. WRITE T&M switch off during WRTM mode c. WRITE ALL switch off during WALL mode Stops selected tape unit. Cleared when switches reset to valid positions or when a non-conflicting operation is selected.
11	Selection Error(SELE)	Set when the program has either selected a non-existent tape unit or has attempted to select more than one tape unit. Stops selected tape unit. Disabled if MAINT bit (bit 13 in TCCM) is set or if function is SAT (bits 3, 2, and 1 in TCCM cleared). Cleared when unit selection switches set to valid positions or when another unit is selected.
10	Block Missed(BLKM)	Set when a block was missed. The transfer from read block number (RNUM) to read data (RDATA) or write data (WDATA) functions occurred too late. Also, indicates switch to RDATA from WDATA was too late. Cleared in the same manner as ENDZ.
9	Data Missed(DATM)	Set when data was missed. Request for data transfer not honored in time during RDATA, WDATA, WALL, or RALL. Cleared in the same manner as ENDZ.
8	Non-Existent Memory(NEX)	Set to indicate non-existent memory. This occurs when TC11 Controller is bus master and does not receive a SSYN response within 20 μs after asserting MSYN. Cleared in the same manner as ENDZ.
7	Tape Is Up To Speed(UPS)	Set when selected tape unit is up to speed required for proper operation. Cleared when UNIT SELECT or REV bit is changed. Set when unit is up to speed; set when MAINT bit (bit 13 in command register) is set, or when the selected function is WRTM.

6	Clock Simulates Timing(CLK)	Used to simulate timing track. May be loaded when MAINT bit is set. When CLK is set, produces TP1; when cleared, produces TPO.
5	Maint Mark Track(MMT)	Used to simulate the bit read from the mark track. May be loaded when MAINT bit is set.
4	Data Track 0(DT0)	Used to simulate output of the read amplifier when loaded; when read, reads the input to the write amplifier. When MAINT bit is set, DT0 loads into RWB2 and reads as RWB5.
		NOTE Bits 4, 3, and 2 function as six bits. When loaded, they simulate the read amplifier and are loaded into RWB2, RWB1, and RWB0. When read, they read the write amplifier inputs from RWB5, RWB4, and RWB3.
3	Data Track 1(DT1)	Functions the same as DT0 except loads into RWB1, reads as RWB4.
2	Data Track 2(DT2)	Functions the same as DT0 except loads into RWB0, reads as RWB3.
1	Extended Data 17(XD17)	Allows reading and writing on areas of the tape not accessible during 16-bit word transfers.
0	Extended Data 16(XD16)	

Command Register (TCCM) 777 342

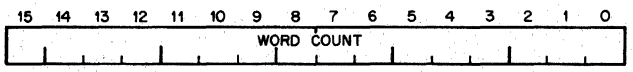


Effect of the Initialize (INIT) signal: clear bits 13 through 8, 6 through 1; set bit 7

Read only: bit 7
Write only: bit 0

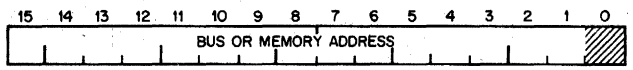
BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition which is the inclusive OR of all error conditions (bits 15-8 in TCST). Causes an interrupt if enabled (see bit 6). Clears errors (except ILO and SELE) when loaded with zero. Sets READY bit (bit 7).
13	Maintenance(MAINT)	Used for maintenance functions. When set, enables operation of bits 6-2 in the TCST.
12	Delay Inhibit(DINHB)	Set to inhibit the delay associated with bringing a tape unit up to speed when reselecting a tape unit known to be up to speed by a previous command.
11	Tape Direction(REV)	Specifies direction of tape motion. When set, specifies reverse motion; when cleared, specifies forward motion.
10-8	Unit Select	Specifies the number of the tape unit which is to receive the desired command. These three bits are set or cleared to represent an octal code which corresponds to the unit number of the tape unit to be used.
7	READY	Set when the Control is ready to receive a new command. Cleared when DO (bit 0) is set. Set when command execution is complete; set by ERROR (bit 15).
6	Interrupt Enable(IE)	Set to allow either READY (bit 7) or ERROR (bit 15)=1 to cause an interrupt.
5-4	Ext Bus Address(XBA)	Used to specify address line 17 (bit 5) or address line 16 (bit 4) in direct memory transfers. Increments with the TCBA.
3-1	Function Bits	Specifies a command to be performed upon the selected transport. Cleared by INIT to SAT.
0	DO	Set when a new function is given. Clears READY.

Word Count Register (TCWC) 777 344



BIT	NAME	FUNCTION
15-0	Word Count	Contains two's complement of the number of words to be transferred. This register counts the number of word transfers made during RDATA (read data) and WDATA (write data) functions. When one of these functions is initiated, the word count register is loaded. The register is incremented by 1 after each transfer. When the contents of the register equals all zeros, further transfers are inhibited. Cleared by INIT. (Note: This register must not be modified by using byte instructions. Use only word instructions when loading).

Bus Address Register (TCBA) 777 346



BIT	NAME	FUNCTION
15-1	Address	Specifies the bus or memory address to or from which data is to be transferred during RDATA (read data) and WDATA (write data) operations. These bits are used in conjunction with bits XBA17 and XBA16 in the command register. After each transfer (during RDATA and WDATA) is made, this register is incremented to advance it to the next word location. The XBA bits in TCCM participate in the incrementation; they are a logical extension to this register. Cleared by INIT. (Note: the bus address register must not be modified by using byte instructions when loading this register).

Data Register (TCDT) 777 350

BIT	NAME	FUNCTION
15-0	Data	Contains data word read from or to be written on the magnetic tape. These bits and bits XD17 and XD16 in the status

register form the 18 bits which correspond one to one with the six 3-bit characters read or written on the tape.
The data register accepts information under program control during WALL (write all) and WRTM (write timing and mark) operations. During RALL (read all) and RNUM (read block number) operations, the data register contains data read from the tape. During WDATA (write data) and RDATA (read data) operations, the data register is used to buffer information between the controller and memory. Cleared by INIT.
Note: The data register must not be modified by using byte instructions. Use only word instructions when loading this register.

PROGRAMMING EXAMPLES
The following two examples represent typical methods of programming the TC11 Control. The first example finds a specified block. The second example is a routine for writing data into a specific block.

Routine to find a specified block

```
;ENTER WITH R0 = BLOCK WANTED
;FINDS BLOCK IN FORWARD DIRECTION

SEARCH:  MOVE R0, BWANT
         SUB #3, BWANT          ;OFFSET
         MOV #4003, TCCM        ;UNIT 0, REVERSE, RNUM, DO

LOOP1:   BIT #100200, TCCM      ;CHECK READY AND ERROR
         BEQ LOOP1
         BMI ERROR
         SUB TCDT, #BWANT       ;CHECK BLOCK FOUND
         BLT SEARCH

FORWRD:  MOV R0, BWANT
         MOV #3, TCCM           ;UNIT 0, FORWARD ,RNUM, DO

LOOP2:   BIT #100200, TCCM      ;CHECK FOR READY AND
                                ;ERROR
         BEQ LOOP2
         BMI ERROR
         SUB TCDT, BWANT        ;CHECK BLOCK FOUND
         BGT FORWRD
         BLT SEARCH
         RTS PC                 ;RETURN WHEN BLOCK IS
                                 FOUND
```

```
ERROR:  TST TCST          ;TEST FOR ENDZ
        BMI LOOP3
        HALT              ;HALT ON ERROR OTHER
                          ;THAN
                          ;ENDZ

LOOP3:  BIT #4000, TCCM   ;CHECK DIRECTION
        BNE FORWRD        ;IF REV, NOW SEARCH
                          ;FORWARD
        BR SEARCH         ;IF FOR, NOW SEARCH
                          ;REVERSE
```

Routine to write 100 words into block 47 on unit 0

```
        MOV #47, R0       ;SET UP R0 FOR SUBROUTINE
                          ;CALL
        JSR PC, SEARCH    ;GO FIND BLOCK
        MOV #-100, TCWC   ;SET UP WORD COUNT
        MOV #BUFFER, TCBA ;SET UP BUS ADDRESS
        MOV #15, TCCM     ;GIVE COMMAND: WDATA, DO
                          ;UNIT 0, FORWARD

LOOP4:  BIT #100200, TCCM ;CHECK READY AND ERROR
                          ;ROR = 0
        BEQ LOOP4         ;BRANCH ON READY AND ERROR
        BMI ERR           ;BRANCH TO ERROR SERVICE
        .
        .
        .                 ;CONTINUE WITH PROGRAM
        .
        .
BUFFER: 0                 ;START OF BUFFER
```

SPECIFICATIONS FOR TC11-G

Main Specifications

Storage medium:	¾" wide magnetic tape (DECtape)
Capacity/tape reel:	147,968 words (144K)
Data transfer speed:	5,000 words/sec (200 μsec/word)
Drives/control, max:	8 (4 dual units)

Data Organization

Number of tracks:	10 (5 are redundant)
Blocks/reel:	578
Words/block:	256
Bits/word:	16
Recording method:	Manchester phase encoding
Recording density:	350 ± 55 bits/inch

Tape Motion

Speed:	97 ± 14 inches/sec (bi-directional)
Start time:	150 ± 15 msec
Stop time:	100 ± 10 msec
Turnaround time:	200 ± 20 msec

Tape Characteristics

Length:	260 ft
Type:	1 mil, Mylar sandwich, Mylar protected on both sides
Reel diameter:	3.9 inches
Handling:	Direct drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers.

Register Addresses

Control and Status	(TCST)	777 340
Command	(TCCM)	777 342
Word Count	(TCWC)	777 344
Bus Address	(TCBA)	777 346
Data	(TCDT)	777 350

UNIBUS Interface

Interrupt vector address:	214
Priority level:	BR6
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	10½" panel height for tape drive + 10½" for control unit

Power

Input current:	9 A at 115 VAC
Heat dissipation:	870 W

Environmental

Operating temperature:	15°C to 27°C
Relative humidity:	40% to 60%

Models

TC11-GA:	Dual tape drive and control,	115 VAC, 60 Hz
TC11-GB:	"	230 VAC, 50 Hz

SPECIFICATIONS FOR TU56

Mechanical

Mounting:	mounts in a std PDP-11 cabinet
Size:	10½" front panel height
Weight:	80 lbs

Power

Input current:	3 A at 115 VAC
Heat dissipation:	350 W

Prerequisite: TC11-G

Model

TU56: Dual tape drive

MAGNETIC TAPE, TM11

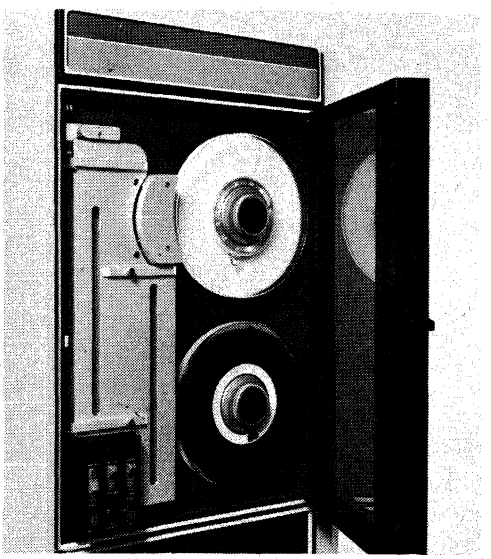
DESCRIPTION

The TM11 is a high-performance, low-cost magnetic tape system ideally suited for writing, reading, and storing large volumes of data and programs in a serial manner. Because the system reads and writes in industry-compatible format, information can be transferred between a PDP-11 and other computers. For example, a PDP-11 might be used to collect data and record it for later processing on a large-scale computer. The 10 1/2-inch tape reels contain up to 2400 feet of tape upon which over 180 million bits of data can be stored on high density 9-track tape or over 140 million bits can be stored on high density 7-track tape.

The TM11 employs read after write error checking to verify that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to insure no loss of data.

Tape motion is controlled by vacuum columns and a servo-controlled single-capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing.

A Magtape System consists of up to 8 tape transports and a Control Unit. Transports are capable of operation with seven or nine-track tape and a system can contain any combination of 7- and 9-track units. A TM11 includes a control unit and the first Tape Transport.



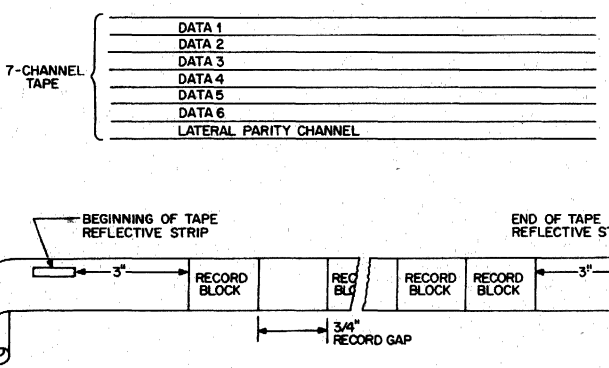
TU10 MAGTAPE UNIT

Operation

Reading and writing occurs when the tape is moving forward, but the control can move the tape to new positions in forward or reverse. For writing on tape, 8-bit data words are transferred from memory to a data buffer in the controller. The data buffer logic supplies the character to the tape transport write logic. For reading, the sequence is reversed; and information is read from tape as 6-bit characters for 7 track tape; (8 bits for 9 track tape) which are sent to the data buffer. When a word has been assembled in the data buffer, an NPR transfer is initiated to transfer the data buffer word into memory.

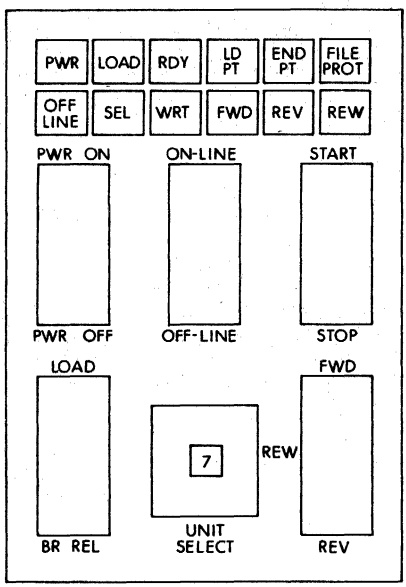
The 7- and 9-track system use 1/2-inch mylar base tape which is coated on one side with an iron oxide composition. The method of recording is non-return-to-zero (NRZ). A seven track tape includes six data channels and a lateral parity channel. Density modes of 200, 556, and 800 bytes per inch are selectable. Nine-track tape is similar to the 7-track tape, but operation is only in the 800 bpi mode and it has the industry standard cyclic redundancy character at the end of each record. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 inches of blank tape is wound on a reel and precedes the BOT and EOT strips; a gap of about 3 inches is left from the load point before writing can begin.

Each computer word contains two 8-bit tape characters. Record blocks are separated by 3/4 inch gaps on 7-track units and 1/2 inch gaps on 9-track units. The industry standard format has 7-track tape records containing from 24 to 4008 characters, and 9-track tape records from 18 to 2048 characters.



Magtape Format

CONTROLS & INDICATORS



Operator Control Box

Control Box Switches

PWR ON/PWR OFF — Applies power to entire TU10. Also, supplies power to the bus terminators if the tape transport is the most remote unit on the bus.

LOAD/BR REL

LOAD Position	Enables vacuum motor, which draws tape into the buffer columns.
Center Position	Disables vacuum motor; brakes are full-on.
BR/REL	Release brakes.

ON-LINE/OFF-LINE

ON-LINE Position	Selects remote operation.
OFF-LINE Position	Selects local operation.

FWD/REW/REV

FWD Position	Selects, but does not initiate, forward tape motion when transport is off-line
REW Position	Selects, but does not initiate, tape rewind when transport is off-line.
REV Position	Selects, but does not initiate, reverse tape motion when transport is off-line.

START/STOP

START Position	Initiates tape motion selected by FWD/REW/REV switch when transport is off-line.
STOP Position	Clears any motion commands when transport is off-line.

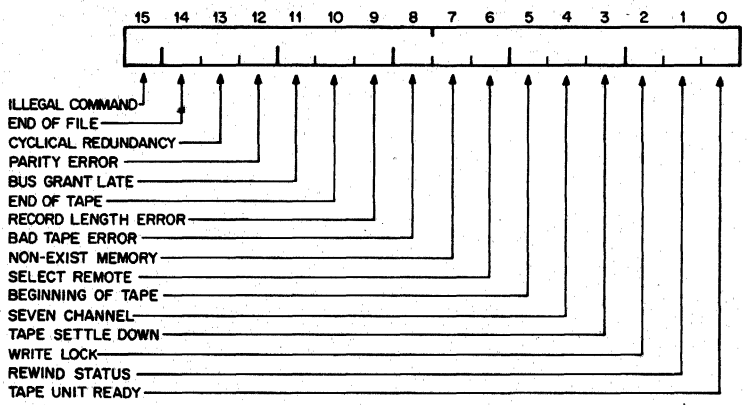
UNIT SELECT Selects the tape transport unit by number (0-7). This number is used in the program to address the tape transport.

Status Indicators

PWR	Indicates power has been applied to the transport.
LOAD	Indicates that vacuum is on and the tape is loaded into the buffer columns.
RDY	Indicates that the tape transport is ready (vacuum on and settledown delay complete); there is no tape motion.
LD PT	Indicates that the tape is at load point (Beginning of Tape)
END PT	Indicates that the tape is at end point (End of Tape).
FILE PROT	Indicates that write operations are inhibited because the write enable ring is not mounted on the file reel.
OFF-LINE	Indicates local operation by the control box.
SEL	Indicates the tape transport is selected by the controller (program).
WRT	Indicates that the program his initiated a write operation in the tape transport.
FWD	Indicates that a forward command has been issued.
REV	Indicates that a reverse command has been issued.
REW	Indicates that a rewind command has been issued.

REGISTERS

Status Register (MTS) 772 520



BIT	NAME	FUNCTION
15	Illegal Command	Set by any of the following illegal commands: 1. Any DATO or DATOB to the Command Register MTC during the tape operation period 2. A Write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1 3. A command to a tape unit whose SELECT REMOTE bit is a 0 4. The SELECT REMOTE (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition the CU ready bit remains set.

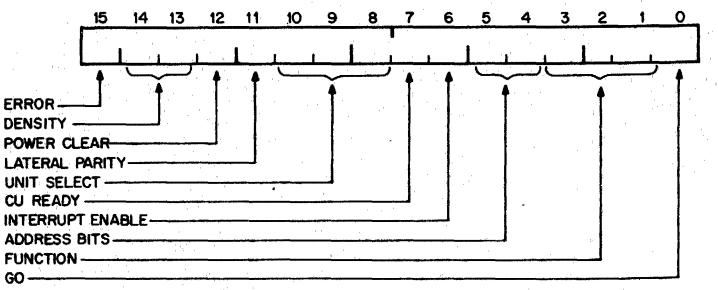
14	End of file (EOF)	Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit

		sets when the LPC character strobe is generated with the FILE MARK signal upon EOF detection.
13	Cyclical Redundancy Error (CRE)	Detected only during a read operation. It compares the CRC character read from tape with that regenerated during the same read operation. If they are not the same, CRC ERROR from the tape unit becomes a 1 which forces the CRE bit to a 1. However, the ERR bit does not become a 1 until the LPC character is detected.
12	Parity Error (PAE)	The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected. A parity error does not affect the transfer of data; that is, in a write operation, the entire record is tranferred to tape and in a read operation, the entire record is written into core memory. For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of 1's is detected on any track in the record. A lateral parity error occurs when an even number of 1's is detected on any character when PEVN is a 0, or an odd number of 1's is detected on any character when PEVN is a 1.
11	Bus Grant Late (BGL)	Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets

		simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.
10	End of Tape (EOT)	Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.
9	Record Length Error (RLE)	Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop. However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.
8	Bad Tape Error (BTE)	Sets when a character is detected (RDS pulse) during the gap shut-down or settling down period for all operations (except rewind). When BTE is detected the ERR bit is set immediately, and if INT ENB is set, an interrupt sequence is started.
7	Non-Existent Memory (NXM)	Set during NPR operations when the control unit is bus master, and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 micro seconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

6	Select Remote (SELR)	Cleared when the tape unit addressed does not exist, is off line, or has its power turned off.
5	Beginning Of Tape (BOT)	Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.
4	Seven Channel (7 CH)	Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.
3	Tape Settle Down (SDWN)	Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.
2	Write Lock (WRL)	Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.
1	Rewind Status (RWS)	Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.)
0	Tape Unit Ready (TUR)	Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

Command Register (MTC) 772 522



BIT	NAME	FUNCTION
15	Error (ERR)	Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.
14-13	Density (DEN 8, DEN 5)	Cleared on INIT.

BIT 14	BIT 13		
0	0	200 bpi	7 channel
0	1	556 bpi	7 channel
1	0	800 bpi	7 channel
1	1	800 bpi	9 channel

12	Power Clear (PCLR)	Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.
11	Lateral Parity (PEVN)	Set for even parity. Cleared for odd parity. A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.
10-8	Unit Select	Specifies one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.
7	CU Ready (CUR)	Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.
6	Interrupt Enable (INT ENB)	When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit. (i.e. CU READY or ERROR = 1)
5-4	Address Bits	Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are

an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

3-1 Function Bits — Selects 1 of 8 functions (programmable commands).

BIT 3	BIT 2	BIT 1	
0	0	0	Off line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write with Extended Interrecord Gap
1	1	1	Rewind

0 Go — When set, begins the operation defined by the function bits.

Byte Record Counter (MTBRC) 772 524
The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

Current Memory Address Register (MTCMA) 772 526
The MTCMA contains 16 of the possible 18 memory address bits. It is

used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 1 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

Data Buffer (MTD) 772 530
The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 thru 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

TU10 Read Lines (MTRD) 772 532
The memory locations allocated for the TU10 read lines are:

Bits 0-7 for the channels 7-0 respectively.

Bit 8 for the parity bit.

Bit 12 for the gap shutdown bit.

Bit 13 for the BTE error generation.

Bit 14 for the CRC, LPC character selector.

Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

Timer
TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SPECIFICATIONS FOR TM11

Main Specifications

Storage medium:	½" wide magnetic tape (industry compatible)
Capacity/tape reel:	5 to 20 million characters
Data transfer speed:	36,000 char/sec
Drives/control, max:	8

Data Organization

Number of tracks:	7 or 9
Recording density, 7 track:	200, 556, or 800 bits/inch; program selectable
9 track:	800 bits/inch
Interrecord gap, 7 track:	0.75 inches, min.
9 track:	0.50 inches, min.
Recording method:	NRZI

Tape Motion

Read/write speed:	45 inches/sec
Rewind speed:	150 inches/sec
Rewind time:	3 minutes, typ

Tape Characteristics

Length:	2,400 ft.
Type:	Mylar base, iron-oxide coated
Reel diameter:	10½ inches
Handling:	direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer changers with constant tape winding tension.

Register Addresses

Status	(MTS)	772 520
Command	(MTC)	772 522
Byte Record Counter	(MTBRC)	772 524
Current Mem Address	(MTCMA)	772 526
Data Buffer	(MTD)	772 530
TU10 Read Lines	(MTRD)	772 532

UNIBUS Interface

Interrupt vector address:	224
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	26" panel height for tape drive + 10½" for control unit
Weight (incl. cab):	500 lbs.

Power

Input current:	9 A at 115 VAC
Heat dissipation:	1000 W

Environmental

Operating temperature:	15°C to 27°C
Relative humidity:	40% to 60%

Miscellaneous

BOT, EOT Detection:	Protoelectric sensing of reflective strip, industry compatible
Skew Control:	Deskewing electronics included in tape transport to eliminate static skew
Write Protection:	Write protect ring sensing on tape transport
Data Checking Features:	Read after write parity checking of characters; Longitudinal Redundancy Check (7- and 9-channel); Cyclic Redundancy Check (9-channel)
Extended Features:	Self-test of Control with tape transport offline; core dump for 7-channel units.
Magnetic Head:	Dual gap, read after write.

Models

TM11-EA:	Tape transport and control,	9 track, 115 VAC, 60 Hz
TM11-ED:	"	9 track, 230 VAC, 50 Hz
TM11-FA:	"	7 track, 115 VAC, 60 Hz
TM11-FD:	"	7 track, 230 VAC, 50 Hz

SPECIFICATIONS FOR TU10

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	26" front panel height
Weight (incl. cab):	450 lbs.

Power

Input current:	9 A at 115 VAC
Heat dissipation:	1000 W

Prerequisite: TM11

Models

TU10-EE:	Tape transport,	9 track, 115 VAC, 60 Hz
TU10-EJ:	"	9 track, 230 VAC, 50 Hz
TU10-FE:	"	7 track, 115 VAC, 60 Hz
TU10-FJ:	"	7 track, 230 VAC, 50 Hz

UNIVERSAL DIGITAL CONTROL SUBSYSTEM, UDC11

DESCRIPTION

The UDC11 is a unique, highly flexible digital information input/output option for industrial and process control applications that use the PDP-11 computers.

The UDC11 interrogates or drives up to 252 directly addressable digital sense and control functional I/O modules or up to 4032 individual digital points. I/O functions include relay output, contact sense/interrupt counters, D/A converters, etc.

Automatic hardware logic within the UDC11 rapidly identifies interrupting inputs according to input module type and address, typically within 5 μsec.

The subsystem has been designed to take full advantage of the PDP-11 processor including the UNIBUS, and permits data to be read or loaded with a single move instruction.

Modular design and industrial packaging, including provisions for two wire, screw terminal input connectors, permit the UDC11 to be configured and modified according to application needs. The UDC11 is normally supplied as part of an IDACS-11 system; however it may be easily field added to existing PDP-11 systems.

Operation

The UDC11 operates under computer program control as a high level digital multiplexer, interrogating digital inputs and driving digital outputs located on directly addressable functional modules.

Sixteen bit data words are transferred directly between a functional module and a preassigned address location in the PDP-11 core memory by a single MOVE instruction when reading data in, or conversely from core to a module when sending data out.

Depending upon the module type selected, a 16-bit data output word can represent the single 16-bit digital word required by a D/A converter or 16 individual parts for contact closures, pulse outputs, etc.

Signal Conditioning and Functional I/O Modules

Each UDC11 system is tailored to meet a specific application by modularly assembling the appropriate modules.

Functional Input/Output Modules include Contact Interrupt, Contact Sense, Single Shot Driver, Flip-Flop Driver, Latching Relay, Single Shot Relay, Flip-Flop Relay, D/A Converters, and I/O Converters. Each of these modules plug interchangeably into the DD02 File Units which serve as universal interface units. The logical address of each unit can be determined by simple jumper wire connections, so that addresses are completely independent of the unit's physical location. Thus hardware additions or system program changes do not require the rewiring of input terminals.

Each Functional I/O Module requires a Signal Conditioning Module to normalize input voltages, provide fusing, and distribute field-supplied excitation and control power to the Functional I/O Modules.

Signal Conditioning Modules

a. Isolated Power BW400—Provides the interface between individual points on the functional I/O modules and field signals. Differential pair field wiring is terminated on screw terminals, one pair for each of the 16 points on the functional module.

b. Common Power BW402—Is similar to the BW400 except that a 17th input pair permits field supplied excitation or control power to be brought directly to the Signal Conditioning Module and distributed in parallel (common) to each of the 16 circuits on the module. The input is fused for 4 amperes. As with the BW400, the BW402 can supply signal conditioning and arc suppression, if required.

c. Output Driver Module BW403—Is similar to the BW402 Common Power Module except that a common ground return is provided for the open collector devices of the Single Shot Driver and Flip-Flop Driver (used with BW685 and BW687 only).

d. Contact Sense BW731—Provides electrically isolated, differential inputs for 16 external customer contacts or voltages. Isolation of up to 250 volts is achieved by a miniature read relay buffer on each input point. This module provides reliable and trouble free digital sensing in high noise environments. Also, its differential input characteristics are particularly suited for those applications where the ground of the customer's excitation voltage power supply may be different from (i.e., not directly strapped to) computer system ground.

e. Contact Interrupt BW733—Provides 16 electrically isolated, differential inputs for external customer contacts or voltages. It is electrically and mechanically similar to the BW731 Contact Sense Module. The BW733 is used to economically and reliably interface asynchronous devices requiring fast service from the processor because of priority or short duration.

Functional I/O Modules

a. Flip Flop Driver BM685—Provides 16 solid state buffered driver circuits for control of solenoid valves, relays, lamps, displays, etc. Capable of switching control voltages of up to + 55 VDC, the BM685 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver includes diode protection for inductive loads.

b. Single Shot Relay BM807—Provides 16 electrically isolated normally open mercury wetted contact outputs for initiating alarms, controls, and field relays. Normally closed operation can be achieved through a module jumper change performed in the field by the customer or at the factory on a special order basis. The duration of the output is trimpot adjustable from 2 msec to 2 seconds. A logical "1" energizes the relay coil for the pre-set pulse duration.

c. Single Shot Driver BM687—Provides a solid state pulse output to activate up to 16 field circuits such as lights, buzzers, or external control relays. Capable of switching control voltages of up to + 55 VDC, the BM687 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver also provides diode protection against inductive loads.

d. Latching Relay BM803—Provides "fail-safe" operation of 16 electrically isolated mercury wetted relay outputs. Magnetically latched, the relays remain set in the event of power failure, insuring the continuity and integrity of field circuits. Change of state can be effected only by a logical "1" or "0." Relay contacts are open when the relay is set by a logical "0," and closed when set by a logical "1." Contacts are rated at 2 amps, 250 volts, the product not to exceed 100 va.

e. Flip-Flop Relay BM805—Provides 16 electrically isolated normally open mercury wetted relay output contacts for buffered control of relays, contactors, displays, lamps, etc. Normally closed operation is possible by a module jumper change performed in the field by the customer or at the factory on a special order basis.

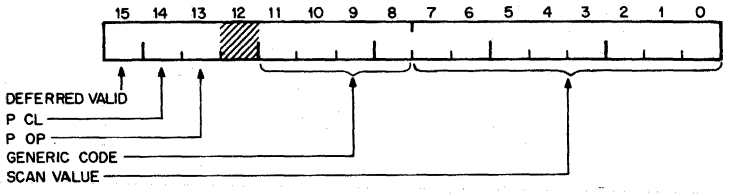
f. BW734 Counter Module—Is a 16-bit asynchronous binary up counter. An output buffer register is included which is updated after each counter increment. When the buffer is read (under program control), the update is inhibited, preventing any data change. The counter is parallel loading, enabling it to be preset under program control. Count down is accomplished by presetting 2's complement. May be used for Input or Output counting functions, stepping motor control, etc.

g. BA633 Digital-to-Analog Converter—Is interchangeable with any functional I/O module in the UDC11. It contains four complete channels of 10-bit digital-to-analog conversion. Single-ended output current or voltage is provided by one of the four signal conditioning modules listed below. Selection of a channel (1 of 4) and loading of data into the D/A buffer is accomplished by a single move instruction. The analog output remains constant until the channel is readdressed with new data. A separate H738A analog power supply is required for each group of up to four (16 channels) BA633. Power fail backup can be provided to maintain the analog output at its constant last value in the event of system or line power failure.

h. Digital-to-Analog Converter BA633 Signal Conditioning Modules—A signal conditioning module is required for each BA633. Each module contains four channels of signal conditioning and scales the four analog outputs of the BA633 to the required current or voltage range.

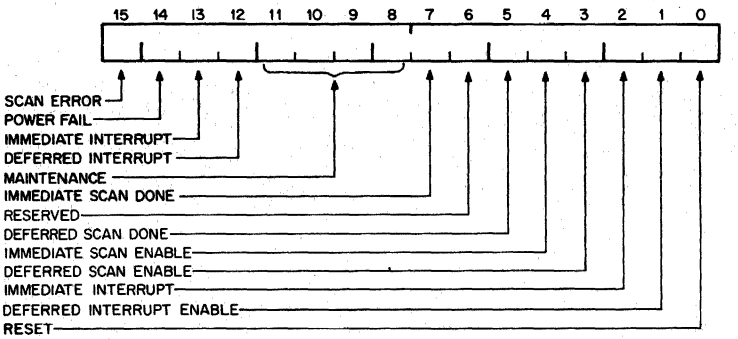
BA233	0 to + 10v @ 15 ma
BA234	+ 1v to + 5v @ 15 ma
BA235	4 ma to 20 ma into 750 ohms
BA236	10 ma to 50 ma into 300 ohms

REGISTERS
Scan Register (UDSR) 771 774



BIT	NAME	FUNCTION
15	Deferred Valid	Set to indicate that a deferred scan done was displaced by an immediate scan.
14	P CL	Set to indicate interest in contact closures from interrupt module.
13	P OP	Same as P CL but for contact openings.
11-8	Gen 3, 2, 1, 0	Generic code of interrupt module.
7-0	Scan Value	Address of interrupt module found as result of scan.

Control And Status Register (UDSR) 771 776



BIT	NAME	FUNCTION
15	Scan Error	Set by scan overflow in x, y, or wd; reset by initialize. Read only.
14	Power Fail	Set by power fail from expander H721B power supply; reset by initialize. Read only.
13	Intermediate Interrupt (IM INT)	Set by interrupt class I/O module; reset when interrupt class I/O module is reset; immediate. Read only.

12	Deferred Interrupt (DEF INT)	Same as IM INT but for deferred interrupt. Read only.
11	Maintenance Mode Word (M STP WD)	Maintenance mode of generating an interrupt module word address stop to test scanner. Read/Write.
10	Maintenance Mode Y (M STP Y)	Same as M STP WD but for Y address stop. Read/Write.
9	Maintenance Mode X (M STP X)	Same as M STP WD but for X address stop. Read/Write.
8	Maintenance Mode (M MODE)	Maintenance mode bit when set enables bit 02 to cause an IM INT or Bit 01 a DEF INT. Read/Write.
7	Immed. Scan Done	Set by an end of scan and IM INT; reset by initialize, clear done, or RIF. Read only.
5	Deferred Scan Done	Set by an end of scan and DEF INT; reset by initialize, clear done, or RIF.
4	Immed. Scan Enable (IM SCAN)	Set to enable immediate scan. Read/Write.
3	Deferred Scan Enable (DEF SCAN ENABLE)	Set to enable deferred scan. Read/Write.
2	Immediate Interrupt (IM INT)	Set to enable immediate interrupt; reset-set transition generates clear done signal. Read/Write.
1	Deferred Interrupt Enable (DEF INT ENABLE)	Set to enable deferred interrupt; reset-set transition generates clear done signal. Read/Write.
0	Reset (RIF)	Reset-set transition generates clear done and resets interrupting module; reset by initialize or delayed clear done. Read/Write.

NOTE: Initialize Resets All Bits.

Two types of service requests exist for interrupt producing functional I/O modules. These are "immediate" and "deferred."

The type of request serviced by the UDC11 is governed by program selection. If both requests are enabled the UDC11 will always service the immediate requests before servicing deferred requests.

Upon receipt of a service request by a functional module, the UDC11 controller determines the type of request and automatically initiates a scan to determine the address of the interrupt. Since the search is com-

pletely asynchronous and software overhead to test the controller with each data transfer prohibitive, programmed data transfer will take precedence over the hardware search.

Upon locating the address of the I/O module requesting service a hardwired four bit generic code is transferred to the scan register.

When the address and generic code are located the PDP-11 is interrupted on level BR6 if immediate service is required, or BR4 if deferred service is required. In either case the address and code may be read to the preassigned vector address to determine and call the appropriate subroutine for processing of the interrupt.

SPECIFICATIONS

Main Specifications

Modes of Operation:	Programmed Digital Output Programmed Digital Input Interrupt Controlled Input Interrupt Controlled Counting
Data Format:	16-bit I/O Data Words
Digital Inputs/Outputs:	252 16-bit words (4032 digital points) maximum
Type of Input/Output:	(see Functional I/O Modules and Signal Conditioning Modules)
I/O Module Selection:	Directly addressable
Interrupt Module:	Module type code and Module address
Interrupt Scan:	Locates address and type in 5 μsec typical (20 μsec, worst case)
I/O Data Rate:	10^5 16-bit words/sec
System Clock Rates:	3 available to each I/O word Line frequency, 6.3v AC 175 Hz—1.75 KHz adjustable 1.75 KHz—17.5 KHz adjustable
Cooling/Filtering:	Dust filters and blower fans in system cabinet.
Input Cabling:	Top or bottom entry, screw terminal connections. #18 A.W.G. 2 wire twisted pair/point max. size for fully wired cabinets. (Screw terminals will accommodate #14 A.W.G. wires.)

Register Addresses

Scan Register (UDSR)	771 774
Control and Status (UDCS)	771 776

UNIBUS Interface	
Interrupt vector address:	234
Priority level:	BR4 or 6
Bus loading:	2 bus loads
Mechanical	
Size:	each cabinet is 72"H x 21"W x 30"D
Weight:	750 lbs. (dual cabinet, 64 words or 768 points
Power (per cabinet)	
Input current:	15 A at 115 VAC, 40 to 440 Hz, single phase
Heat dissipation:	1700 W
Environment	
Operating temperature:	5°C to 50°C
Relative humidity:	10% to 90%

OSCILLOSCOPE, VR01-A

DESCRIPTION

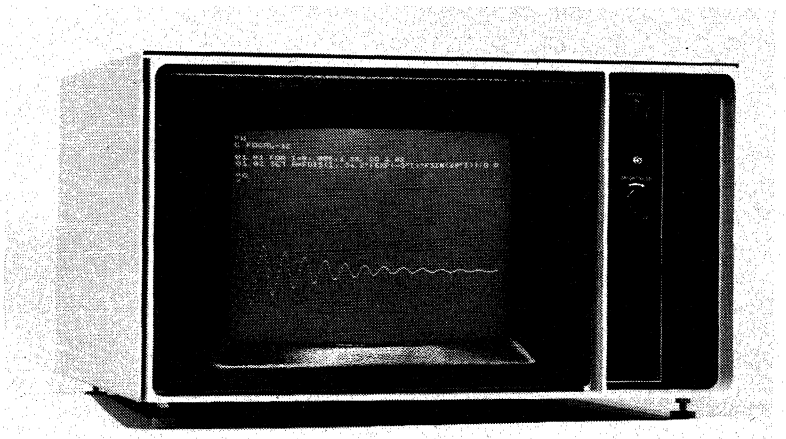
The VR01, a modified Tektronix type RM503 oscilloscope, provides accurate measurements in DC-to-450 kHz applications. It is a low-frequency, high sensitivity display and can be used for accurate curve plotting in the X-Y mode of operation.

For information concerning the control and programming refer to the AA11-D subsystem.

SPECIFICATIONS

Display Area:	8 x 10cm
Height:	7 in.
Width:	19 in.
Rack Depth:	17 in.
Net Weight:	30 lbs.
Display Rate:	45 kHz max.
	50 Hz min.
Display Time:	20 μs deflection time
	2 μs intensification time
Intensification Levels:	2

POINT PLOT DISPLAY VR14



VR14 POINT PLOT DISPLAY

DESCRIPTION

The VR14 Point Plot Display is a completely self-contained CRT display with a 6.75 x 9-inch viewing area in a compact 19-inch package. The VR14 requires only analog X and Y position information with an intensity pulse to generate sharp, bright point plot displays. Except for the CRT itself, the unit uses all solid state circuits with high speed magnetic deflection to enhance brightness and resolution. The intensity pulse may be time multiplexed or gated by a separate input to allow the screen to be timeshared between two inputs.

The VR14 is interfaced to the UNIBUS and controlled through the AA11-D digital/analog conversion subsystem.

SPECIFICATIONS

Main Specifications

Viewable Area:	6¾ x 9 in.
Spot Size:	⩽ 20 mils inside the usable screen area at a brightness of 30 foot-lamberts.
Jitter:	⩽ ± ½ spot diameter
Repeatability:	⩽ ± 1 spot diameter (Repeatability is the deviation from the nominal location of any given spot)

Gain Change:	From a fixed point on the screen, less than ± 0.3% gain change for each ± 1% line voltage variation.
Brightness:	⩾ 30 foot-lamberts: measured using a shrinking raster technique.
Linearity:	Maximum deviation of any straight line will be ⩽ 1% of the line length measured perpendicular to a best fit straight line.
Deflection Method:	Magnetic (70° diagonal deflection angle)
Focus Method:	Electrostatic
Shielding:	CRT is fully enclosed in a magnetic shield.
Overload Protection:	Unit is protected against fan failure or air blockage by thermal cutouts.

Mechanical

Mounting:	1 panel mounted unit
Size:	10½" front panel height
Weight:	75 lbs.

Power

Input current:	4 A at 115 VAC
Heat dissipation:	400 W

Environment

Operating temperature:	10°C to 50°C
Relative humidity:	10% to 90%

STORAGE DISPLAY, VT01-A

DESCRIPTION

The VT01-A Storage Display is a Tektronix Model 611 direct-view storage tube with a resolution of 400 stored line pairs vertically and 300 stored line pairs horizontally. Dot writing time is 20 μs, with a full screen erase time of 500 ms. The VT01 can display 30,000 discrete resolvable points.

The VT01-A is interfaced to the UNIBUS and controlled via the AA11-A and AA11-D conversion subsystem.

SPECIFICATIONS

Main Specifications

Resolution:	Equivalent to 400 stored line pairs along the vertical axis; 300 stored line pairs along the horizontal axis.
Erase Time:	0.5 seconds
Display Time:	Storage Mode—80 μs deflection time, 20 μs intensification time
	Non-Storage Mode—80 μs deflection time, 2 μs intensification time
Display Size:	8¼ Vertical x 6⅝ Horizontal
Display Rate:	10 kHz max. (storage mode)

Mechanical

Mounting:	1 table top unit
Size:	12"H x 12"W x 23"D
Weight:	50 lbs.

Power

Input current:	2 A at 115 VAC (1 A at 230 VAC)
Heat dissipation:	250 W

Environment

Operating temperature:	0°C to 50°C
Relative humidity:	10% to 80%

ALPHANUMERIC TERMINAL, VT05B

DESCRIPTION

The VT05B Alphanumeric Display Terminal, consisting of a CRT display and self-contained keyboard, can be used as a peripheral I/O device with a computer or as a stand-alone closed-circuit television monitor. In computer applications, the VT05 (with system software) can be used to compose, edit, and forward messages to the computer; retrieve and update alphanumeric data contained in the computer files; receive instructions and data from the processor; and perform on-line debugging. When performing these functions, the VT05 operates similarly to a teletypewriter, except that it is a soft copy device. The advantages of using the VT05 are: it is faster, quieter, more compact, easier to maintain, and considerably more reliable than an electromechanical teletypewriter.

Design Features

The VT05 is a totally self-contained desk-top unit. For ease of maintenance, seven easily replaced solid-state modules make up the entire circuitry of the VT05.

The VT05 has a human engineered CRT screen and input keyboard. The CRT can display up to 1440 very large characters (0.22" x 0.10") at one time. It can be read under most ambient light conditions. Brightness and contrast controls are readily accessible for individual operator adjustment. A special tinted glass shield eliminates glare. The input keyboard offers high input capability with virtually noiseless operation.

The distinctive flowing lines of the VT05 blend well with any decor.

Operational Characteristics

The VT05 is logically and electrically equivalent to the teletypewriter. It can be connected directly to modems, data phones, acoustic couplers and other EIA compatible devices. Or the VT05 may be connected directly to the computer via its 20 milliamp current loop teletypewriter interface. All the functions of the teletypewriter are duplicated so there is no need to modify program codes.

A single switch on the rear of the VT05 allows the operator to select transfer rates of 110, 150, 300, 600, 1200 and 2400 Baud. At the flick of another switch, the VT05 will change from a full duplex terminal to a half duplex one.

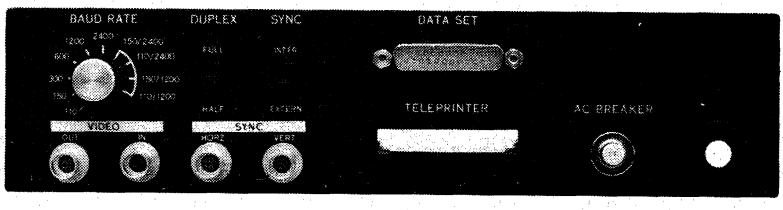
The VT05 keyboard can transmit in either of two modes — half ASCII or full ASCII. Half ASCII means that the terminal transmits in upper case alpha codes only. Full ASCII indicates the ability to transmit in both upper and lower alpha codes as well as all control characters.

A unique feature of the VT05 is direct cursor addressing. The cursor is a blinking underline showing where the next character will be displayed on the CRT. With direct cursor addressing, the cursor may be placed at any position on the screen by a computer instruction. This is very useful for filling in of fixed input formats.

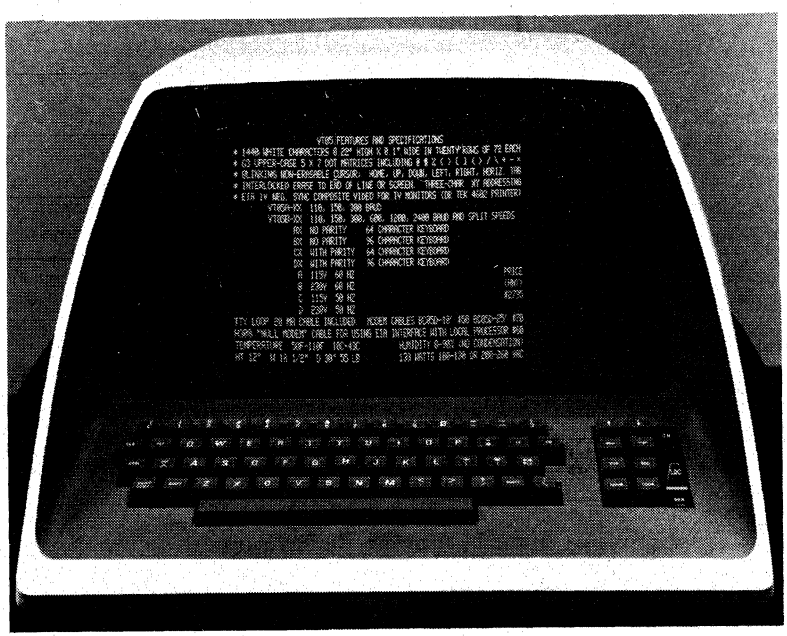
VT05

The VT05 can accept video input from a TV camera for simultaneous display of the video image and alphanumeric data from the computer. This capability can be very useful in training, teaching, and testing applications as well as factory, warehouse and process control.

The VT05 will also drive many slave monitors. This output capability is useful in controlling large closed circuit information display systems without the need for computer control.



Rear Control Panel of the VT05



VT05 Terminal

CONTROLS AND INDICATORS

Control or Indicator	Location	Function
Power ON/OFF Switch	Right-front	Applies power to the terminal.
LOCAL/REMOTE Switch	Right-front	In LOCAL mode, the terminal is off-line and data transmitted from the keyboard is input to the receiver logic by connecting the transmitter output to the receiver input. In REMOTE mode, data is transmitted from the VT05 to the computer while simultaneously receiving data from the computer for entry into the VT05 buffer memory (full duplex operation). If inputs are received from both the VT05 transmitter and the computer simultaneously (half duplex), the two inputs will be mixed or garbled.
FULL/HALF DUPLEX Switch	Rear Panel	Used to select FULL DUPLEX or HALF DUPLEX operation when LOCAL/REMOTE switch is in the REMOTE position.
CONTRAST Control	Right-hand side	Used to adjust the picture for contrast.
BRIGHTNESS Control	Right-hand side	Used to adjust the CRT brightness (intensity).
VERTICAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
HORIZONTAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
BAUD RATE Switch	Rear Panel	A ten-position switch used to select the terminal transmit/receive baud rates.

Baud Rate Switch

Switch Position	Transmit Rate	Receive Rate
Fully Counterclockwise	110	110
	150	150
	300	300
	600	600
	1200	1200
through	2400	2400
	150	2400
	110	2400
	150	1200
Fully Clockwise	110	1200

REGISTERS

The VT05 interfaces to the PDP-11 via the DL11 Controller. All software control of the DL11 Asynchronous Line Interface is performed by four device registers. These registers are assigned UNIBUS addresses and can be read or loaded with PDP-11 instructions that refers to their address.

Register	Mnemonic	Function
Receiver Status Register	RCSR	Provides detailed information on the keyboard status of the VT05, and the DL11 receiver logic. Status information includes such bits as receiver active (RCVR ACT) and receiver done (RCVR DONE). Also includes the interrupt enable bit that can be used to initiate interrupt sequences when RCVR DONE sets.
Receiver Buffer Register	RBUF	Holds the character received from the VT05 keyboard prior to transfer to the UNIBUS.
Transmitter Status Register	XCSR	Provides the interrupt enable bit and the transmitter ready (XMIT RDY) bit (meaning VT05 is ready to accept a character to be displayed). The transmitter logic can be monitored and an interrupt sequence initiated, if desired.
Transmitter Buffer Register	XBUF	Holds the character to be transferred to (displayed by) the VT05.

SPECIFICATIONS

Main Specifications

Transmission speed:	110 to 2400 Baud
Number of columns:	72
Number of lines:	20
Number of printing characters:	63 (upper case ASCII subset)
Data transmission:	EIA and 20 ma current loop compatible
Interface to PDP-11:	DL11

CRT Display

Screen size:	10⅛" x 7⅝"
Character displayable area:	8" x 6¼"
Character generation method:	5 x 7 matrix
Character Size	0.22 in. × 0.11 in.
Phosphor	P4 (white)
Deflection Type	Magnetic
Deflection Method	Raster Scan
Input Impedance (at VIDEO IN input)	75Ω ± 5%
Video Input Signal	0.9 to 2.2V with separate horizontal and vertical SYNC.
Sinusoidal Frequency Response	15 Hz to 12 MHz @ 3 dB point
Video Pulse Rise and Fall Time	30 ns (10% to 90% point), measured at cathode with 1.0V p-p input and 30V p-p output.
Video Output Amplitude	< 30V p-p (minimum), measured at cathode with 1.0V p-p input.
Resolution	Screen Center — 600 lines (minimum) Screen Corners — 400 lines (minimum) (using shrinking raster method)
Horizontal Sweep Frequency	15.6 kHz
Vertical Sweep Frequency	50 or 60 Hz (selectable)
Horizontal Retrace	11 μs (maximum)
Vertical Retrace	21 horizontal lines @ 15.6 kHz
High Voltage	11 kV (minimum) @ 50 μA beam current @ 24 Vdc power supply adjustment
High Voltage Regulation	12 MΩ (maximum), with a beam current change from 50 to 150 μA @ 24 Vdc power supply adjustment.
Horizontal Linearity	± 5%, measured at 0.5 in. intervals.
Vertical Linearity	± 7%, measured 0.75 in. intervals.
CRT Refresh Rate	50 or 60 Hz

Mechanical

Mounting:	1 table top unit
Size:	12"H x 19"W x 30"D
Weight:	55 lbs.

Power

Input current:	2 A at 115 VAC
Heat dissipation:	130 W

Environment

Operating temperature:	10°C to 43°C
Relative humidity:	8% to 90%

Models

Optional variations available in the VT05 Alphanumeric Display Terminal are listed below.

VT05B — X X

X:
- A: 115V; 60 Hz
- D: 230V; 50 Hz

X:
- A: no parity; half ASCII-Keyboard
- B: no parity; full ASCII-Keyboard
- C: with parity; half ASCII-Keyboard
- D: with parity; full ASCII-Keyboard

CHAPTER 5

UNIBUS THEORY AND OPERATION

5.1 INTRODUCTION

5.1.1 Single Bus

The UNIBUS is a single, common set of signal wires that connects the processor, memory, and all peripherals. Addresses, data, and control information are transmitted along the 56 lines of the bus. Figure 5.1 is a simplified block diagram of the PDP-11 System and UNIBUS.

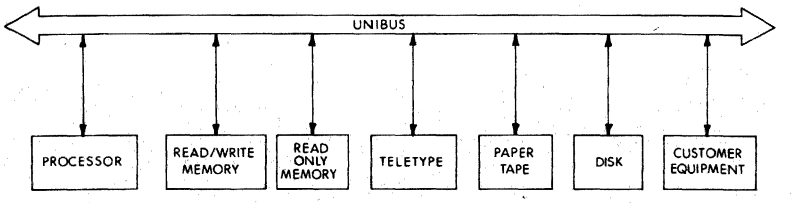


Figure 5.1 PDP-11 System Simplified Block Diagram

The form of communication is the same for every device on the UNIBUS. The processor uses the same set of signals to communicate with memory and peripheral devices. Peripheral devices also use this set of signals when communicating with the processor, memory, or other peripheral devices.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers. Therefore, peripheral device registers may be manipulated as flexibly as memory by the processor. This is an especially powerful feature, considering the special capability of PDP-11 instructions to process data in any memory location as though it were an accumulator.

5.1.2 Bidirectional Lines

Most UNIBUS lines are bidirectional: therefore, the input lines can also be driven as output lines. This means that a peripheral device register can be either read or can be used for transfer operations. Thus, the same register can be used for both input and output functions.

5.1.3 Master-Slave Relation

Communication between two devices on the bus is in a master-slave relationship. During any bus operation, one device has control of the bus. This device, the bus master, controls the bus when communicating with another device on the bus, called the slave. A typical example of this relationship is the processor, as master, transferring data to memory, as

slave. Master-slave relationships are dynamic. The processor, for example, can pass bus control to a disk. The disk, as master, then communicates with a slave memory bank.

The UNIBUS is used by the processor and all I/O devices; thus, a priority structure determines which device obtains control of the bus. Consequently, every device on the UNIBUS capable of becoming bus master has an assigned priority. When two devices which are capable of becoming bus master, have identical priority levels and simultaneously request use of the bus, the device that is electrically closest to the processor receives control.

5.1.4 Interlocked Communication

Communication on the UNIBUS is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Therefore, communication is independent of the physical bus length and the response time of the master and slave devices. The maximum transfer rate on the UNIBUS with optimum device design, is one 16-bit word every 400 ns, or 2.5 million 16-bit words per second.

5.2 PERIPHERAL DEVICE ORGANIZATION AND CONTROL

Registers in peripheral devices are assigned addresses similar to memory; thus, all PDP-11 instructions that address memory locations can become I/O instructions. Data registers in devices can take advantage of all the arithmetic power of the processor. The PDP-11 controls devices differently than most computer systems. Control functions are assigned to addressable registers, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Status conditions are also handled by the assignment of bits within this register, and the status can be checked by program instructions. There is no limit to the number of registers that a device may have, providing an unlimited flexibility in the design and control of peripheral equipment.

5.3 TRANSFER OF BUS MASTER

A device (other than the processor) that is capable of becoming bus master generally requests use of the bus for one of two purposes:

a. To make a non-processor transfer of data directly to or from memory, or

b. To interrupt program execution and force the processor to jump to a specific address where an interrupt service routine is located.

5.3.1 Transfer Request Handling

The request and granting of bus mastership is performed in parallel with data transfers on a completely independent set of bus lines. Thus, while one device is using the bus, the next request is being checked for priority and the next user is being assigned. Because of this time parallelism, successive data transfers by different master devices can occur at the full UNIBUS speed.

5.3.2 Priority Structure

When a device capable of becoming bus master requests use of the bus, the handling of that request depends on the location of that device in the priority structure. The following factors must be considered to determine the priority of the request:

a. The processors priority is set under program control to one of eight levels usings bits 7, 6, and 5 in the processors status register. These three bits set a priority level that inhibits granting of bus requests on the same or lower levels.

b. Bus requests from external devices can be made on any one of five request lines. A non-processor request (NPR) has the highest priority, and its request is granted by the processor between bus cycles of an instruction execution. Bus request 7 (BR7) is the next highest priority and bus request 4 (BR4) is the lowest. The four lower level priority requests (BR7 to BR4) are granted by the processor between instructions. When the processor priority is set to a specific level, all bus requests on that level and below are ignored. For example, if the processor priority is 6, requests on BR6 or any other lower level are not granted.

c. When more than one device is connected to the same bus request line, the device electrically nearer the processor has a higher priority than the device further away. Any number of devices can be connected to a specific BR or NPR line.

When a device other than the processor gains control of the bus, it uses the bus to perform either a data transfer or an interrupt request.

5.3.3 Data Transfer

Direct memory or device access data transfers can be accomplished between any two peripherals without processor supervision. These are called NPR level data transfers. Normally, NPR transfers are made between the memory and a mass storage device, such as a disk.

During NPR transfers, it is not necessary for the processor to transfer the information between the memory and the mass storage device. The bus structure enables device-to-device transfers, thereby allowing customer-designed peripheral controllers to directly access other devices (such as disks) on the bus. This direct access capability permits operations such as a disk directly refreshing a CRT display.

An NPR device provides extremely fast access to the bus and can transfer data at high rates once it gains control. The processor state is not affected by this type of transfer; therefore, the processor can relinquish bus control while an instruction is in progress. This release of the bus can occur in general, whenever the processor is not using the bus. However, the bus can never be released between cycles of a read-modify-write sequence. An NPR device in control of the bus transfers 16-bit words or 8-bit bytes to memory at the same speed as the memory cycle time.

5.3.4 Interrupt Requests

Devices that gain bus control with one of the bus request lines (BR7,

BR6, BR5, BR4) can take full advantage of the power and flexibility of the processor by requesting an interrupt. The entire instruction set is then available for manipulating data and status registers. When a device servicing program is to be run, the task being performed by the processor is interrupted, and the device service routine is initiated. After the device request has been satisfied, the processor returns to its former task. Note that interrupt requests can be made only if bus control has been gained through a BR priority level. An NPR level request must not be used for an interrupt request.

5.3.5 Interrupt Procedure

This paragraph provides an example of an interrupt operation. Assume that a peripheral requires service and requests use of the bus at one of the four BR levels. The operations required to service the device are as follows:

a. Priorities permitting, the processor relinquishes bus control to the device.

b. When the device gains control of the bus, it sends the processor an interrupt command and a unique address of a memory location which contains the starting address of the device routine. (This is called the interrupt vector address.) Immediately following this pointer address is a word (located at vector address + 2) to be used as the new processor status (PS) word.

c. The processor pushes the current processor status word and then the program counter (PC) value on the processor stack. The stack is pointed to by register R6.

d. The new PC and PS (the interrupt vector) are taken from the address specified by the device, and the device service routine is initiated.

NOTE

These operations are performed automatically and no device polling is required to determine which service routine to execute.

e. The device service routine can cause the processor to resume the interrupted process by executing the Return from Interrupt (RTI) instruction which pops the two top words from the processor stack and transfers them back to the PC and PS registers.

f. A device service routine can, in turn, be interrupted by a higher priority bus request any time after the first instruction of the routine has been executed.

g. If such an interrupt occurs, the PC and PS of the current device service routine are automatically pushed onto the stack, and the new device routine is initiated as before. This nesting of priority interrupts can continue to any level; the only limitation is the amount of memory available for the processor stack.

5.4 UNIBUS SIGNAL LINES

The PDP-11 UNIBUS consists of 56 signal lines, see Table 5-1. All devices, including the processor, are connected to these lines in parallel

(see Figure 5.2). The bidirectional nature of 51 signal lines permits signals to flow in either direction. The remaining five unidirectional lines are used for granting priority bus control.

UNIBUS pin assignments are listed in Appendix B.

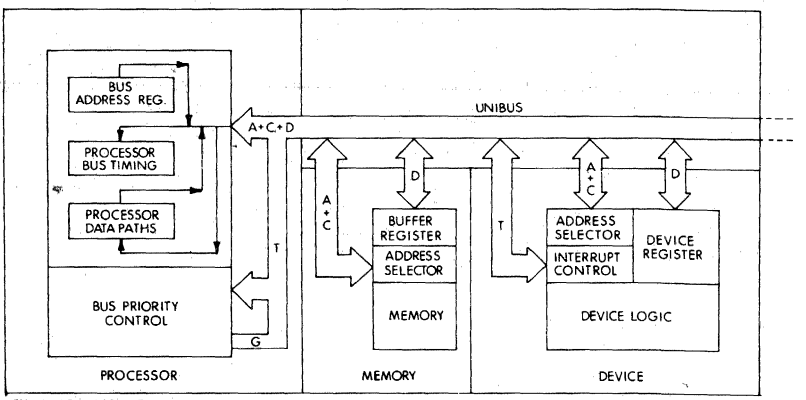


Figure 5-2 PDP-11 Interface Block Diagram

TABLE 5-1 UNIBUS SIGNALS

Name	Mnemonic	No. of Lines	Function
Address	A	18	Selects slave device.
Data	D	16	Information transfer
Control	C	2	Type of data transfer
Master Sync	MSYN	1	Timing control for data transfer.
Slave Sync	SSYN	1	
Parity	PA, PB	2	Byte parity Error Indication.
		40	
Bus Request	BR	4	Priority bus control
Bus Grant	BG	4	
Non-processor Req	NPR	1	Direct Memory Access control.
Non-processor Grant	NPG	1	
Slave Acknowledge	SACK	1	Bus control
Interrupt	INTR	1	
Bus Busy	BBSY	1	
		13	
Initialize	INIT	1	Resets system
AC Line Low	AC LO	1	Power detection
DC Line Low	DC LO	1	
		3	

The Bus Grant signals, BG (4 lines) and NPG are uni-directional lines. They are not wire-ORed as the rest of the UNIBUS lines, but are received and redriven by each device.

Simplified and standardized control logic is made possible by using separate dedicated lines for all signals. In any data transfer, data is transmitted and received; the master device provides the address of the slave device; and control and timing signals are provided. Each of these three functions occurs on a distinct set of bus lines, eliminating the use of additional hardware and extra timing states to distinguish between address, control information, and data.

All bus activity is asynchronous and depends on interlocking of control signals. In every case, a signal from a slave device is generated in response to a signal from a master device, and the master signal is dropped in response to the slave signal. The complete elimination of critical self-timing gives the bus the flexibility to operate with devices running at different speeds.

5.5 DATA TRANSFER

Forty bidirectional bus lines are used for data transfer. In a data transfer, one device is a bus master and controls the transfer of data to or from a slave device. The processor may be bus master when no other device is using the bus, and it is master for all data transfers involved in normal instruction processing.

5.5.1 Signals used in Data Transfer

A <17:00>* Address Lines. The 18 address lines are used by the master device to select the slave (a unique memory or device register address) with which it will communicate.

The reason for 18 address lines is to extend the total memory capability to 262,144 bytes. The bit format of the 18 signals is shown in Figure 5-3.

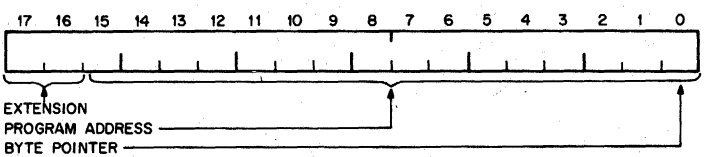


Figure 5-3 Address Line Bit Format

Lines A <17:01> specify a unique 16-bit word. In byte operations, A00 specifies the byte being referenced. If a word is referenced at X (X must be even, since words can be addressed on even boundaries only), the low-order byte can be referenced at X and the high-order byte at X + 1.

*Angle brackets enclose groups of lines; A < 17:00 > = A17 through A00 inclusive.

Only 16 bits are normally supplied by programs as memory reference addresses. In the basic processor, lines A17 and A16 are asserted (forced to 1) whenever the processor attempts to reference an address between 160000 and 177777; i.e., where A15 = A14 = A13 = 1. Thus, the processor converts this 16-bit address to a full 18-bit bus address.

Peripheral devices are normally assigned an address from within the bus address allocations from 760000-777777 (program addresses, 160000-177777).

D <15:00> Data Lines. The 16 data lines are used to transfer information between bus master and slave.

The bit format is shown in Figure 5-4.

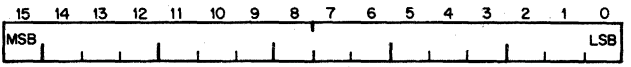


Figure 5-4 Data Line Bit Format

C<1:0> Control Lines. These two bus signals are coded by the master device to control the slave in one or four possible data transfer operations.

CI	CO	Operation
0	0	DATI—Data In
0	1	DATIP—Data In, Pause
1	0	DATO—Data Out
1	1	DATOB—Data Out, Byte

MSYN Master Synchronization. A control signal used by the master to indicate to the slave that address and control information is present.

SSYN Slave Synchronization. The slave's response to the master (usually a response to MSYN).

PA, PB These lines are used to indicate a parity error. The slave sets PA = 0 and PB = 1 to indicate a parity error on a DATI; PA = 0 and PB = 0 indicates no parity error. PA = 1 and PB = 0 or 1 are reserved for future extensions.

5.5.2 Direction of Data Transfer

There are 4 types of bus-data transfers. The bus master determines one of the four data transfers by asserting the proper code on the C<1:0> lines.

NOTE

All data transfers are with reference to the master device; data-in is always from slave to master, and data-out is from master to slave. For example, when the processor (master) loads data into memory (slave), a data-out bus operation is performed.

Bus-Data Transfer Transactions

Name	Mnemonic	C Lines C1	C0	Function	Octal Code
Data in	DATI	0	0	Data from slave to master	0
Data in, pause	DATIP	0	1	Inhibits restore cycle in destructive read-out devices; Pause flip-flop is set which inhibits clear cycle on following DATO (B). Must be followed by DATO or DATOB.	1
Data out	DATO	1	0	Data from master to slave.	2
Data out, Byte	DATOB	1	1	Transfers data from master to a single byte in slave. Data transferred on D<15:08> for A00 = 1; D<07:00> for A00 = 0.	3

The DATI and DATIP transactions request transfer of data from a slave, the address of which is specified by A<17:00>, from the master. Both transfers use the data lines to carry the data. There is no distinction made by the slave as to whether the transfer is used for byte or word data. The slave places the data on D<15:00>. It is the function of the master device to retrieve the data from the proper lines: low-order byte register with A00 = 0 from D<07:00>; high-order byte register with A00 = 1 from D<15:08>; or word register from D<15:00>. The DATIP operation is identical to the DATI, except DATIP is used to inform the slave device that this is the first part of an in-modify-out cycle. A DATIP normally sets a pause flag in the destructive read-out device (i.e., core memory) which inhibits the restore cycle. The DATIP must be followed by a data-out cycle (DATO or DATOB), and the master must retain bus control until it is completed. In nondestructive readout devices (i.e., flip-flops), the DATI and DATIP are treated identically.

The DATO and DATOB operations transfer data from the master to the slave. A DATO is used to transfer a word to the address specified by A<17:01>. The slave ignores A00 and the master places data on D<15:00>. A DATOB is used to transfer a byte of data to the address specified by A<17:00>. Line A00 = 0 indicates the low-order byte, and the master places the data on lines D<07:00>; A00 = 1 indicates the high order byte, and master places the data on lines D<15:08>.

5.5.3 Conventions and Definitions

Signal Transmission

All UNIBUS signals are buffered by Transmitter and Receiver circuits before being used by any interfacing device. Most signals are bi-directional, having both a Transmitter and a Receiver within the same device. Figure 5-5 shows a typical signal. Note that within the same device, a bi-directional signal appears in two different physical places, at the input of a Transmitter and at the output of a Receiver. All UNIBUS signals mentioned in this chapter will imply reference within the Transmitter/Receiver device interface, and signals will be differentiated by:

(T) = transmitted signal (at input of Transmitter)
(R) = received signal (at output of Receiver)

Levels

A signal, such as MSYN, will be considered activated when asserted. For simplicity, timing waveforms will be shown for logic levels, rather than voltage levels. The higher level will correspond to the assertion level, and the lower level will be the cleared level.

Asserted = Logic 1 = TRUE = higher level
Cleared = Logic 0 = FALSE = lower level = (negation)

Skew

When two separate signals are sent from one device to another device starting at the same time, there can be a time difference in the receipt of these signals by the second device, even if similar circuitry and transmission medium are used. This time difference (or time uncertainty) is called skew. It is guaranteed to be less than 75 nsec for the UNIBUS. Figure 5-6 shows an example.

If signals A & B represent 2 Data lines on the UNIBUS, there could be a maximum time difference (skew) of 75 nsec in the receipt of these signals. Signal A could precede signal B by 75 nsec, or it could arrive later than B by 75 nsec.

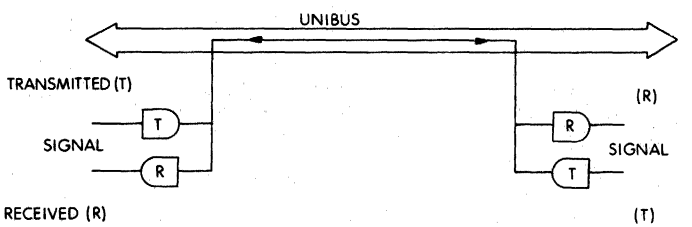
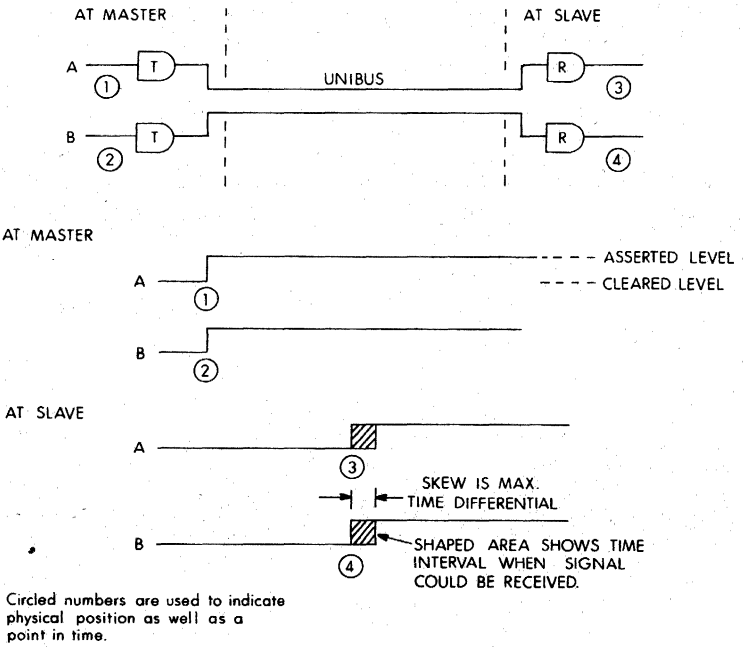


Figure 5-5 Bi-directional Signal



NOTE: Circled numbers are used to indicate physical position as well as a point in time.

Figure 5-6 Example of Skew

5.5.4 Equivalent Logic at the Slave

To allow asynchronous data transfer between master and slave, 2 interdependent timing signals are used, MSYN and SSYN. Simplified, equivalent logic at the slave interface to the UNIBUS is shown in Figure 5-7.

The sequence of events is:

1. Address, Control, (and Data) are sent from the master.
2. After a delay, to make sure lines have settled and address decoding has been performed, MSYN is sent. MSYN is a gating (or strobing) signal for the Address and Control lines. It is always cleared before Address and Control are changed.
3. SSYN is the acknowledging response to MSYN and means that
   (a) Address has been recognized by a device register (or memory), and
   (b) The action requested has been performed; data has been accepted or data has been placed on the UNIBUS.

The logic shows 2-input AND gates and D-type flip-flops. The information present on the D (data) input is stored in the flip-flop when the C (clock) input is activated.

Single lines have been shown for the different groups of signals (A,C, & D) to simplify the diagram.

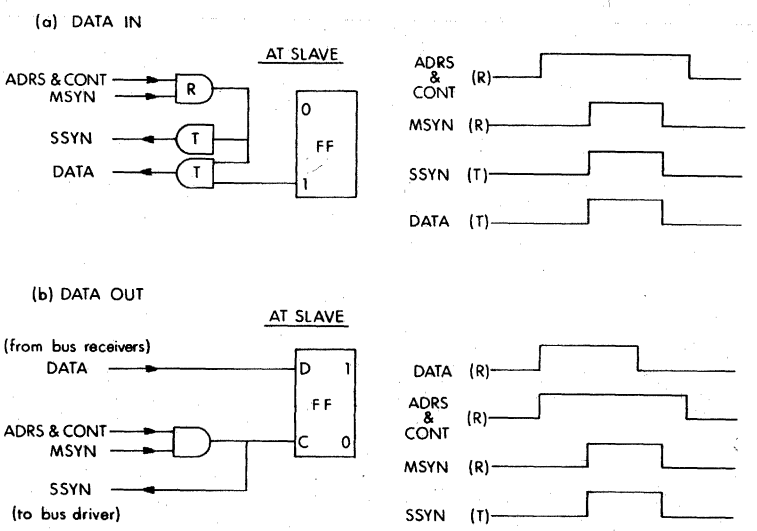


Figure 5-7 Simplified Slave Logic

5.5.5 Data Transfer Timing

The design of the UNIBUS imposes certain timing restrictions although transfers are interlocked. Responsibility for these timing restrictions has been assigned to the master to simplify the slave design.

In all transfers, it is assumed that there can be a maximum 75-ns skew due to driver, receiver, and transmission line tolerances. In other words, the coincident assertion of two lines at the transmitter inputs of one device could result in a maximum difference of 75-ns in the occurrence of those signals at the receiver outputs in another device.

Because of this possible skew, the master always delays its MSYN signal to ensure that MSYN does not reach the slave device prior to valid data or addresses. In addition, the MSYN signal is further delayed to allow 75 ns for decoding by the slave device. The master also must not drop the A (address) or C (control) lines until 75 ns after MSYN has been dropped to guarantee that there are no spurious selections. Note, however, that when a slave transmits data to a master (DATI or DATIP), the deskew and decode time delay must be made by the master.

5.5.6 DATI and DATIP Bus Transaction (See Figure 5-8)
All data transfer functions are with reference to the master device; therefore, data-in (DATI) indicates data transfer from the slave to the master.

a. The master device places the address (or location) of the slave device on the A lines, and places 0 on the C lines (C1 = 0, C0 = 0) for a DATI, or 1 for a DATIP (C1 = 0, C0 = 1). The master device then waits 150 ns (minimum): 75 ns to allow for worst-case signal skew, and 75 ns to allow internal logic in the slave devices to decode the address.

b. The slave device decodes the address and control bits to determine if the slave is to participate in a data transfer.

c. If the slave device from a previous bus transaction still has SSYN asserted, the master device waits until SSYN is clear. MSYN is asserted when SSYN is clear and the delay from step **a** is complete.

d. When the MSYN signal is received by the slave device, the device prepares the data for transmission to the master. For devices such as core memory, this means performing a read cycle. For flip-flop registers, the data is available immediately.

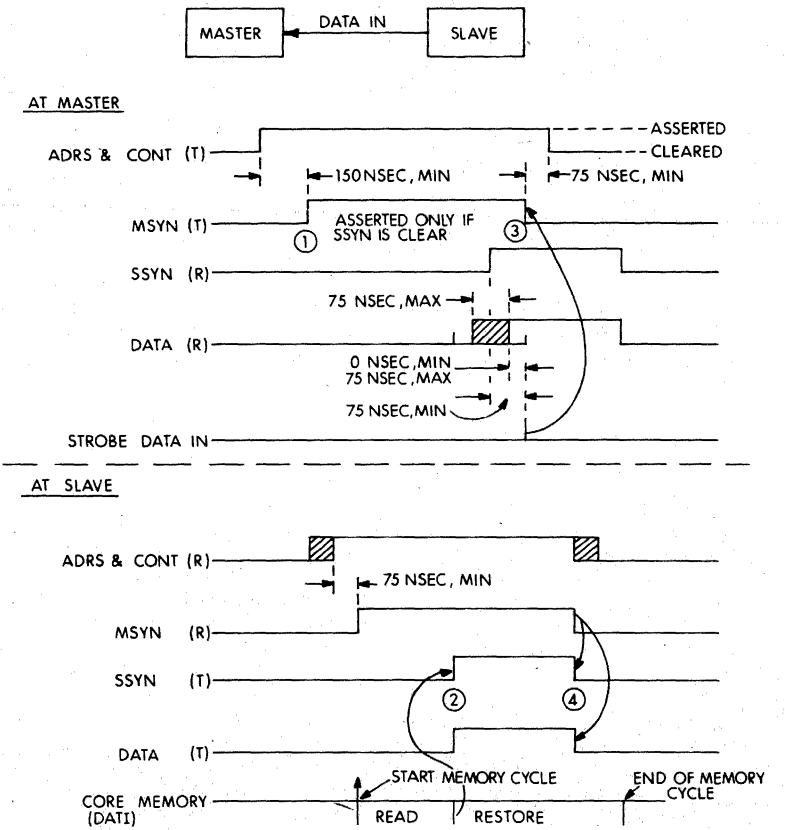
e. When data is available, the slave places data on the D lines and asserts SSYN. If the slave is a destructive read-out device, it enters a restore cycle, if the command was a DATI; for a DATIP, the slave sets a pause flag and waits for modified data before performing a write cycle.

f. The master device receives SSYN and the data. After a 75-ns minimum delay to allow for skew, the master device strobes the data and clears MSYN. If the processor is master and SSYN is not received within 5 to 20 μsec (depending on the particular PDP-11 processor), time-out occurs, the MSYN signal is cleared automatically by the processor, and an error trap occurs.

g. After a 75-ns minimum wait, to ensure that no spurious device selections occur as various bits of the address change while MSYN is still asserted, the A and C lines are cleared.

h. When MSYN is cleared, the slave clears the D lines and SSYN; the bus is now free for other use.

i. The master receives the cleared SSYN, which signals the end of the current bus transaction. If an output transfer follows (a DATO or a DATOB must follow a DATIP), step **a** of the DATO(B) can start now. If another input transfer follows, it can start after step **g** is complete; however, MSYN cannot be asserted until the conditions of step **c** are met.



NOTE: The circled numbers are referred to in Table 5-2. The timing diagram is not drawn to scale.

Figure 5-8 DATI & DATIP Timing Diagram

Interlocking Control Signals for Data In

The sequence of the interlocking timing signals are shown by dashed lines in Table 5-2.

(a) = asserted
(c) = cleared

Table 5-2 Data In Control Sequence

	Master	Slave	Meaning
①	MSYN (a)		Decode address and send data on D lines.
②		SSYN (a)	Address has been recognized and data is on D lines.
③	MSYN (c)		Remove data on D lines.
④		SSYN (c)	Data is removed.

5.5.7 DATO and DATOB Bus Transactions (See Figure 5-9)
Because all data transfers are with reference to the master device, a data out (DATO) indicates data transfer from the master to the slave.

a. The master device places the address (or location) of the slave device on the A lines, the data on the D lines, and asserts 2 on the C lines (C1 = 1, C0 = 0) for a DATO or asserts 3 on the C lines for a DATOB (C1 = 1, C0 = 1).

b. After a 150-ns minimum wait (75 ns to allow for worst case signal skew, and 75 ns to allow internal logic in the slave device to decode the address) the master device asserts MSYN if the bus is inactive (SSYN is clear).

c. The slave decodes A<17:00> and, if this is the assigned address of the slave, it responds to MSYN by taking in the data and then asserting SSYN. For a DATO, the slave accepts a full word; for a DATOB, the slave accepts one byte as determined by A00. For consecutive operations with the same slave device, the slave may have to complete an internal action (such as a restore or write cycle) before responding. If the slave is a destructive readout device with the pause flag set (indicating the previous bus transaction was a DATIP), the slave immediately begins a write cycle.

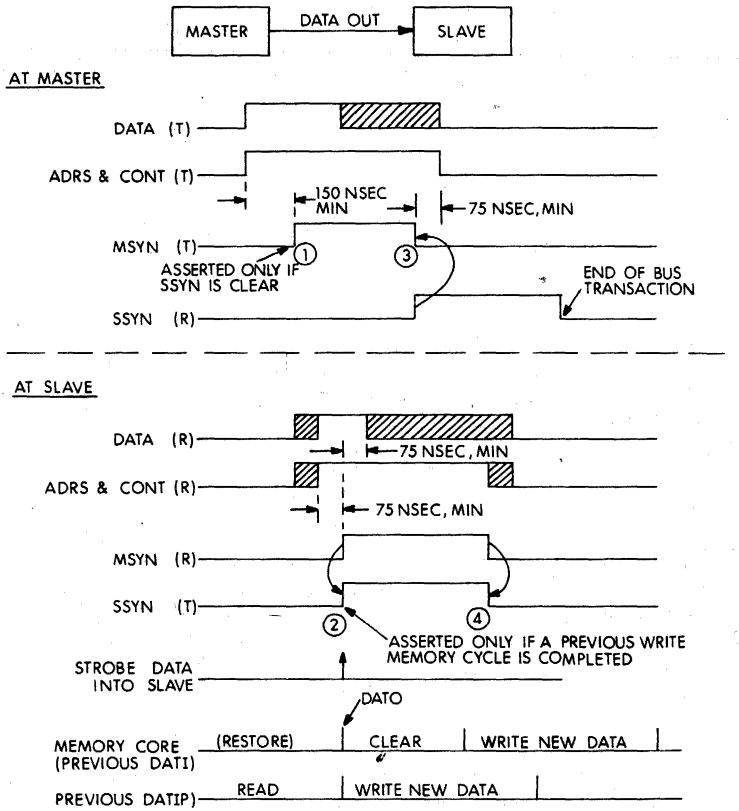
d. The master device receives SSYN and clears MSYN. If the processor is master and SSYN is not received within 5 to 20 μsec (depending on the particular PDP-11 processor), time out occurs, the MSYN signal is cleared automatically by the processor, and an error trap occurs.

e. After a 75-ns minimum wait, the master clears the A and C lines.

f. The slave device receives cleared MSYN and clears SSYN.

g. The master receives cleared SSYN which signifies the end of the bus transaction. A new bus transaction can begin at step **e** of a DATO or DATOB, and the master can assert MSYN at step **g**, when SSYN is cleared.

> **CAUTION** (For slave devices on DATO)
> Data on the D lines is guaranteed valid for 75 μsec minimum after SSYN is asserted. Data is not guaranteed valid when the slave receives negated MSYN.



NOTE: The circled numbers are referred to in Table 5-3.

Figure 5-9 DATO & DATOB Timing Diagram

Table 5-3 Data Out Control Sequence

	Master	Slave	Meaning
①	MSYN (a)		Decode address and accept data.
②		SSYN (a)	Address recognized and data stored.
③	MSYN (c)		Response to SSYN.
④		SSYN (c)	Bus is now free.

5.5.9 Timing Examples

To illustrate the operating speed of the UNIBUS when performing a data transfer, assume a DATO operation to a device that has a flip-flop register. A typical transmitter-bus-receiver delay time is 75 ns. A flow diagram of the transfer procedure is shown in Figure 5-10.

The bus master places address, control, and data information on the UNIBUS, waits 150 ns, and then asserts MSYN. After a worst case propagation delay of 75 ns, the slave recognizes MSYN and clocks the data into its register. Since the 75-ns propogation delay includes the transmitter and receiver delays, the time required to turn MSYN around into SSYN is literally 0. Also, since the data preceded MSYN by 150 ns (worst case skew is only 75 ns), there is ample preset time for the data input to the slave device flip-flop register.

When the master sees SSYN, it clears its MSYN control (nominal time, 25 ns) and then waits 75 ns before clearing or changing address and control information. Additional DATO(B) cycles may proceed at this time provided SSYN is cleared before MSYN is again asserted. This means that a sustained DATO transfer rate of 400 ns/word may be maintained. This is equivalent to a transfer rate of 40 million bits per second.

Figure 5-11 is a typical timing flow diagram for a DATI transfer. The procedure for a DATI transfer is essentially the same as for a DATO transfer with four exceptions:

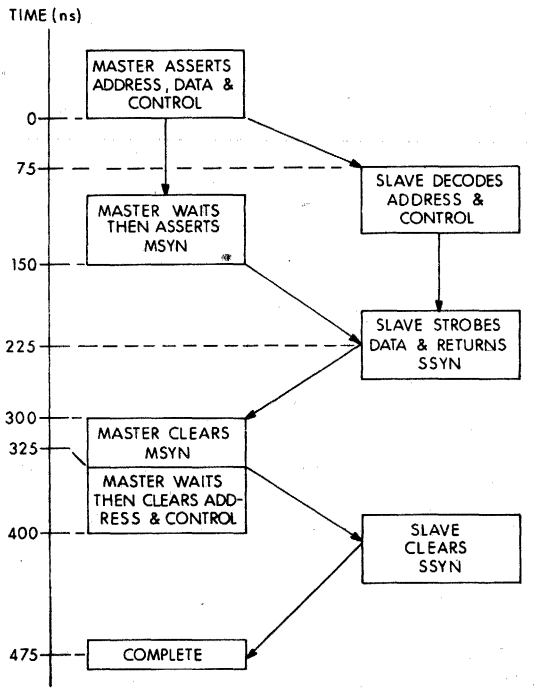
a. The master asserts only address and control information.

b. The slave gates data onto the bus simultaneously with the return of SSYN.

c. The master must wait 75 ns (to allow for skew between SSYN and DATA) before clearing MSYN and strobing data.

d. The slave clears data when it clears SSYN.

The DATI cycle allows sustained transfer rates of 450 ns-word which is equivalent to 35.2 million bits/second.



NOTES:

Worst case propagation delay of 75ns is shown.
Total time = 475ns for a single transfer.
Next cycle may begin at 400ns when master may assert new address and control
Maximum sustained transfer rate is 2.5 million words/sec.

Figure 5-10 Typical DATO Timing Flow

5.6 PRIORITY TRANSFER

5.6.1 Signals used in Priority Transfer

The UNIBUS contains 13 lines classified as priority transfer lines. Five of these are priority bus request lines (BR<7:4>,NPR) and five are the corresponding grant lines (BG<7:4>,NPG) which the processor uses to respond to a specific bus request. Each device of the same priority level passes a grant signal to the next device on the line, unless it has requested bus control; in this case, the requesting device blocks the signal from the following devices and assumes bus control. In addition, there are three other control lines: SACK, BBSY, and INTR. All 13 lines are described below.

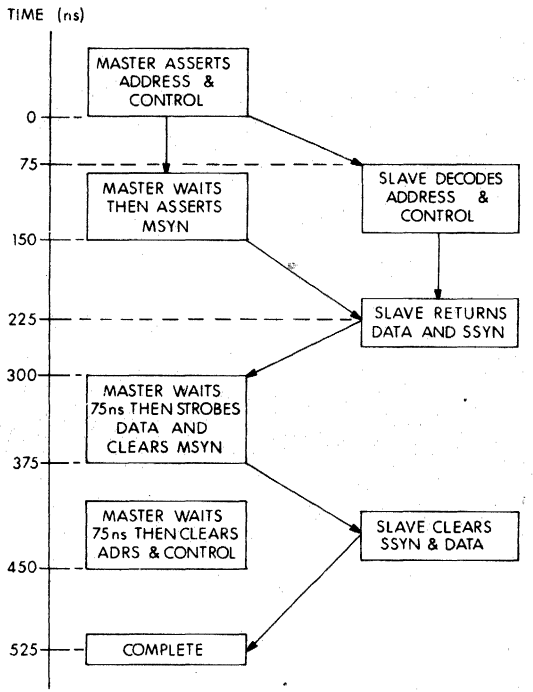


Figure 5-11 Typical DATI Timing Flow

BR <7:4> Bus Request Lines. These four bus signals are used by peripheral devices to request control of the bus.

BG <7:4> Bus Grant Lines. These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.

NPR Non-Processor Request. This signal is a bus request from a peripheral device to the processor.

NPG Non-Processor Grant. This signal is the processor's response to an NPR. It can occur whenever the CPU is not using the bus.

SACK — Selection Acknowledge. SACK is asserted by a bus-requesting device that has received a bus grant. Bus control passes to this device when the current bus master completes its operation.

INTR — Interrupt. This signal is asserted by the bus master to start a program interrupt in the processor.

BBSY — Bus Busy. This signal is asserted by the master device to indicate bus is being used.

5.6.2 Transfer of Control

Transfer of bus control from one device to another is determined by priority arbitration logic, which is part of the processor. Requests for the bus can be made at any time (asynchronously) on the bus request (BR) and non-processor request (NPR) lines. The arbitration logic checks for an NPR request on a regular basis (since these requests take precedence over processor use of the bus), unless the previous operation was a DATIP. If an NPR is present, the logic issues an NPG signal and receives a selection acknowledge (SACK) signal in return. This procedure occurs simultaneously with the current data transfer. When the device scheduled to become the new bus master is selected, it waits for the present master to clear bus busy (BBSY); then, the newly selected device becomes bus master and asserts BBSY.

A similar procedure occurs at the end of each instruction when the priority arbitration logic checks the bus request lines against the processor priority (as determined by bits <7: 5> of the processor status register) and the priority logic issues a grant on the corresponding line. Thus, one of the four levels of BR requests is granted by the processor between instructions unless the instruction currently being executed causes an internal trap (either an error or trap instruction). In this case, BR requests are not granted until completion of the first instruction following the trap sequence. The highest request is always granted first (if the processor priority level is lower than the request level). The grant signals always pass serially through each device connected to the corresponding level in the system. If a device makes a request, it blocks the signal transmission to the next device on the line; otherwise, it passes the signal on.

This causes the device closest to the processor to be the highest sub-priority on each request level.

5.6.3 Priority Transfer

The signal sequence by which a device becomes selected as next bus master is the priority transfer (PTR) bus operation (see Figure 5-12). This operation does not actually transfer bus control; it only selects a device as next bus master. The sequence of events is as follows:

a. The device that needs control of the bus asserts the BR (or NPR) line assigned to it.

b. The processor receives one or more BR signals. These signals enter a priority arbitration system, which compares BR levels with the processor priority levels and against the NPR. If a request has the

highest priority entering the arbitration system, and the SACK line is clear, the processor asserts the corresponding BG (or NPG) line. NPG is asserted anytime, while BG is asserted only at the end of the current instruction.

c. Each device on the asserted BG line passes the BG signal, unless it is requesting bus control.

d. The first device on the line which has BR asserted responds to the BG by asserting SACK, blocking the BG signal from following devices, and clearing its BR.

e. The processor receives the SACK signal and clears BG. (If SACK, is not received within 5 to 10μs, time out occurs and the bus grant is cleared automatically by the processor.)

f. The current bus master, when finished with the bus, clears BBSY.

g. The selected device, which is the new bus master, asserts BBSY when BBSY, BG, and SSYN are clear at the end of the previous data transfer. INTR may be asserted at this time, if the new bus master is interrupting.

h. SACK is dropped at the same time INTR is asserted if the device is interrupting. If the device is to transfer data first, the SACK signal is dropped prior to the start of the last bus cycle that the device does, see Figure 5-14.

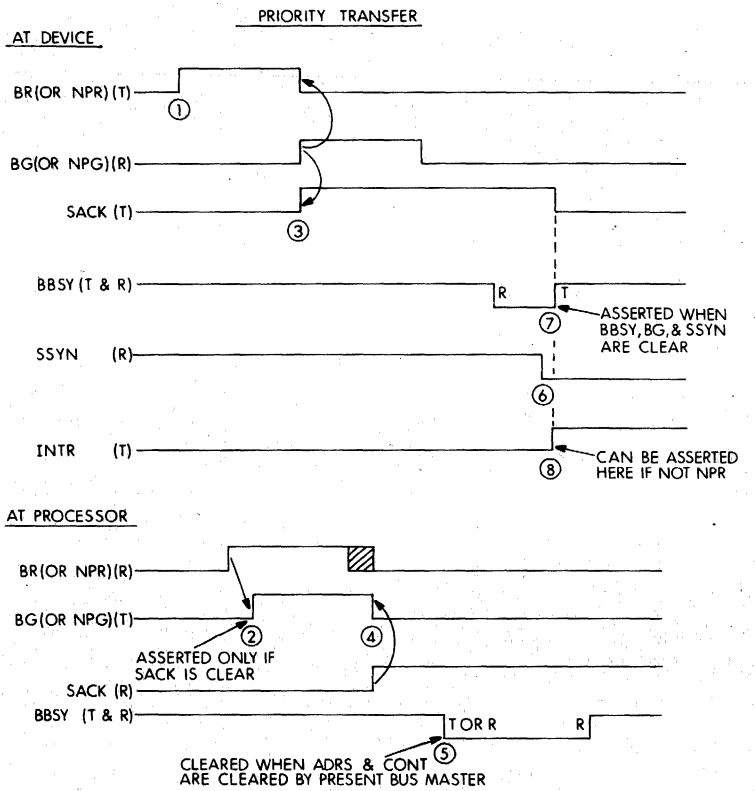
i. When the new bus master has completed its last data transfer, it clears BBSY. A new bus master then takes control of the bus. If no device is selected (SACK is clear), the processor may assert BBSY and use the bus. If, instead of clearing BBSY in a passive release, the device asserts INTR, the processor conducts an INTR bus transaction. This is called active release of the bus.

CAUTION

Since an NPR is granted within an instruction, and the interrupt and following processor response would destroy information held in the processor, devices granted bus control through an NPR must not attempt a processor interrupt.

NOTE

During the time a master device has control of the bus, it must either issue MSYN or terminate with an interrupt to provide reclocking of the priority arbitration logic in the processor. This affects only certain models of the PDP-11/20 and PDP-11/15 processors.



NOTE: Circled numbers are referred to in Table 5-4.

Figure 5-12 Priority Transfer Timing Diagram
(nominally, for processor master)

Table 5-4 Priority Transfer Control Sequence

	Processor	Device	Meaning
①		BR (a)	Request bus mastership.
②	BG (a)		Request granted, slave can take over during instruction (NPR), or after instruction (BR).
③		SACK (a)	Acknowledge receipt of BG or NPG.
④	BG (c)		Response to SACK by processor.
⑤	BBSY (c) (from previous master)		Address and Control lines are clear.
⑥	SSYN (c) (from previous slave)		Bus is now free.
⑦		BBSY (a)	New master (requesting device) has control of the bus.
⑧		INTR (a)	Direct processor to go to interrupt service routine. Read vector address on D lines.

5.6.4 Interrupt Operation

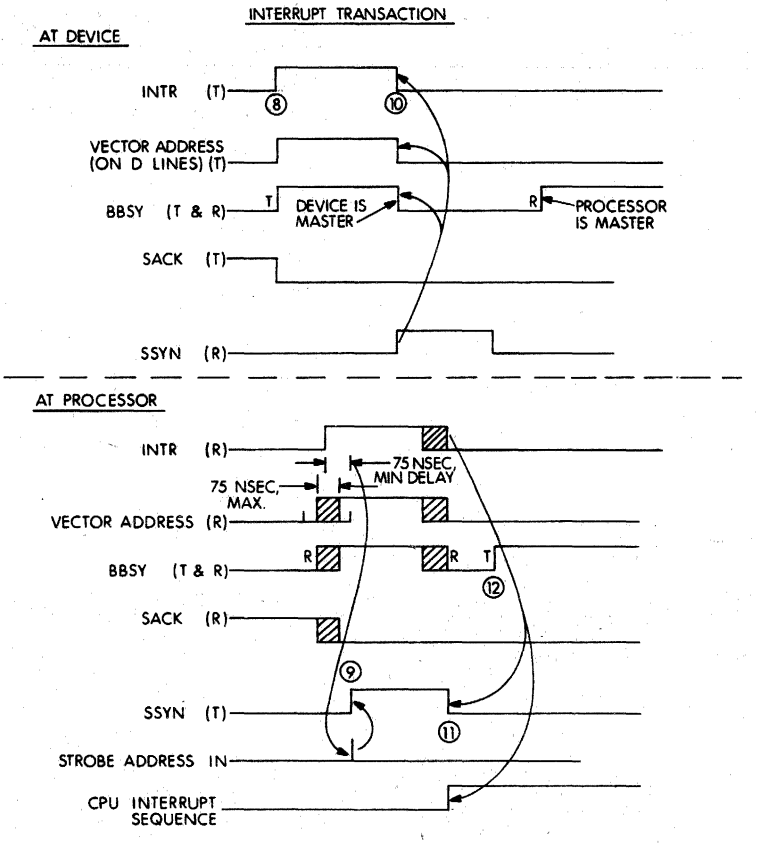
A device may cause the interrupt operation to occur any time it gains bus control with one of the BR levels (see Figure 5-13). It is usually accomplished immediately on becoming bus master; however, it may follow one or more data transactions on the bus.

a. If immediate interrupt operation is to be initiated, a device which has been selected as bus master asserts INTR and a vector address on the D lines, at the same time that it clears SACK and asserts BBSY. If data transfers occur prior to interrupt then SACK must remain asserted until INTR is asserted. If the device has been making data transfers prior to the interrupt, it should assert SACK through the last cycle, see Figure 5-14.

b. The processor receives the INTR signal, waits 75 ns for deskew to ensure that all bits of the interrupt vector address are available, and asserts SSYN when the data is read in.

c. The bus master (interrupting device) receives SSYN and clears INTR, the D lines, and BBSY. This constitutes active release of the bus to the processor.

d. The processor clears SSYN when INTR is cleared, and enters the interrupt sequence to store the contents of the current PC and PS registers and replace them with the contents of the locations specified by the vector address.



NOTE: Circled numbers are referred to in Table 5-5.

Figure 5-13 Interrupt Timing Diagram

Table 5-5 Interrupt Control Sequence

	Processor	Device	Meaning
⑧		INTR (a) DATA (a)	Direct processor to go to interrupt service routine. Read vector address on D lines.
		SACK (c)	Cleared after INTR; or on data transfer, prior to start of last bus cycle the device uses.
⑨	SSYN (a)		Vector address has been read in.
⑩		INTR (c)	Active release of the bus by the device.
		DATA (c)	Vector address cleared.
		BBSY (c)	Allow processor to become bus master.
⑪	SSYN (c)		Response to INTR (c), address can be removed from D lines.
⑫	BBSY (a)		Processor is now bus master.

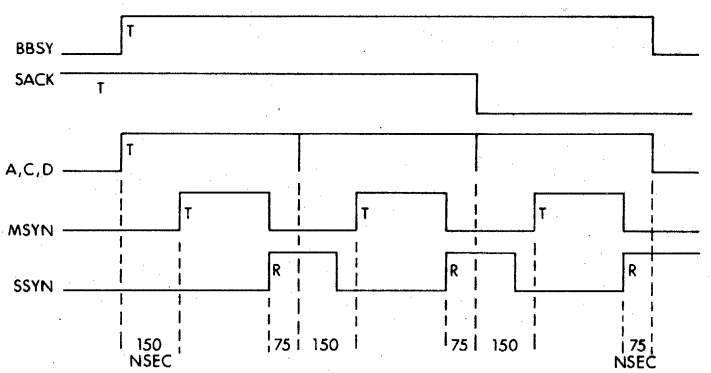


Figure 5-14 Device Multi-Word Tranfers

5.7 MISCELLANEOUS CONTROL LINES

There are three additional lines on the UNIBUS which may be used by all devices. These lines are: Initialize, AC low, and DC low:

INIT — Initialize. This signal is asserted by the processor when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. In the latter case, INIT is asserted following the

power fail service routine while power is going down, and again when power comes up. INIT may also be used to clear and initialize all peripheral devices at the same time by means of the RESET instruction.

AC LO — AC Line Low. This is an anticipatory signal which starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss. When AC LO is cleared, the power up instruction sequence in the processor begins. It is the programmer's responsibility to make certain that the trap vector is loaded with a pointer to the power fail routine. If this is not done, an undefined sequence results.

DC LO — DC Line Low. This signal, which emanates from the power supply, is available to all System Units on the UNIBUS. Each power supply must furnish both AC LO and DC LO signals, and be able to hold these lines at ground (less than 0.8 volts) when power is off to that supply, even if other equipment tries to pull up the lines. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply. Devices such as core memories use the DC LO signal to inhibit further operations. The DC LO signal is normally cleared before AC LO when power is coming up and is asserted after AC LO when power is going down. Note that the power fail trap is initiated by AC LO only and that the DC LO signal is used by the processor to cause INIT on the bus.

Refer to Figure 5-15.

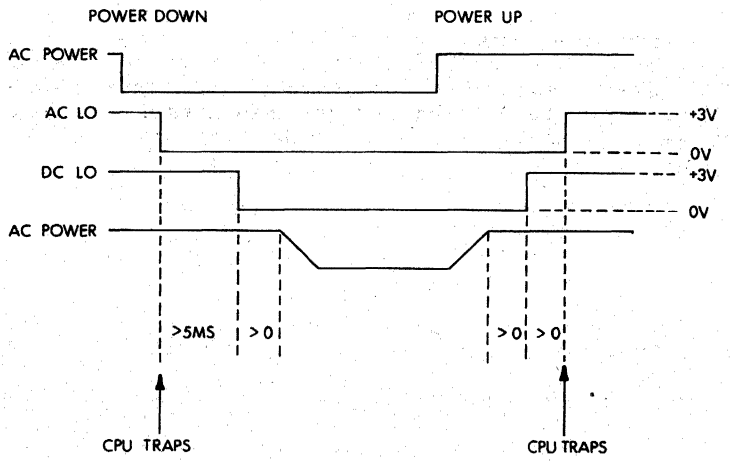
5.8 SUMMARY OF UNIBUS SIGNALS

Name	Mnemonic	Source	Destination	Timing	Function
Data Transfer Signals (For transfer of data to or from master)					
Address	A<17:00>	Master	All	MSYN	Selects slave device
Data	D<15:00>	Master	Slave	MSYN (DATO, DATOB)	
		Slave	Master	SSYN (DATI, DATIP)	
Control	C<1:0>	Master	Slave	MSYN	Selects transfer operation
Master Sync	MSYN	Master	Slave	Beginning of transfer	Initiates operation and gates A, C and D signals
Slave Sync	SSYN	Slave	Master	Data accepted (DATO, DATOB) Data Available (DATI, DATIP)	Response to MSYN
Parity Bit Low	PA	Master	Slave	Same as Data	PA PB 0 0 no error 0 1 parity error 1 0 (reserved) 1 1 (reserved)
Parity Bit High	PB	Master	Slave	Same as Data	
Priority Transfer Signals (For transfer of bus control to a priority-selected master)					
Non-processor Request	NPR	Any	Processor	Asynchronous	Highest priority bus request
Bus Request	BR<7:4>	Any	Processor	Asynchronous	Requests bus mastership

5.8 SUMMARY OF UNIBUS SIGNALS (Cont.)

Name	Mnemonic	Source	Destination	Timing	Function
Non-Processor Grant	NPG	Processor	Next master	Asynchronous	Transfers bus control
Bus Grant	BG<7:4>	Processor	Next master	After instruction	Transfers bus control
Selection Acknowledge	SACK	Next Master	Processor	Response to NPG or BG	Acknowledges grant & inhibits further grants
Bus Busy	BBSY	Master	All	Asserted by bus master	Asserts bus mastership
Interrupt	INTR	Master	Processor	After asserting BBSY (not after NPR), device may perform several transfers before asserting INTR.	Transfers bus control to handling routine in processor
Miscellaneous Signals					
Initialize	INIT	Processor	All	Asynchronous	Clear and reset signal
AC low	AC LO	Power	All	Asynchronous	Indicates impending power failure
DC low	DC LO	Power	All	Asynchronous	Indicates dc voltages out of tolerance, and system operation must be suspended.

NOTE
Signals on the UNIBUS are asserted when **low** (except for the 5 unidirectional bus grant lines).



NOTE: 5 msec is needed between the AC LO and DC LO signals on Power Down to guarantee the program 2 msec of running time.

Figure 5-15 Power Fail Sequence

5.9 UNIBUS

5.9.1 Timing

Although all bits of an information signal are transmitted simultaneously, differences in bus path lengths and speeds of individual gate responses may cause variations in transmission time and in the elapsed time before reception. To allow for slow signals to arrive, and to permit settling of levels which have encountered transmission noise, the strobing or gating of this data is delayed a nominal 75 ns. This delay is greater than the worst case signal skew encountered in practice.

A further delay may be necessary to allow an information signal within a device to qualify gates that accept a strobing signal. A 75-ns delay allows for this gating and must be provided by any device which acts as bus master for a data transfer. Thus, a slave is always guaranteed that address and data are valid at its interface (the device side of the

receivers) 75 ns in advance of the MSYN signal at the output of the MSYN receiver. If a slave requires more decoding time, it must provide its own delay for the MSYN signal, or trigger a delayed strobe from the MSYN signal.

To simplify slave device design in a DATI or DATIP sequence, the slave may place the data on the D lines coincident with the assertion of SSYN. The deskewing (75 ns) and decoding delay is the master's responsibility. In the INTR sequence, the interrupting device may place the vector address on the D lines coincident with the INTR signal. The processor allows for the 75-ns skew.

5.9.2 Time-Out Protection

A precaution must be taken when designing peripheral devices that gain control of the bus for the purpose of transferring data to another element on the UNIBUS. Normally, such a device contains a bus address register, which is loaded by the program as one of the initialization steps. This address must then be incremented by the device upon completion of each data transfer. If the program loads an erroneous address or if the register increments beyond the available core memory in the existing system, no SSYN response is generated for the data transfer. To prevent this problem from hanging up the system, it is recommended that a 10- to 25-μs integrating one-shot be triggered each time the master device asserts MSYN. If this one-shot times out before SSYN is received, the master should stop the transfer by clearing MSYN, BBSY, and any other signals it has asserted. The master should then set an error flag in its status register.

5.9.3 Priority Chaining

The PDP-11 uses electrical chaining of devices to assign minor priority levels. These levels separate devices of the same major priority level to provide a full array of priority servicing. Figure 5-16 illustrates the mode of operation and advantages of this system. Six devices are shown in order of their electrical distance from the processor. Three devices are at major priority level 4: device A, device C, and device D. The remaining three are at major priority level 5.

If the processor is at priority level 5 or above, no bus requests are granted from any of these devices. At a processor priority of 4, only requests from devices B, E, or F are granted. Assume that the processor priority is 2 and also that during one instruction cycle, devices C, E, and F assert bus requests. At the end of the instruction, the processor conducts a PTR operation. Since BR 5 is asserted, the processor does not respond to BR 4 (device C). When BG 5 is asserted, the signal first goes to device B. The signal is passed on, since device B was not asserting BR and does not block the pulse. Next, the signal goes to device E, which blocks the pulse, drops BR 5, and takes control of the bus. Device F still has BR 5 asserted, however, and device C has BR 4 asserted. These requests remain on the bus until granted or actively cleared by the processor. If device E does an INTR operation, device F gains control of the bus after the first instruction of the handling routine has been executed, unless the INTR operation raises the processor priority.

Changing the processor priority is accomplished easily since the trap

sequence following the INTR operation provides a new PS word, which includes a new processor priority. If the priority is set to 5, the processor ignores the current bus request but grants requests from other devices with higher major priority levels (if there are any).

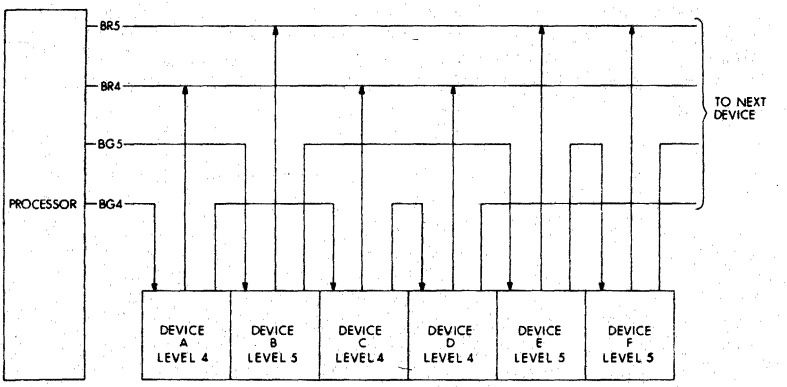


Figure 5-16 Priority Chaining Example

At the conclusion of the interrupt handling routine, the original processor priority is restored and normal processing is resumed. After one instruction, device F gains control of the bus. When normal processing resumes again, device C, which is still waiting for bus service, gains control in a similar manner.

Higher priorities are assigned to devices that require faster service to avoid destruction or loss of data. Slower devices, which can afford to wait, operate with low priorities. Therefore, service can be provided to all devices in an equitable manner, with no lost data and maximum speed and bus efficiency.

5.9.4 Address Mapping

A PDP-Address Map is shown in Appendix A. Observe that, in the following discussion, all addresses are numbered in octal. The letter K, which is normally used to devote 1000 (decimal), is used in this discussion to denote 1024 (decimal).

The UNIBUS addresses 2^{18} locations ($262{,}144_{10}$ or 256K), and each location contains eight bits. On the basic PDP-11 systems only 16 bits of address information are under program control. This limits the processor to an address map of 64K locations. Since the word length and bus width are two bytes, most bus operations access two locations at once; the address supplied on the bus is that of the even-numbered location, and the next higher odd location is selected as well. Byte operations can explicitly address any byte. For example, a DATI to location 400 transfers the information in locations 400 and 401, while a DATOB to location 400 loads only location 400. In all cases, a full-word operation cannot address an odd-numbered location.

The address map (Appendix A) contains full, 18-bit wide bus addresses. Without the Memory Management option, hardware in the processor forces A(17:16) to ones if A(15:13) are all ones when the processor is master; thus, the last 8K byte locations are relocated to be the highest locations accessible by the bus. All device addresses and internal processor locations are assigned in these 8K locations.

Interrupt and Trap Vector Locations
The first 1000 (octal) locations in the address map are reserved for trap and interrupt vectors. The stack pointer overflow feature of the processor warns the user that the data in these locations may be subject to destruction if the system stack expands downward into this area. Locations 0 through 37 are used for trap vectors for internal processor use, locations 40 through 57 are reserved for use as system software communications words, and the remaining locations are used for device interrupt vectors. There is no limit to interrupt vectors above 400 except that they are not protected from stack overflow, except with the Programmable Stack Limit option.

To prevent customer-designed interfaces from interfering with standard DEC products, the vector addresses (170, 174, 270, and 274) are reserved for customer interfaces.

Each vector requires four locations (two words), and the vector addresses are constrained to even-word boundaries; that is, each vector must end in 4 or 0. (This is implemented by providing vector addresses which do not specify bits 0 or 1. Since the low bits are always 0, address bit 2 specifies either 0 or 4.)

Memory Locations
Memory locations, either read/write or ROM, begin at 0 and proceed to 757777. The highest numbered 8K-block in the map is used by device registers and by internal processor register addresses.

Device Register Locations
Each device has one or more device registers. Device register addresses are always even (A00 is 0), although byte operations may address either half of a register.

The top 4K word locations are allocated for device register assignment. The top 2K words (770000-777777) is reserved by Digital for processor addresses and standard peripheral devices. The 1K word addresses (764000-767777) are reserved for customer allocation. It is recommended that customer-built interfaces be given addresses in this area.

5.9.5 Devices Registers
The actual transfer of data between a device and the UNIBUS takes place through one or more registers in the device. These registers may be either flip-flop storage registers or dynamic signals which are simply gated to the bus during a transfer. In addition, it is not necessary for the exact nature of the register bits to be the same. Some bits may be used for read/write (transfered on both DATI and DATO transactions); some may be write only (participate only in DATO transactions, and appear as 0s for DATI's); and some may be read only (participate only in DATI's, unaffected by DATO's). Exercise caution when assigning bit usage. For

example, a BIS (Bit Set) instruction to a word containing a write-only bit does not set the bit, but clears it. This is because a BIS performs a DATIP, DATO sequence and, if the bit reads as a 0, it is rewritten as a 0. Examples of all three types are usually found in control and status registers. A typical example of a read write bit is an interrupt enable bit; an example of the write bit is a go command bit; an example of a read bit is an indicator of an error condition requiring operator intervention.

To standardize register format types, Digital has adopted some preferred bit assignments which are shown in Figure 5-17. The preferred order of register address assignments is given in Table 5-6. These preferences are included for reference only and should not be construed as mandatory requirements for interfacing to the UNIBUS. The exact nature of register assignments varies with each device.

FUNCTION: Device Function (read, write, punch, search, etc.) Single function devices should use bit 0 because INC CSR (an operate instruction) performs the command with less program storage and is also faster than a conventional MOV.

EXTENDED MEM: Used to specify A(17:16) when doing device controlled data transfers to locations not in the first 64K block of addresses.

INTR ENB: Interrupt Enable. Inhibits Interrupt on done or error if not set.

READY or DONE: Bit set by device when internal processing is completed and the device is ready to participate in a transfer. Can be checked by the instruction sequence LOOP: TSTB CSR, BPL LOOP.

UNIT SELECT: Used to select multiple devices connected to a single controller (such as DECtape units with operator set unit numbers).

BUSY: Indicates that the device is doing internal processing and cannot participate in a new operation. Need not be used in many devices, READY may be adequate.

ERROR: Indicates the source or cause of an Error Interrupt. Bit 15 is used for single-error conditions or may be the logical OR of several error condition to allow the TST instruction to check error status.

Table 5-6 Preferred Order of Device Register Assignments

ADDRESS (OCTAL)		
N	CSR	CONTROL STATUS REGISTER
N + 2	DBR	DATA BUFFER REGISTER
N + 4	MAR	MEMORY ADDRESS REGISTER
N + 6	WCR	WORD COUNT REGISTER
N + 10	DAR	DEVICE ADDRESS REGISTER

CSR—Device function, status interrupt control.
DBR—Data register for information transfer.
MAR—Memory location for block transfer. Incremented by device logic each word transfer.
WCR—Set by program to control length of block transfer.
DAR—Track or block number for mass storage devices.

When several registers are used for the same function, they should be assigned contiguous addresses, and be followed by registers of other functions in the same order as for single registers of each function.

CSR1
CSR2
DBR1
DBR2
DBR3
MAR
WCR
DAR

All register types are optional; only implemented registers should be assigned addresses.

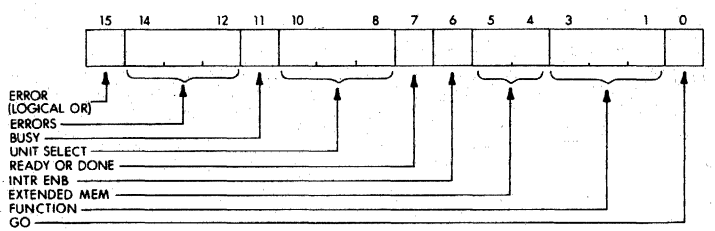


Figure 5-17 Preferred CSR Bit Assignments

5.10 COMPARISON BETWEEN NPR & BR OPERATION

	NPR	BR
Operation	data transfer (Direct Memory Access)	program interrupt
When granted	during an instruction	at end of an instruction
Condition for grant	always	higher priority than CPU
Signals		
Request	NPR	BR7, BR6, BR5, BR4
Grant	NPG	BG7, BG6, BG5, BG4
Select Acknowledge	SACK	SACK
Bus Busy	BBSY	BBSY
Typical Registers used		
Command & Status (CSR)	X	X
Data Buffer (DBR)	X	X
Word Count (WCR)	X	
Data Address (DAR)	X	
Memory Address (MAR)	X	
Usage	critical data	plenty of time
Trade off	inexpensive in time, expensive in hardware, hardware does the work	inexpensive in hardware, expensive in time, software does the work
If wrong choice	higher cost	lose data or bad data
Typical devices	disk tape A/D (high speed) communications MX scopes	paper tape terminal A/D (low speed) communications single line

CHAPTER 6

UNIBUS INTERFACING

6.1 GENERAL

This chapter discusses the specific circuits and modules used for interfacing devices to the UNIBUS.

The UNIBUS, a high-speed data transmission facility, imposes certain restrictions when attaching other devices to it. The actual bus is a matched and terminated transmission line which must be received and driven with devices designed for that specific application. The following paragraphs describe bus transmission, bus signal levels, bus length, and bus receiver and transmitter circuits.

6.1.1 UNIBUS Transmission

The actual bus medium consists of several types of cable. The standard cabling is composed of short jumper modules that interconnect the system units within a mounting assembly. The M920 Module serves as the jumper module. Critical ground signals are also carried on this module. Cables used between mounting assemblies consist of a flat ribbon cable assembly with alternating signals and grounds. The characteristics necessary for proper UNIBUS transmission are:

Characteristic Impedance:	120Ω ± 18Ω
Resistance:	0.135Ω/ft, maximum

Either twisted pair or coaxial cable laid for minimum crosstalk is recommended for long cable lengths and for applications requiring extreme physical durability of the cable.

The UNIBUS is terminated at each end by a resistive divider for each signal except the grant signals (see Figure 6-1). The grant signals are terminated with a single resistor. Two M930 Terminator Modules are included in every system to provide these functions.

6.1.2 UNIBUS Signal Levels

For most UNIBUS signals:

logic 1 = 0 volts (LOW)
logic 0 = + 3.4 volts (HIGH)

Note that the polarity is opposite to that normally used with TTL integrated circuits.

The rest state for all UNIBUS signal lines, except the grant lines BG < 7:4 > and NPG, is a logic 0 of + 3.4V. The asserted state (logic 1) is between ground and + 0.8V, which is the saturation voltage of the

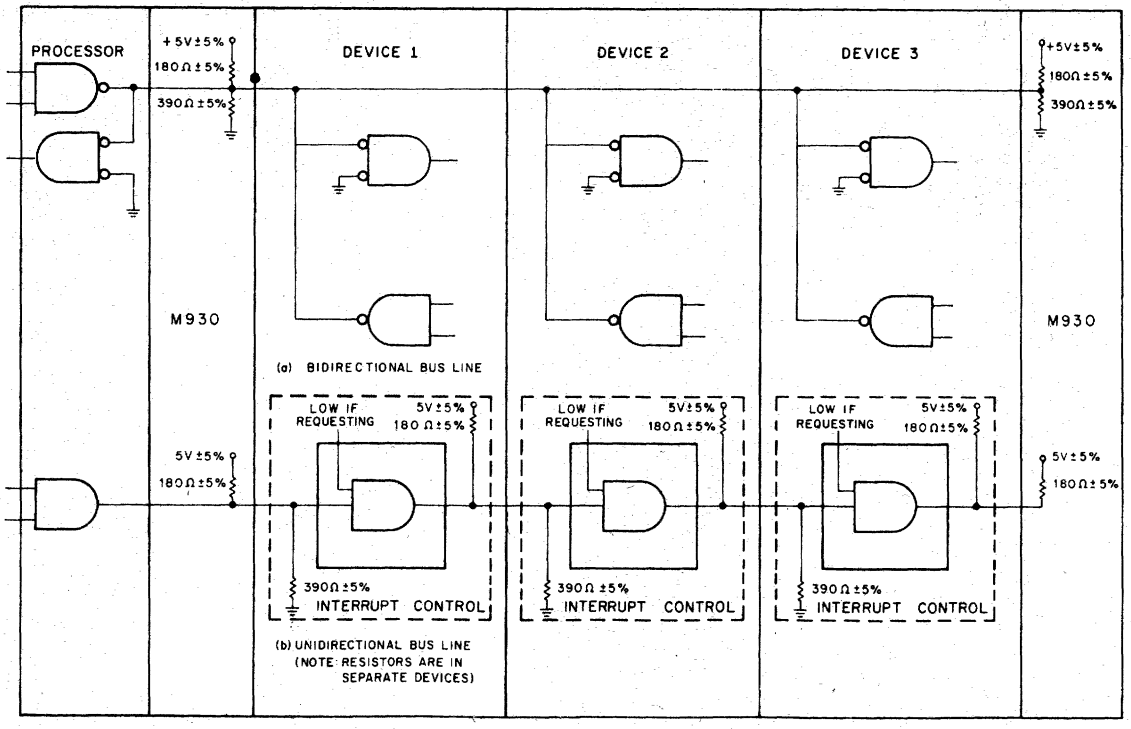


Figure 6-1 Bus Terminations for Bidirectional (a), and Unidirectional (b) Bus Lines

transistor driving the bus. The rest state for the grant signals is ground (logic 0) and the asserted state (logic 1) is + 3.4V. To guarantee operation under worst case conditions, receivers should have a switching threshold of approximately + 1.5V.

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic and is separated by a space. This letter indicates the asserted (logic 1) state of the signal to be either high (approximately + 3V) or low (ground). Thus, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

With flip-flops, a 1 or 0 in parentheses is often used following the signal name to indicate the assertion state, see Figure 6-2.

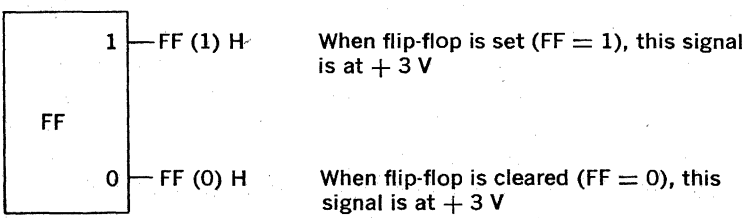


Figure 6-2 Flip-flop signals

Note that:

FF (1) H = FF (0) L

and

When FF is a 0, this signal is at 0 V.

FF (0) H = FF (1) L

All signals which are not UNIBUS signals are characterized in terms of standard transistor-transistor logic (TTL) loads. These devices, which are similar to the 7400 Series, have a low state input load of — 1.6 mA and a high state leakage current of 40 μA. Outputs are characterized by the number of inputs they can drive (called fanout).

A standard TTL gate can drive 10 unit loads.

6.1.3 Bus Receiver and Transmitter Circuits

The equivalent circuits of the standard UNIBUS receivers and transmitters are shown in Figure 6-3. Any device which meets these requirements is acceptable. To perform these functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 6-1. Typical transmitter and receiver circuits are shown in Figure 6-4.

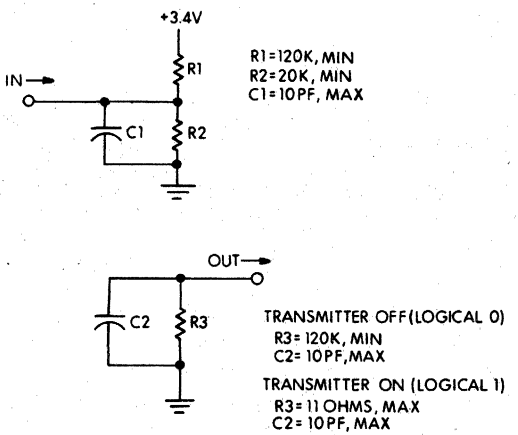


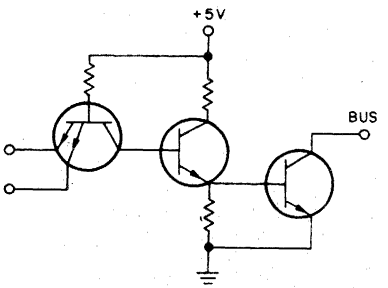
Figure 6-3 Transmitter and Receiver Equivalent Circuits

Table 6-1 Unibus Receiver and Transmitter Characteristics

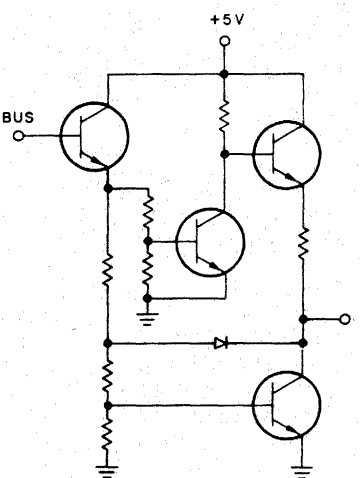
	Characteristic		Specifications	Notes
Receiver (DEC 380)	Input high threshold	VIH	2.5V min.	1
	Input low threshold	VIL	1.4V max.	1
	Input current @ 2.5V	IIH	160 μA max.	1, 3
	Input current @ 0V	IIL	± 25 μA max.	1, 3
	Output high voltage	VOH	3.5V min.	2
	Output high current	IOH	— 2 mA	2, 3
	Output low voltage	VOL	0.6V max.	2
	Output low current	IOL	— 12.5 mA	2, 3
	Propagation delay to high state	TPDH	10 ns min. 45 ns max.	4, 5
	Propagation delay to low state	TPDL	10 ns min. 35 ns max.	4, 5
Transmitter (DEC 8881)	Input high voltage	VIH	2.0V min.	6
	Input low voltage	VIL	0.8V max.	6
	Input high current	IIH	60 μA max.	6
	Input low current	IIL	— 2.0 mA max.	6
	Output low voltage @ 70 mA sink	VOL	0.8V max.	1
	Output high leakage current @ 3.5V	IOH	25 μA max.	1, 3
	Propagation delay to low state	TPDL	25 ns max.	5, 7
	Propagation delay to high state	TPDH	35 ns max.	5, 8

NOTES:

1. This is a critical parameter for use on the UNIBUS. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving seven unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 375Ω to + 5V and 1.6KΩ in parallel with 15 pf to ground.
5. Times are measured from 1.5V level on input to 1.5V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.
7. Conditions of 100Ω to + 5V, 15 pf to ground on output.
8. Conditions of 1KΩ to ground on output.



TYPICAL UNIBUS DRIVER



TYPICAL UNIBUS RECEIVER

Figure 6-4 Transmitter and Receiver Typical Circuits

Transmitter
If both inputs to a UNIBUS Transmitter are logic 1 (HIGH), there will be a logic 1 (LOW), on the UNIBUS. Refer to Figure 6-5. Logically, the Transmitter is an AND gate; there is voltage inversion, but no logic inversion.

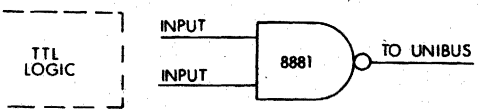


Figure 6-5 UNIBUS Transmitter

The outputs of 2 Transmitters can be tied together to perform the "Wired-OR" operation. Refer to Figure 6-6.

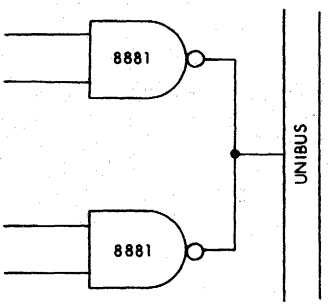


Figure 6-6 Wired OR Configuration

If any 8881 Transmitter has both its inputs at logic 1, there is a logic 1 on the UNIBUS. The logical operation is AND-OR.

Receiver
If the UNIBUS line is a logic 1 (LOW), the output will also be a logic 1 (HIGH). Refer to Figure 6-7. Logically, the Receiver has no effect on the signal; but there is voltage inversion, thereby cancelling the effect of the first voltage inversion by the Transmitter.

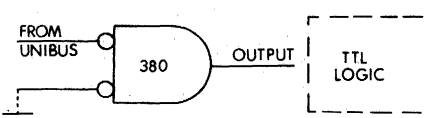


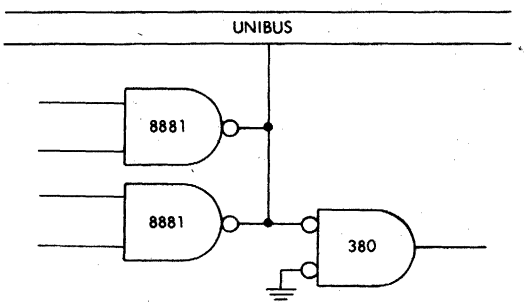
Figure 6-7 UNIBUS Receiver

If the inputs were connected to separate UNIBUS signals, the Receiver would logically be a 2-input OR gate.

6.1.4 UNIBUS Length and Loading
Since the UNIBUS is a transmission line, and the transfers are asyn-

chronous and interlocked, the electrical delay imposed by length is not a factor.

With ribbon cable the maximum length is 50 ft. minus the combined length of all stubs or taps, which are those wires from the actual bus to the receivers and transmitters. For proper operation, the length of these stubs must be minimized. If necessary, the UNIBUS signals should have receivers and transmitters in one place (near the UNIBUS cable) to act as a buffer between the UNIBUS and the signal lines carrying UNIBUS signals within the equipment. This maximum length is obtainable only if the individual tap lengths are less than 18 inches and if the loading is not more than one standard bus load. One bus load is defined as 2 transmitters and 1 receiver, see Figure 6.8. If loads are concentrated at one end of the UNIBUS and a single load is at a distant point, the maximum length could change, provided that the crosstalk of the employed cable is low enough.



1 bus load = 2 transmitters + 1 receiver

Figure 6-8 1 Bus Load

The UNIBUS is limited to a maximum of 20 bus loads. This limit is imposed because of the loading of receivers and leakage of drivers at the high state. This limit is set to maintain a sufficient noise margin. For more than 20 bus loads, a UNIBUS repeater option (DB11-A) is used.

6.2 UNIBUS INTERFACE MODULES

This section describes modules used for UNIBUS interfacing.

Module	Name	Description
BC11A	UNIBUS Cable	120-conductor ribbon cable, 56 signals plus 64 grounds, alternating.
M105	Address Selector	Address decoding for 4 devices.
M783	Bus Transmitter	12 drivers, mixed logic.
M784	Bus Receiver	16 receivers; single input, single output.

M785	Bus Transceiver	8 drivers plus 8 receivers.
M795	Word Count & Bus Address	2 16-bit counters.
M796	Bus Master Control	Complex control logic.
M920	Bus Jumper	Connects SU to SU; 56 signals plus 14 grounds.
M930	Bus Terminator	180 ohms to + 5V and 390 ohms to ground.
M7820	Interrupt Control	2 Master Control circuits.
M7821	Interrupt Control	NPR plus BR circuits.

6.2.1 BC11A, UNIBUS Cable

The BC11A (see Figure 6-9) is a 120-conductor ribbon cable used to connect System Units in different mounting drawers or assemblies.

The 120 signals include all the 56 UNIBUS lines plus 64 grounds. Signals and grounds alternate to minimize crosstalk. Cable types and lengths are listed below:

Type	Length (ft.)
BC11A-2	2.0
BC11A-5	5.0
BC11A-8F	8.5
BC11A-10	10.0
BC11A-15	15.0
BC11A-25	25.0

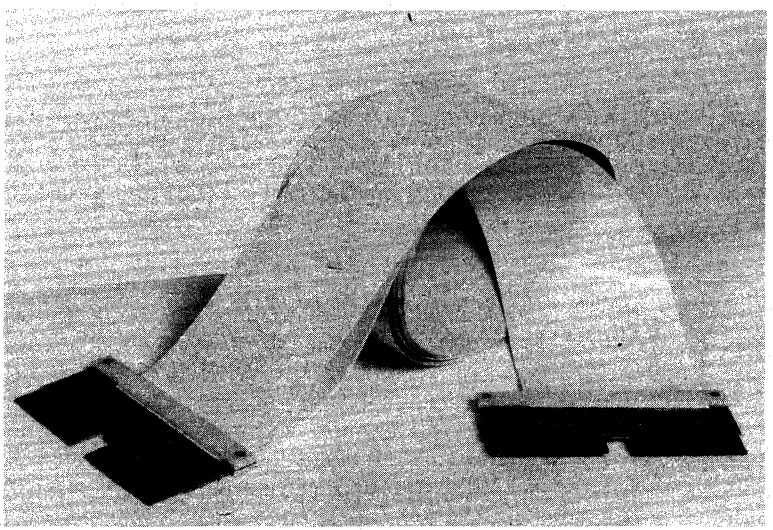


Figure 6-9 UNIBUS Cable BC11A

6.2.2 M105 Address Selector Module

The M105 Address Selector Module provides gating signals for up to 4 full 16-bit device registers. A block diagram of this module is shown in Figure 6-10. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the M105 is used in a peripheral device, an OUT transfer is a transfer of data out of the master (such as the processor) and into the device. Likewise, an IN transfer is the operation of the peripheral furnishing data to the processor.

Inputs: The M105 Module input signals consist of 18 address lines, A <17:00>; 2 bus control lines, C <1:0>; and a master synchronization MSYN line. The address selector decodes the 18-bit address on lines A <17:00> as described below. This address format, used for selecting a device register, is shown in Figure 6-11. Note that all inputs are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers.

c. Decoding of lines A <12:03> is determined by jumpers on the module. When a given line contains a jumper, the address selector searches for a zero on that line. If there is no jumper, the address selector searches for a one.

d. Address lines A <17:13> must be all ones. This specifies an address within the top 8K byte address bounds for device registers.

Slave Sync (SSYN): When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the M105. In this case, the SSYN must be generated by another source. When SSYN INH is not grounded, SSYN is returned to the master 100 ns after register select becomes true. This time may be extended to a maximum of 400 ns by adding an external capacitor between SSYN INH and ground. SSYN INH can also be driven with an open collector gate.

Outputs: The M105 Select Signals permit selection of four 16-bit registers and provide three signals used for gating information to and out of the master device. The M105 may be used instead to select up to eight 8-bit registers, or any appropriate combination of byte and word registers.

The input signals select the M105 control output line states as shown in Tables 6-2 and 6-3.

Table 6-2 M105 Select Lines

Input Lines A <02:01>	Select Lines True (+ 3V)
00	0
01	2
10	4
11	6

NOTE

1. Lines A <17:13> must be all 1's (OV on UNIBUS).
2. Lines A <12:03> are selected by jumpers.

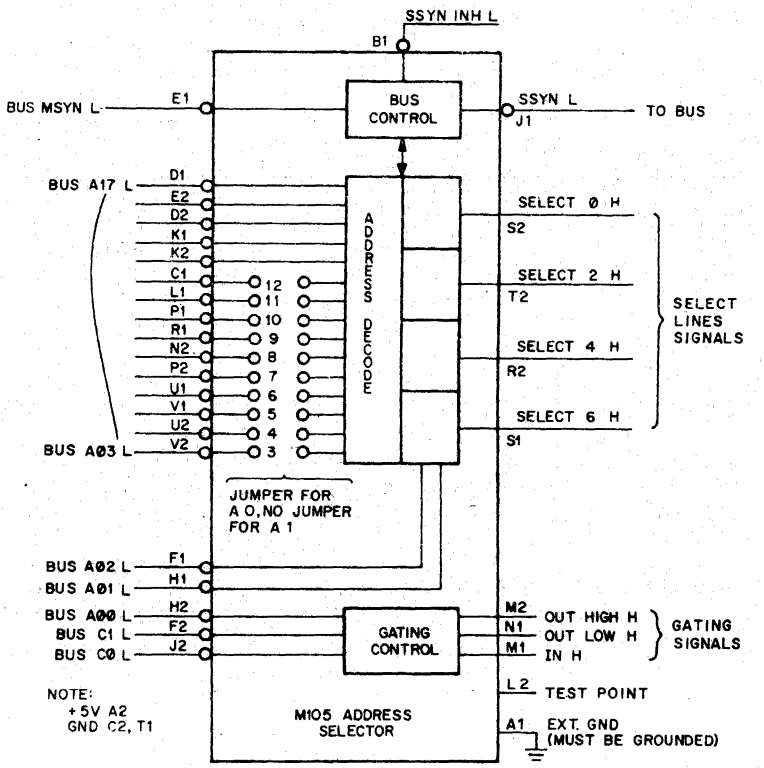


Figure 6-10 M105 Address Selector

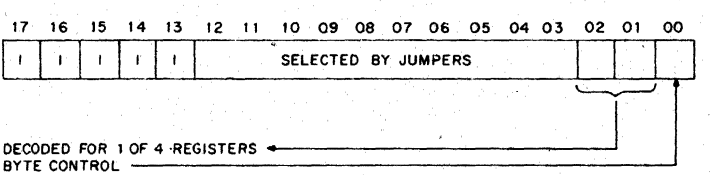


Figure 6-11 Device Register Select Address Format

Table 6-3 Gating Control Signals

Mode Control C <1:0>	Byte Control A00	Gating Control Signals True (+ 3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW, OUT HIGH	DATO
10	1	OUT LOW, OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE

Gating control signals may become true although select lines are not.

Specifications: The M105 output fanout is ten standard TTL loads for register select lines and eight standard TTL loads for gating control lines. The module is single-height. A circuit schematic for this module is shown in Figure 6-12. Note that pin A1 (EXT GND) must be grounded by the user.

When using the output signals of the M105 to load registers that comprise storage elements that are edge-triggered, insure that this edge is derived from the positive transition of the SELECT line, i.e. the leading edge of MSYN.

If the storage elements are loaded by a strobing pulse (not edge-triggered), then the entire pulse must be generated prior to the assertion of SSYN. The length of the loading pulse can be lengthened by adding capacitance to SSYN INHB on the M105.

6.2.3 M783 UNIBUS Transmitter Module

This transmitter module contains 12 drivers; 8 drivers have a common gate line, 4 have 2-input positive AND gating. Input loading is 1.25 standard TTL load. The module is single-height. A circuit schematic of the M783 Transmitter is shown in Figure 6-13.

6.2.4 M784 UNIBUS Receiver Module

This receiver module consists of 16 DEC 380 inverting circuits which receive bus signals and provide a buffered bus signal output. The output fanout is seven standard TTL unit loads. The receiver module is single-height. A circuit schematic of the M784 Receiver Module is shown in Figure 6-14.

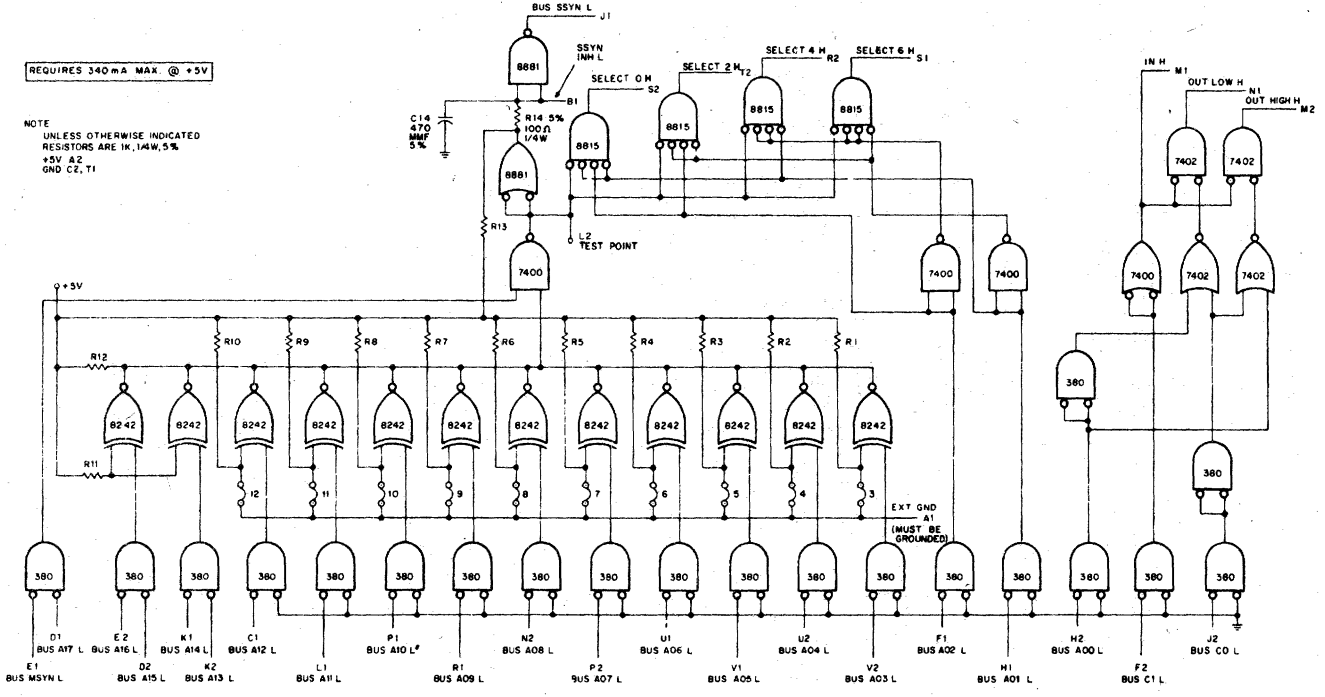


Figure 6-12 M105 Address Selector (schematic diagram)

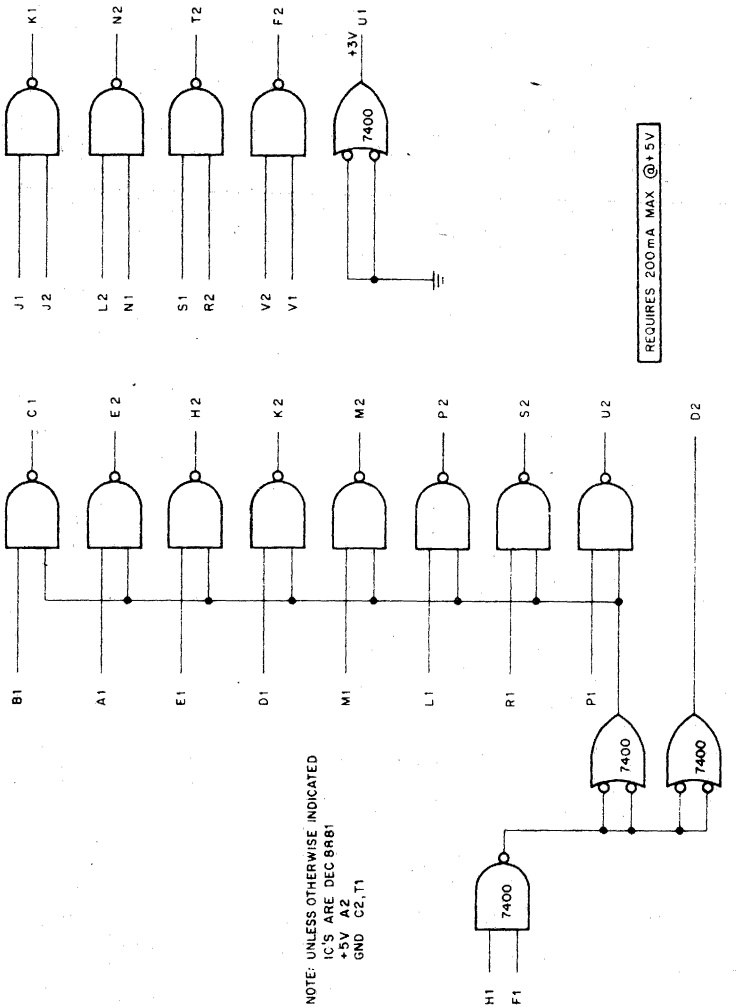


Figure 6-13 M783 UNIBUS Transmitter (schematic diagram)

6.2.5 M785 UNIBUS Transceiver Module

This module consists of eight pairs of DEC 8881 Drivers and DEC 380 Receivers which are used for bidirectional interfacing to the UNIBUS. The drivers and receivers have two common gate lines: one for receivers, one for drivers. The driver input loading is 1.25 standard unit load and the receiver fanout is 7 standard TTL unit loads. The module is single-height. A circuit schematic of the M785 Transceiver Module is shown in Figure 6-15.

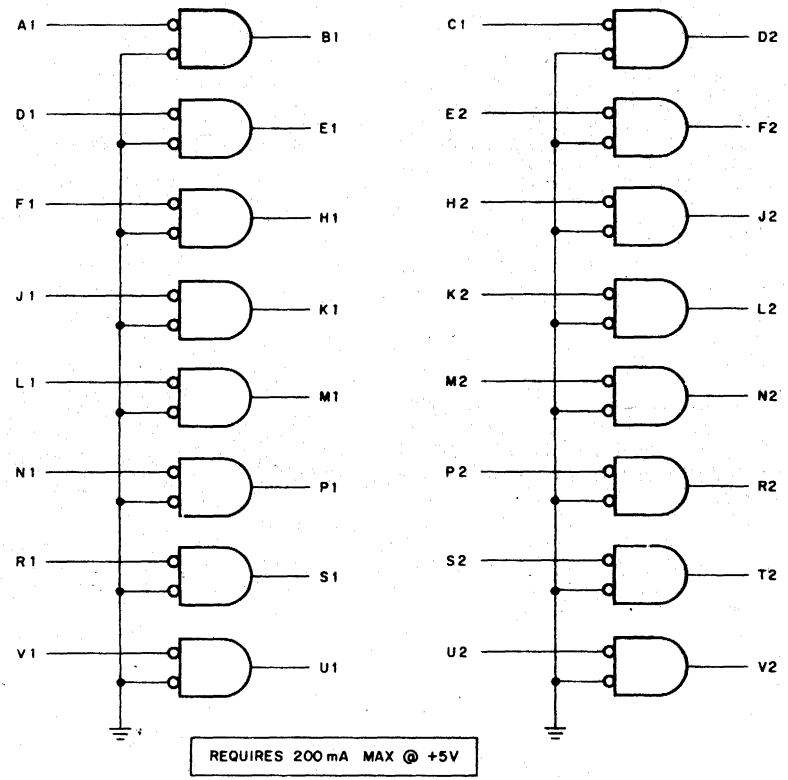


Figure 6-14 M784 UNIBUS Receiver (schematic diagram)

6.2.6 M795 Word Count and Bus Address Module

The M795 Word Count and Bus Address Module is used to interface direct memory access (DMA) devices to the UNIBUS. This module contains two 16-bit counters: one counter is used to count the number of data transfers that occur; the other counter is used to specify the bus address of the data to be transferred.

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is transfer count. Initially, a register is loaded with the 2's complement of the number of items to be transferred to or from memory. After each transfer is complete, the register is incremented. If the new value of the register is 0 (indicated by an overflow), further transfers are

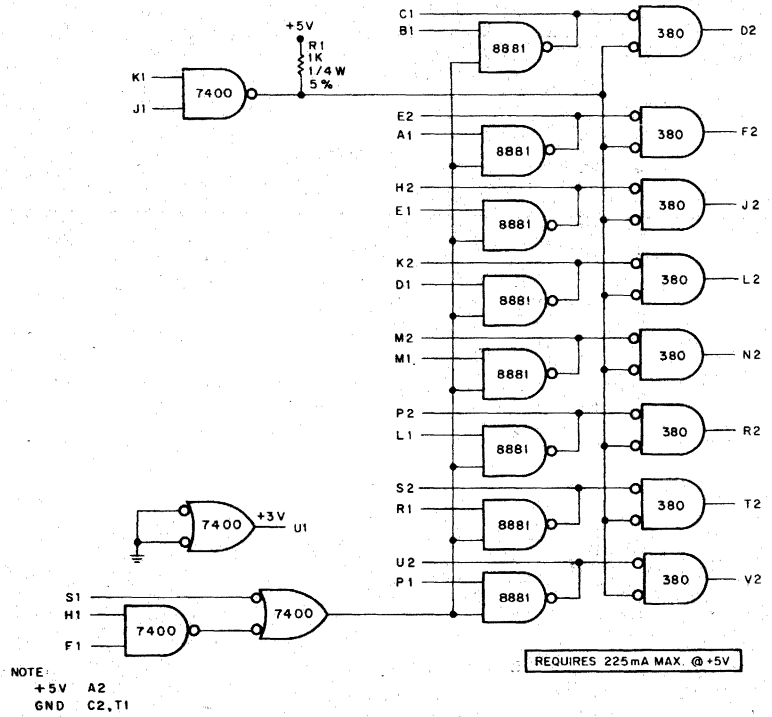


Figure 6-15 M785 UNIBUS Transceiver (schematic diagram)

inhibited and the block transfer is complete. Since information can be transferred in words (16 bits each) on the UNIBUS the name Word Count (WC) is usually assigned to this register. However, the UNIBUS is also capable of transferring 8-bit bytes of data at a time, and this register may be used equally as well as a Byte Count register.

The second parameter used in block transfers is the transfer address. Initially, a register is loaded with an address that specifies the memory location to, or from, which data is to be transferred. The register is incremented after each transfer; thus, the register continually "points" to sequential memory locations. Since memories and devices have addresses on the UNIBUS, this register is usually called the Bus Address (BA) register.

A simplified block diagram of the M795 module is shown in Figure 6-16. Both the word count (WC) and bus address (BA) registers consist of 16 flip-flops. These flip-flop registers can be loaded by placing data on the 16 data line inputs common to both registers and asserting the appropriate loading signal. There are four independent loading signals: WC high byte, WC low byte, BA high byte, and BA low byte. Each of the outputs of the 16 bits in the WC register are connected to a set of DEC 8881 UNI-

BUS drivers. The contents of the WC register can be gated to the data bus when the appropriate gate signal is activated. The BA register also has a set of UNIBUS drivers connected to each output so that the register contents can be gated to the data bus. Note that the driver outputs of both the WC and BA registers are wire ORed together. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the address bus.

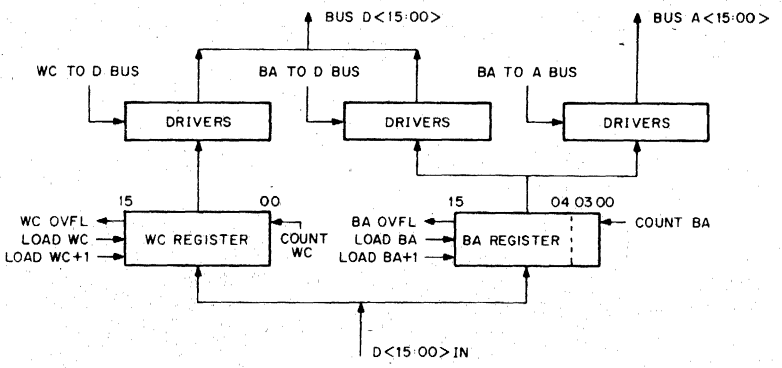


Figure 6-16 M795 Word Count and Bus Address (block diagram)

The storage element on the M795 is not an edge-triggered device; data must be established and held for the duration of the loading pulse.

The BA register can be incremented by either 1 or 2 as a function of a control input (+3V = 1; ground = +2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the count input of the register. The carry between bits 3 and 4 is broken and brought out to pins on the module. Normally, these pins are jumpered together externally to allow for a full 16-bit count. However, they can be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of its control input. The register increments on the trailing edge of a positive pulse applied to the count input of the register. An overflow pulse is also available. Both registers are reset to all 0s whenever the CLEAR signal is asserted.

Table 6-4 M795 Input Signals

Signal Name	Assertion Level	No. of Signals	Loading	Operation
D<15:00>IN	+3V	16	1.5	Data inputs to register.
LOAD WC LOAD WC + 1	OV	4	1	Loads data on input into selected byte of register.

LOAD BA LOAD BA + 1				Low pulse of 250 ns minimum duration
WC TO D BUS BA TO D BUS BA TO A BUS	OV	3	2	Gates selected register to bus.
CLEAR WC + BA	+3V	1	2	Clears all bits. High level of 1 μs minimum duration.
BA INC CONTROL WC INC CONTROL	+3V = incr by 1 OV = incr by 2	2	3	Controls amount of incrementation.
COUNT WC COUNT BA	+3V	2	4	Trailing edge of positive pulse increments register (100 ns minimum).
BA CARRY IN	OV	1	3	Carry into upper bits of BA.

Table 6-5 M795 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BA CARRY OUT	OV	1	10	Carry out of low four bits.
BA OVFL WC OVFL	OV	2	10	Register overflow; low level pulse.
BUS D<15:00>	OV	16	UNIBUS	Data lines.
BUS A<15:00>	OV	16	UNIBUS	Address lines.

6.2.7 M796 UNIBUS Master Control Module

The M796 UNIBUS Master Control Module provides extremely flexible control logic that is used to control data transfer operations on the UNIBUS when a device is functioning as bus master. In addition to controlling the four transfer operations (DATI, DATIP, DATO, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used for special control functions.

Devices in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed with minimum processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the bus is provided by the M7820 Interrupt Control Module. The M7820 module requests use of the bus (usually by means of an NPR request), receives the bus grant signal

from the processor, asserts selection acknowledge (SACK), waits until the current bus master releases control of the bus, and then asserts BUS BUSY, thereby gaining bus control.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs the data (either a word or byte) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage); a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the device must set BUS C<1:0> for the required type of data transfer, specify the address of the slave device participating in the transfer, assert the MSYN signal, and then wait for the SSYN response from the slave. Data must either be gated to D<15:00> on a DATO cycle or be received and strobed at the proper time on a DATI cycle. The M796 module performs these functions.

Figure 6-17 is a block diagram of the M796 UNIBUS Master control module. The BUS C1 and BUS C0 outputs can directly drive the UNIBUS and are asserted as a function of the control inputs. Table 6-6 lists the states of the control inputs for the four possible bus cycles.

Table 6-6 Control Line Input States for M796

CI	C0	Bus Cycle
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

The data transfer sequence is triggered by meeting the AND condition of two low levels (pins H1 & H2). Usually these two inputs are tied together and are connected to the MASTER signal produced by the M7820 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both BUS C1 and BUS C0 are asserted as determined by their respective control inputs. The ADRS TO BUS signal is also asserted and is used to gate the address of the slave onto BUS A<17:00>. If an output cycle is specified (C1 = 1), the DATA TO BUS signal is asserted and is used to gate the data to be transferred to the slave onto BUS D<15:00>. The BUS MSYN signal is asserted 200 ns after START becomes true. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN causes BUS MSYN to be negated immediately. After a 100-ns delay, BUS C1, BUS C0, ADRS TO BUS, and DATA TO BUS are negated. When these signals drop, an END CYCLE pulse appears and is usually used to release control of the bus.

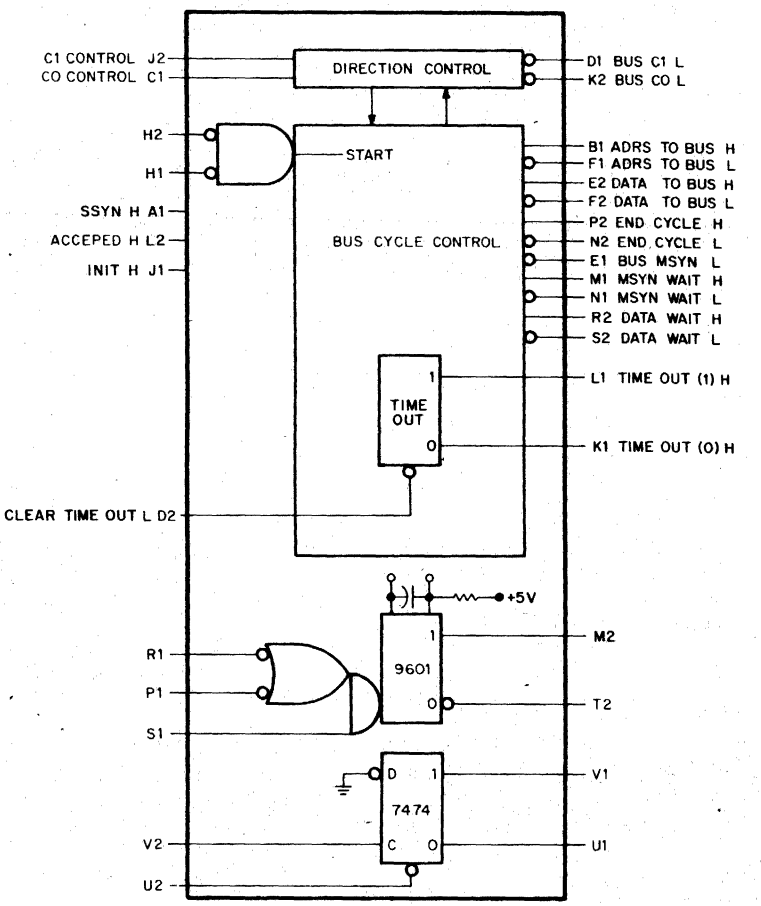


Figure 6-17 M796 UNIBUS Master Control (block diagram)

In a data input cycle (DATI), the assertion of SSYN produces a 200-ns pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necessary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED, causing BUS MSYN to be negated initially, followed by negation of ADRS TO BUS, BUS C1, and BUS CO 100 ns later.

A TIME-OUT flip-flop on the module is set if a SSYN response fails to occur within 20μs after BUS MSYN is asserted. When this flip-flop is set,

the bus cycle is not performed. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME-OUT signal.

The M796 module provides a special flip-flop that has the clock, reset, 1 side, and 0 side available. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true: $(\overline{R1} + \overline{P1}) \cdot S1$. The output pulse width of this one-shot is 150 ns but can be lengthened by adding capacitance across the pair of split lugs on the module.

Note that all times mentioned represent nominal values with a tolerance of $\pm 25\%$. The delays and pulses provided by the module are controlled by simple RC circuits. Therefore, if there are any special requirements, part substitutions can be made to alter these time constants.

Figure 6-18 illustrates a typical interconnection schematic for the M796 UNIBUS Master Control module used in conjunction with the M7820 Interrupt Control module. The read/write (R/W) flip-flop is part of the device interface logic and determines the direction of the data transfer (set for a DATO, clear for a DATI). The data transfer is initiated by pulsing SET REQUEST which sets REQUEST BUS. The REQUEST BUS signal generates an NPR request which, when granted, gives bus control to the device as indicated by the MASTER signal. The MASTER signal causes the internal START signal to be generated. This signal triggers the sequence of timing signals. Timing diagrams for DATO and DATI cycles are shown in Figures 6-19 and 6-20 respectively.

Note that in a DATI operation, the DATA WAIT signal is generated when BUS SSYN is received. The trailing edge of DATA WAIT fires the one-shot that produces the DATA STROBE signal. This signal gates the data present on the bus data lines into the device. The trailing edge of DATA STROBE produces a positive transition at the DATA ACCEPTED input that results in the clearing of BUS MSYN.

The input signals to the module are listed in Table 6-7 and the output signals are listed in Table 6-8.

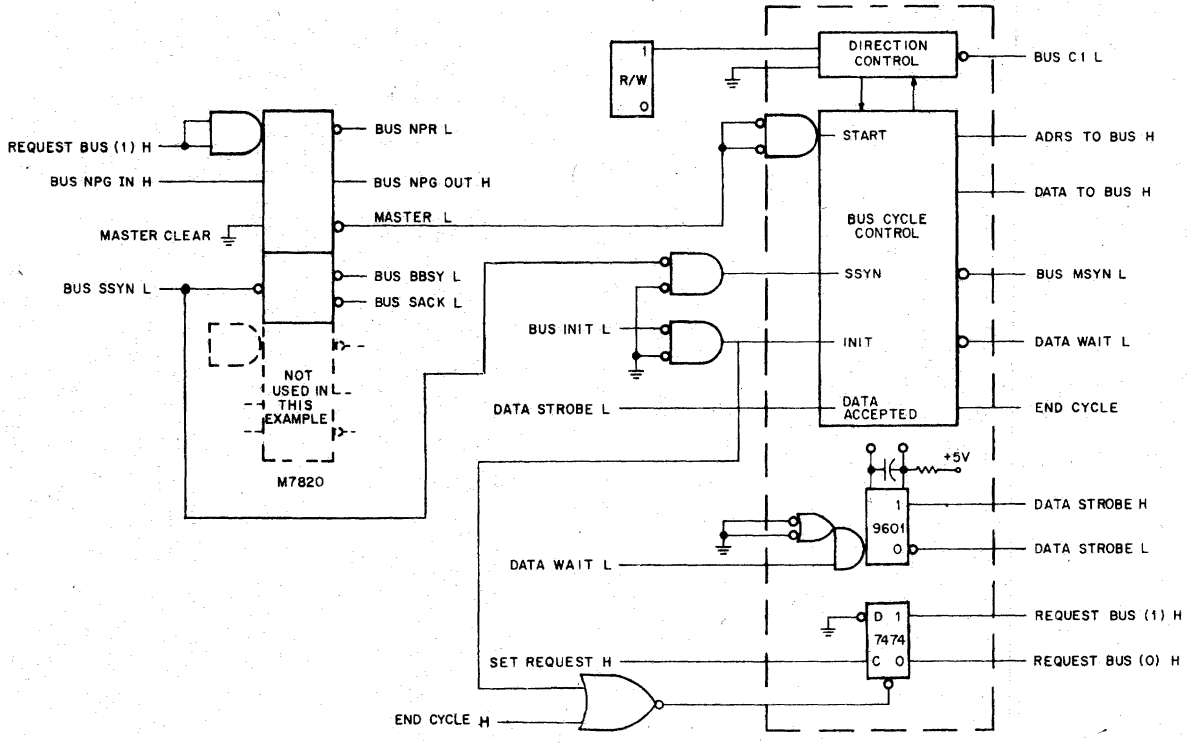


Figure 6-18 M796 UNIBUS Master Control (typical use)

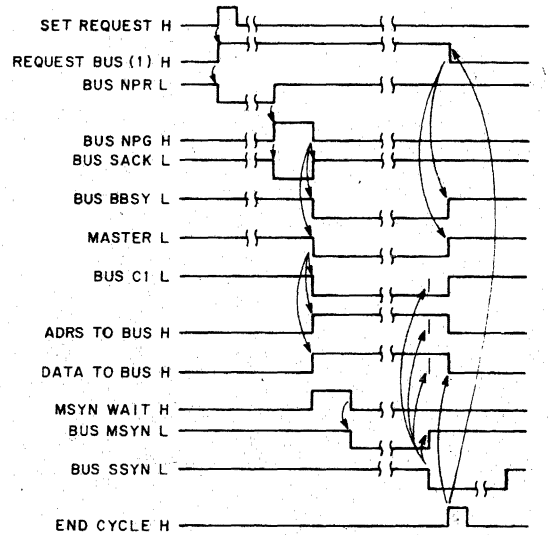


Figure 6-19 M796 Timing Diagram for DATO

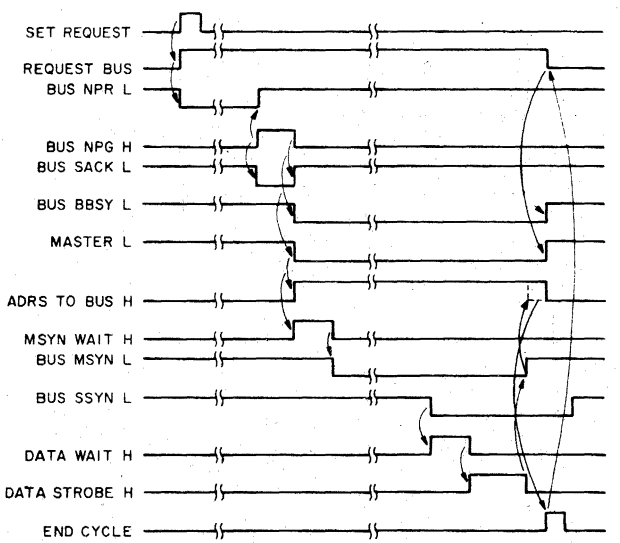


Figure 6-20 M796 Timing Diagram for DATI

Table 6-7 M796 Input Signals

Signal Name	Assertion Level	No. of Signals	Loading	Operation
C1 CONTROL		1	5	Controls Bus C1
C0 CONTROL		1	1	Controls BUS C0
PIN H2				
PIN H1	L	2	1	Produces START
SSYN	H	1	2	Negates MSYN on DATO
DATA ACCEPTED	H	1	2	Negates MSYN on DATI
INIT	H	1	1	Initializes control
CLEAR TIME OUT	L	1	2	Clears TIME-OUT Flip-Flop
PIN P1				
PIN R1	L	2	1	Negative edge triggers one-shot
PIN S1	H	1	2	Positive edge triggers one-shot
PIN V2	H	1	2	Clock input to flip-flop
PIN U2	L	1	2	Clears flip-flop

Table 6-8 M796 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BUS C<1:0>	L	2	UNIBUS	Drives UNIBUS control line
ADRS TO BUS	H	1	8	Gates BA to address bus
ADRS TO BUS	L	1	10	
DATA TO BUS	H	1	10	Gates data to bus on DATO or DATOB
DATA TO BUS	L	1	8	
END CYCLE	H	1	10	100 ns pulse indicating end of bus cycle
END CYCLE	L	1	8	
BUS MSYN	L	1	UNIBUS	Drives UNIBUS MSYN line
MSYN WAIT	H	1	10	200 ns pulse that delays assertion of MSYN
MSYN WAIT	L	1	8	
DATA WAIT	H	1	10	Allows for deskewing of DATA on DATI. Approximately 200 ns
DATA WAIT	L	1	8	
TIME OUT (1)	H	1	10	1 and 0 side of TIME-OUT Flip-Flop
TIME OUT (0)	H	1	10	

PIN M2	H	1	10	Output of one-shot
PIN T2	L	1	10	Output of one-shot
PIN V1	H	1	10	Outputs of flip-flop
PIN U1	L	1	10	

6.2.8 M920 UNIBUS Jumper Module

The M920 Module (see Figure 6-21) is a double module that connects the UNIBUS from one System Unit to the next. The printed circuit cards are on one-inch centers. A single M920 Module carries all 56 UNIBUS signals and 14 grounds.

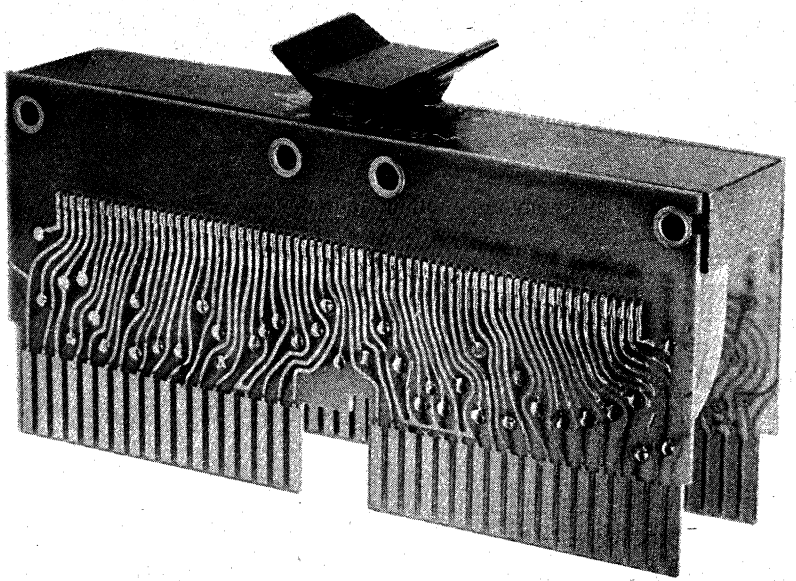


Figure 6-21 UNIBUS Jumper Module M920

6.2.9 M930 UNIBUS Terminator Module

The M930 UNIBUS Terminator Module is a short, double-size module that terminates all signal lines on the UNIBUS. This module requires 1.25 amps at 5V ±5%. All pins have a resistive divider termination of 180Ω to +5V and 390Ω to ground, except those listed below:

390Ω in parallel with 0.001 μf to +5V (for AC LO, DC LO)	180Ω to +5V (for grant lines)	Ground Pins		+5V Input Pins
BF1	AV1	AB2	BB2	AA2
BF2	AU1	AC2	BC2	
	BA1	AN1	BD1	BA2
	BB1	AP1	BE1	
	BE2	AR1	BT1	
		AS1	BV2	
		AT1		
		AV2		

6.2.10 M7820 Interrupt Control Module

The M7820 Interrupt Control Module provides the circuits and logic required to make bus requests and to gain control of the bus (become bus master). The module also includes circuits needed to generate an interrupt, if desired. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus contol. The interrupt control circuit can be used with either, or both, of the request channels and provides a unique vector address for each channel. Figure 6-22 is a block diagram of the M7820 Module, which is single-height.

The master control section (either channel A or B) is used to gain control of the bus. When the INTR and INTR ENB requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the BR line wired to the BR pin of the module. When the priority arbitration logic in the system recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the device has fulfilled all requirements to become bus master, the master control circuit asserts BBSY and then asserts a MASTER signal.

Once the device has gained bus control by means of a BR request, an interrupt can be generated. If an interrupt is desired, the module is interconnected as shown in Figure 6-23. This figure illustrates the use of the two channels to first generate requests for bus control and then initiate interrupts. The request from channel A is a slightly higher priority than the channel B request because the bus grant signal first enters A, then enters B.

The vector address is selected by jumpers on the M7820 Module. Since the vector is a two-word (four-byte) block, it is not necessary to determine the state of bits 0 and 1. The seven selectable lines determine vector address. The least significant line is controlled by the VECTOR BIT 2 input signal. If this input is asserted, then bus line D02 is asserted. Thus, the interrupt on channel A uses a vector at location 100 and channel B uses a vector at location 104.

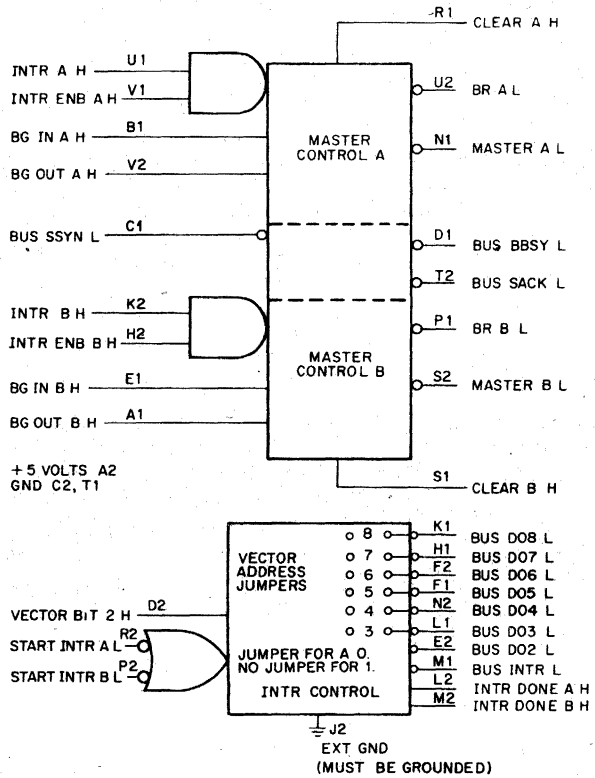


Figure 6-22 M7820 Interrupt Control (block diagram)

Figure 6-24 illustrates an M7820 Module used for bus control in a device that directly transfers data to memory and then causes an interrupt when the transfer is completed. Channel A is connected to the NPR and NPG lines and is used to gain bus control for direct to memory, or device-to-device, transfers. Channel B is used to gain bus control for an interrupt.

Each M7820 Module master control section contains two flip-flops that sequence through four states, thereby controlling the request for bus control. Figure 6-25 is a state diagram of this sequence and Figure 6-26 shows a circuit schematic of the M7820. The BG IN signal is allowed to pass through the module to BG OUT when the device is not issuing a request (state A), is master (state D), or has had the request honored (state E). To request bus use, the AND condition of INTR and INTR ENB must be satisfied. These levels must be true at least until the request is granted. Once bus control has been attained, it can be released by either asserting CLEAR or by negating either INTR or INTR ENB. The first

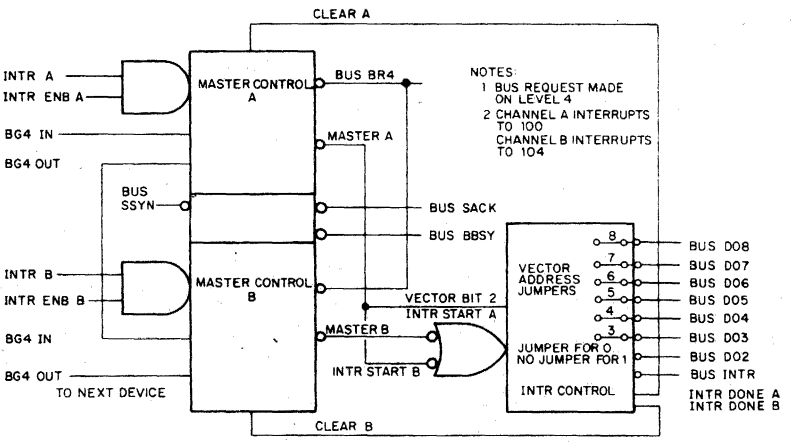


Figure 6-23 M7820 Interconnection for 2-Channel Interrupt

method leaves the master control in state E, thereby inhibiting further bus requests even if INTR and INTR ENB remain asserted. In order to make another bus request, INTR or INTR ENB must be dropped and then reasserted to cause the module to advance from state E through state A to state B where it asserts the request line. This prevents multiple interrupts when the master control is used to generate interrupts. The second method is used to release the bus after NPR use. Note that pin J2 (EXT GND) must be grounded by the user. A summary of all M7820 signals is listed in Table 6-9.

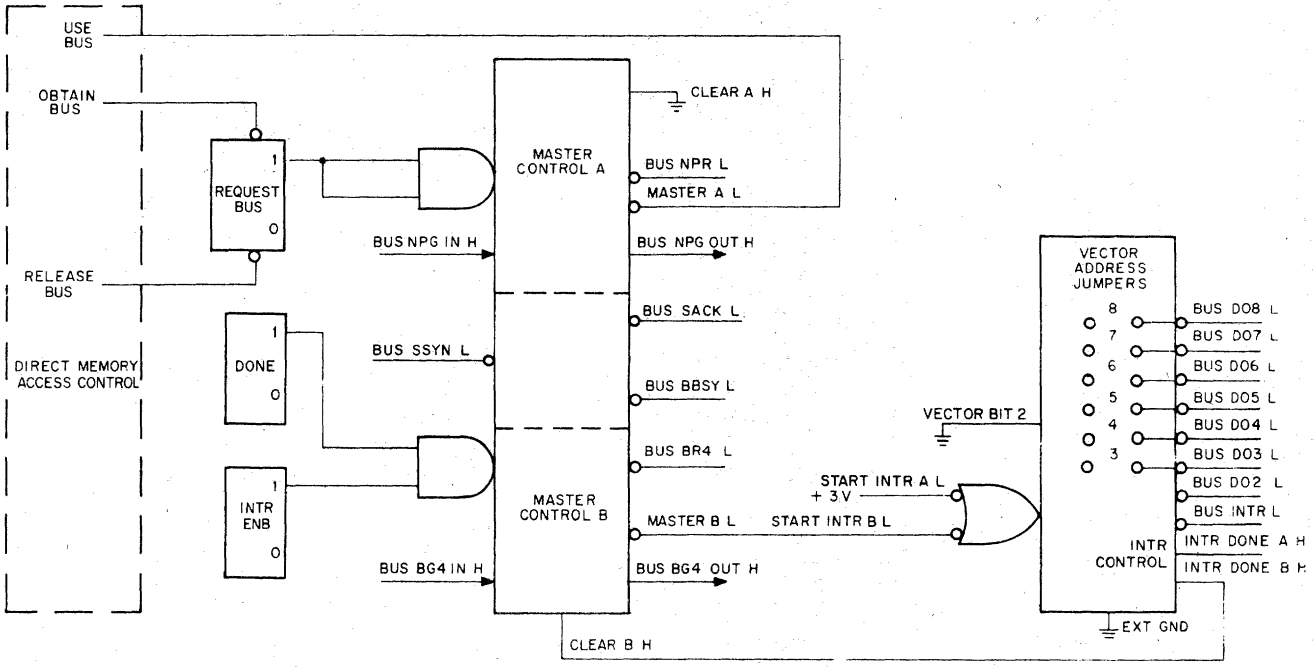
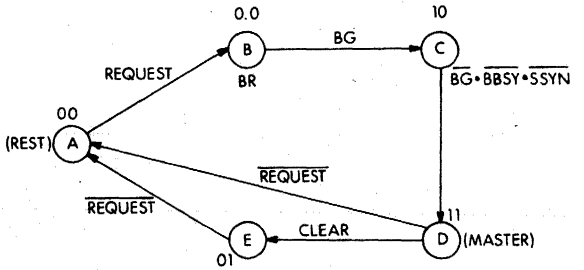


Figure 6-24 M7820 Interconnection for Direct Memory Access



The 2 binary numbers next to each circled state indicate the state of flip-flops FFA1 & FFA2 respectively, as shown in Figure 6-26.

Figure 6-25 State Diagram of M7820

Table 6-9 Summary of M7820 Signals

Signal	Assertion Level	Input Loading	Output Drive
INTR A, B	H	1 TTL (each)	
INTR ENB A, B	H	1 TTL	
CLEAR A, B	H	1 TTL	
MASTER A, B	L		10 TTL
START INTR A, B	L	2 TTL	
INTR DONE A, B	H		10 TTL
BG IN A, B	H	1 R*	
BG OUT A, B	H		2 D**
BR A, B	L		1 D
VECTOR BIT 2	H	1 TTL	
BUS SSYN	L	1 R	
BUS BBSY	L	1 R	2 D
BUS SACK	L		2 D
BUS INTR	L		1 D
BUS D <08:02>	L		D

* R = Standard UNIBUS receiver load.
** D = Standard UNIBUS transmitter (driver) output.

6.2.11 M7821 Interrupt Control Module

The M7821 Interrupt Control Module is a replacement for the M7820 that improves PDP-11 system performance. In almost all cases, it may be used directly in place of the M7820, without making any changes to hardware or software. A block diagram of the module is shown in Figure 6-27.

NOTE

The following description assumes the reader understands the function and operation of an M7820.

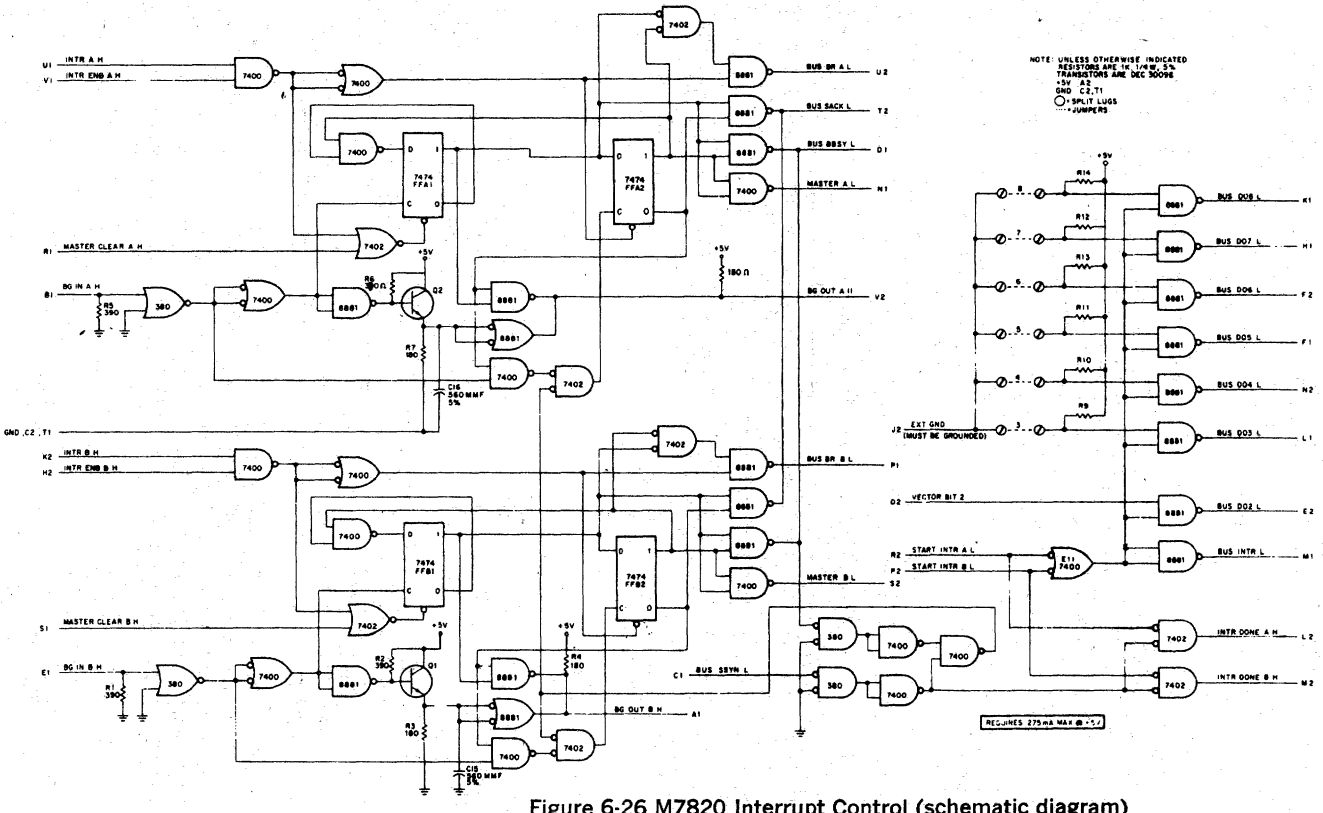


Figure 6-26 M7820 Interrupt Control (schematic diagram)

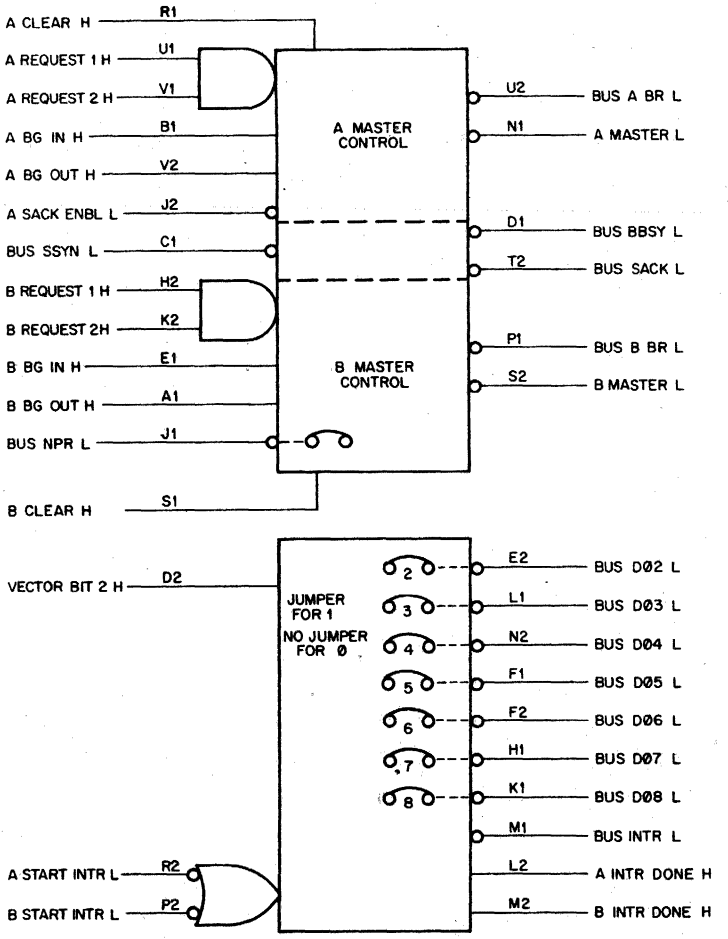


Figure 6-27 M7821 Interrupt Control Block Diagram

The M7821 does not have two identical Master Control halves. For devices which use one half of the module to become master with an NPR and one half for a BR, the top half (Request Bus pins U1 and V1) must be used for NPR and the bottom half (Request Bus pins H2 and K2) must be used for BR.

The NPR half of the module has the ability to prevent the un-assertion of BUS SACK for devices that do more than one data cycle each time they request the bus. This is done by holding pin J2 high until the beginning of the last bus cycle. SACK will be unasserted as soon as pin J2 goes low, and the input on J2 can, therefore, be a pulse or a level. Pin J2

is active only when the Master signal is asserted (pin N1 is low), and, therefore, pin J2 may be permanently grounded if only one bus cycle is done for each request.

NOTE

The M7820 requires pin J2 to be grounded for the interrupt section of the module to work, so the M7821 is compatible.

The BR half of the module does not have the ability to hold BUS SACK asserted and always drops SACK when BUS BBSY is asserted. However, this section of the module does have some special circuitry that looks at the BUS NPR line, which must be wired to pin J1 on the M7821. This circuitry, if it sees the assertion of the bus grant line to which the module is wired while BUS NPR is asserted, will block the grant and return SACK. When BBSY becomes unasserted from the last bus master, the M7821 will then clear SACK off the bus. The processor will then be able to service the NPR, improving the latency time for NPR devices.

CAUTION

Only some PDP-11 processors will work with the special circuitry described above. There is a jumper on the M7821 module which, when cut, prevents the special circuitry from working.

NOTE

Pin J1 is unused on the M7820 module, and if BUS NPR is not wired to this pin, the special jumper noted above must be cut.

If both halves of the M7821 are used for BR requests, pin J2 must be grounded and the jumper may be cut as required. If both halves are used for NPR requests, pin J2 may be used as required, and the jumper must be cut. Note that if the normally BR half (Request Bus pins H2 and K2) are used for NPR's, only one bus cycle may be done per request.

The interrupt section of the module has been changed slightly also. The jumpers on the M7821 module must be left in to generate a "one" in that bit position of the vector, and cut out to generate a "zero." This is the reverse of the M7820. A jumper has also been added to vector bit 2. If the module is to be used the same way as an M7820, the jumper for bit 2 must be left in. However, if only one vector is being generated by the module, pin D2 should be permanently wired to a high level, and then the jumpers can be used to assign vectors to every vector location (4 bytes) without changing backpanel wiring. Note that the jumper for bit 2 must also be in for a one and cut for a zero.

Summary of Compatibility Considerations

On the M7820, pin J2 must be grounded for the interrupt section to work. If pin J2 is grounded, then an M7821 module can be directly plugged in if the special jumper is cut, the vector bit 2 jumper is left in, and the rest of the jumpers are cut appropriately.

CHAPTER 7

INTERFACE EXAMPLES

Examples of interface designs in Paragraphs 7.1 to 7.9 use the techniques and equipment described in previous chapters. To draw attention to the design features of each interface type, a series of related examples is presented. The first example is a simple basic interface. Each additional example implements several features by adding logic circuits to the previous example. Thus, the first example is the simplest possible read/write interface. This circuit is then used with additional logic to form a program-controlled interface, which in turn is used with additional circuits to form an interrupt-serviced interface, until finally, the circuit is used with additional circuits to form a direct-memory-access interface.

The examples cover input and output transfers and also illustrate techniques for combining the two functions into one interface. Each example includes a description of the operation and logic of the interface, a typical implementation, and programming methods that might be used to operate a device with the interface.

7.1 BASIC INTERFACE

The simplest possible interface, a basic read/write interface, is used when data is transferred to and from the register during bus operations. This particular read/write interface consists of only a storage register and bus gating circuits. The register may be used either as a data register or may be used to drive an output device, such as a set of indicator lights.

7.1.1 Interface Operation

When the basic read/write is used, data transfers are under control of the program and the register is assigned an address on the UNIBUS. During execution of an instruction that addresses the interface, the processor conducts a bus data transfer with the interface register, which responds as a slave. Since a 16-bit register is used, it may be addressed as either a one word register or as two byte (8-bit) registers.

As shown in Figure 7-1, the basic interface uses an M105 Address Selector module to decode the UNIBUS address lines and to control the clocking of information into the register and the gating of output information from the register to the bus data lines. The register is interfaced to the bus input data lines by ungated receivers, and the inputs are clocked into the register by a strobing signal derived from the M105 Address Selector. The register outputs are gated through the drivers by the GATE REGISTER TO BUS signal. This output gating is necessary to prevent the register from affecting the UNIBUS data lines when the interface is not participating in a bus data transfer operation.

7.1.2 Data Transfer Operation

The read/write interface can participate in both DATI (or DATIP) and DATO (or DATOB) transfers. Whenever the processor conducts a DATO transfer to the bus address assigned to the read/write register, the data

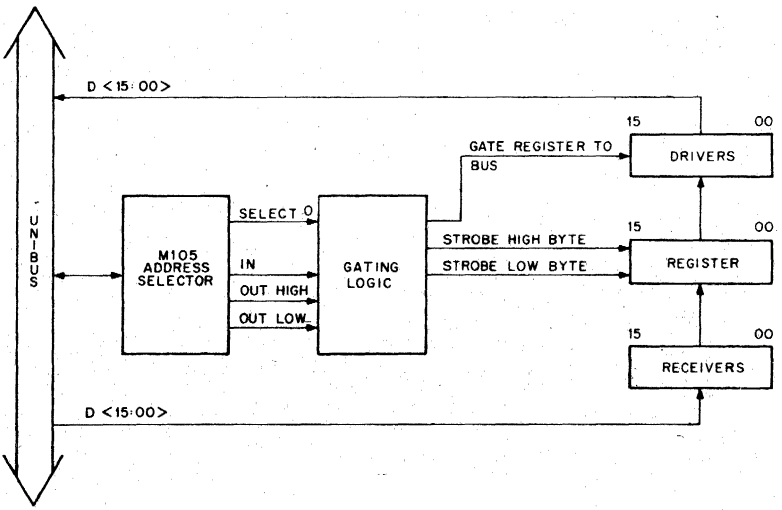


Figure 7-1 Basic Interface (block diagram)

is applied through the bus receivers to the register input. At this time, both the OUT HIGH and OUT LOW signals are produced by the M105 Address Selector. When MSYN is asserted by the processor, the decoded address causes the M105 to produce a SELECT 0 signal which is gated by the two OUT signals to clock data into the register. The UNIBUS timing guarantees that at the slave device data is valid 75 ns prior to assertion of MSYN. Therefore, the inputs have settled before the positive-going transition of the clock signal occurs.

A DATOB transfer functions in a similar manner, except that only one byte of the register is clocked. If address line A00 is 0, the M105 Module asserts OUT LOW but not OUT HIGH. If A00 is 1, then only OUT HIGH is asserted. In either case, data is only strobed into the appropriate byte tion of the register.

When a DATI transfer occurs, the processor addresses the interface and asserts MSYN. In addition, the M105 Module asserts the same SELECT 0 signal. However, in this case, the SELECT 0 is gated by the IN rather than the OUT signals. The IN signal is generated by the state of the bus C lines. Gating of the SELECT 0 signal by the IN signal produces a GATE REGISTER TO BUS signal that gates the output data from the register to the UNIBUS. The M105 Module generates SSYN to indicate that data is ready on the output bus data lines.

7.1.3 Circuit Implementation

Figure 7-2 illustrates a possible method of implementing the circuits in the basic read/write interface. The types and quantities of modules used are: the M105 Address Selector Module (one); the M785 Bus Transceiver Module (two); the M206 General-Purpose Flip-Flop Module (three); and the M617 4-Input Power NAND Gate Module (one). The modules are interconnected and may be mounted in a BB11 System Unit as shown in the insert on Figure 7.2.

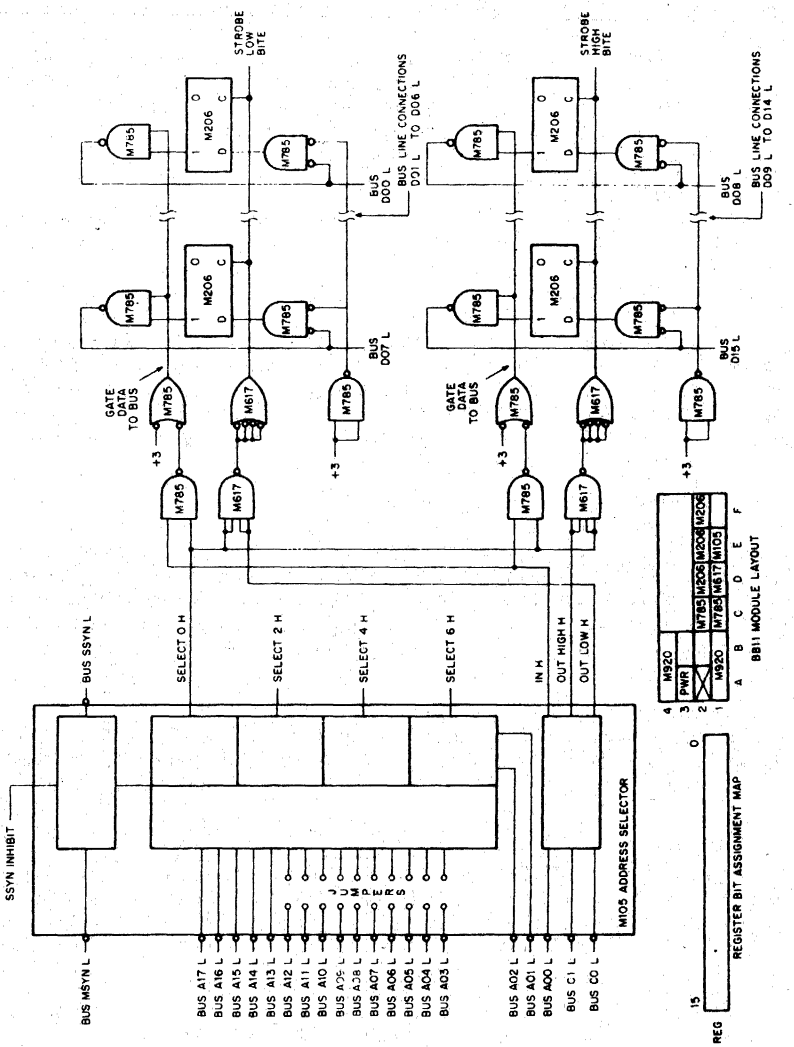


Figure 7-2 Basic Interface (schematic diagram)

Input data flows from the UNIBUS, through the input gates on the M785 Modules, to the data inputs of the M206 Flip-Flops comprising the register. The gating provided on the M785 Receivers is not used, and all gates are wired to continuously receive data. Data stored in the register is protected from these changing inputs by the requirement for a clocking signal to load data into the register.

The output data from the register is gated to the bus data lines through the driver sections of the M785 Modules. The M785 Modules are used in this example because the M785 provides the exact combination of input and output gates needed for an 8-bit read/write register. When the number of receivers differs from the number of drivers required in a specific interface, combinations of M783 Bus Driver Modules and M784 Bus Receiver Modules may be used. This example is devoted to illustrating the use and interconnection of bus drivers and receivers rather than indicating the specific modules used in implementation.

7.1.4 Programming the Interface

All data transfers in the basic read/write interface are under processor control, and all memory reference instructions may directly address the interface. If the mnemonic REG is assigned to the register address, the instruction MOV REG, R4 reads the data stored in the register (a DATI operation) and places the data in general register 4 of the processor. The instruction MOV R4, REG reverses the data flow so that the data in general register 4 is placed in the interface register (a DATIP, DATO operation). Any instruction that can access a bus address can conduct data transfers with the interface register. Therefore, the contents of the register may be incremented by an INC REG instruction or summed with an arbitrary value by an ADD VALUE, REG instruction.

7.2 PROGRAMMED DEVICE INTERFACE

A circuit similar to the one in the preceding example is used as the basis for the program controlled interface to an analog-to-digital converter (ADC). The ADC is simply a representative example of many possible external devices that may be interfaced with a design similar to the one discussed in this section. The ADC input and output signals, however, are covered in the following paragraph because of the requirements they place on the interface.

7.2.1 Analog-to-Digital Converter

The analog-to-digital converter used in this example consists of a multiplexer and converter. (See Figure 7-3.) The multiplexer selects one of 64 analog inputs and applies it to the converter, which produces the digital equivalent of the analog input.

The interface must provide seven input control signals to the ADC. One input is the START CONVERSION signal, which is a positive transition that causes the ADC to begin the conversion process. The other six control signals are applied to multiplexer address lines so the ADMUX register can be used to select one of the 64 analog inputs.

The interface receives 11 output signals from the ADC. One of these is the CONVERSION COMPLETE signal. When the conversion process starts, the CONVERSION COMPLETE signal becomes OV and remains at that level until the conversion is finished. At that time the signal becomes + 3V to

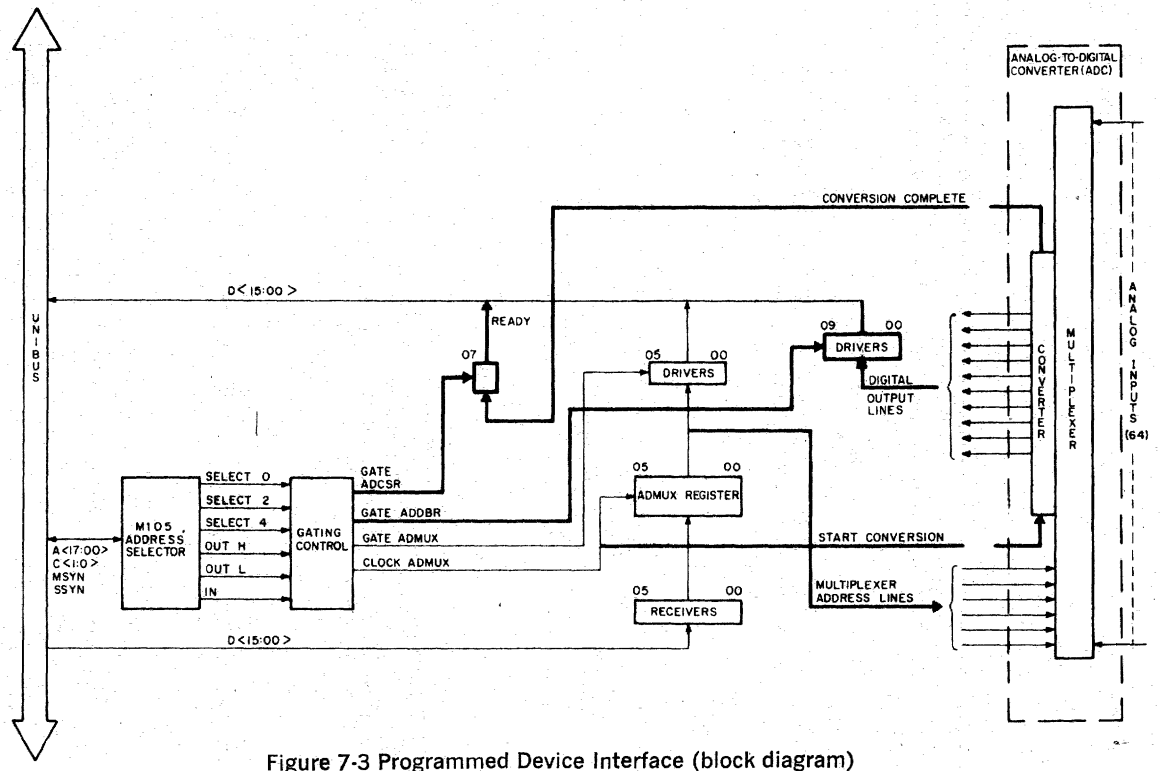


Figure 7-3 Programmed Device Interface (block diagram)

indicate that the digital output reflects the analog input (the conversion is complete).

The remaining ten output lines represent the digital equivalent to the analog input. A zero on any line is indicated by OV and a one is indicated by + 3V.

Signal levels used in the interface are standard DEC levels.

7.2.2 Interface Description

The program controlled interface allows the program to select a specified analog input for application to the ADC and then causes the resultant digitized output and conversion complete signal to be placed on the UNIBUS data lines to transfer data into the bus master.

The heavy lines in Figure 7-3 indicate logic added to the interface of the previous example. The interface functionally operates with three bus addresses. One address is assigned for the multiplexer (ADMUX) register, which is similar in design to the register in the prevous interface example. The second address is for the converted digital output (ADDBR) of a read-only register, and the third address is assigned to a 1-bit control and status register (ADCSR).

The M105 Module decodes the bus address to produce one of three select signals depending on which register is being accessed. The three select signals are gated by IN and OUT LOW to produce the four signals (GATE ADCSR, GATE ADDBR, GATE ADMUX and CLOCK ADMUX) shown in Figure 7-3. Only the ADMUX register accepts inputs from the UNIBUS through the receivers. However, the outputs of all three registers are gated to the bus through separate sets of bus drivers.

Connections between the ADC and interface may be made by a cable connector such as the M908 Module.

7.2.3 Transfer Operations

The program controlled interface participates in bus data transfers in substantially the same manner as the basic interface described in Paragraph 7.1. Each of the three interface registers can be read during a DATI operation. In addition, the multiplexer (ADMUX) register can be loaded by a DATO operation. Although only the multiplexer register accepts data during a DATO, the other two registers respond when a DATO cycle occurs. If any of the three registers is addressed during a DATO, the M105 Module produces SSYN to complete the bus operation. This is necessary to operate the interface with the processor because the destination operand of all instructions that reference data (except TST, CMP, and BIT) is transferred by a DATIP, DATO sequence of bus operations. If the interface does not respond to the DATO operation, the processor cannot continue with the program.

7.2.4 Circuit Implementation

Figure 7-4 includes a map of bit assignments for the three registers and a layout for mounting the logic modules in a BB11 System Unit. Neither the M105 Address Selector Module nor the ADC is shown on the figure, but the signals generated by these units are indicated. The connections to the UNIBUS can be implemented with one M785 UNIBUS Transceiver Module for the multiplexer register and one M783 UNIBUS Transmitter

Module for the data and control registers. Separate gating must be supplied to use one of the four individual bus drivers on the M783 for a READY bit. The CONVERSION COMPLETE signal is renamed to READY after it passes through the bus transmitter.

7.2.5 Programming the Interface

The START CONVERSION signal, which begins the device cycle, is generated in this interface by the CLOCK ADMUX signal, which loads the multiplexer register. In normal operation, the processor loads the multiplexer register; this action starts the ADC; tests the READY (CONVERSION COMPLETE) bit until the bit is set; and then transfers the data from the digital output lines of the ADC to the processor. A possible sequence of instructions to perform this task is given below. This program selects an input, waits for the device to complete the conversion, and then transfers the result to register 4.

```
        MOV   INPUT, ADMUX   ;SELECT ANALOG INPUT
READY:  TSTB  ADCSR          ;CHECK FOR CONVERSION COMPLETE
        BPL   READY          ;NO, TEST AGAIN
        MOV   ADDBR, R4      ;YES, OBTAIN DATA
```

INPUT IS A LOCATION CONTAINING THE NUMBER OF THE DESIRED ANALOG INPUT LINE.

A SUBROUTINE TO EXAMINE A SERIES OF INPUTS MIGHT BE WRITTEN AS FOLLOWS:

```
MUXSCN: MOV   BUFADR, R4     ;INITIALIZE DATA POINTER
        CLR   ADMUX          ;SELECT INPUT LINE ZERO
LOOP:   TSTB  ADCSR          ;CHECK FOR CONVERSION COMPLETE
        BPL   LOOP           ;NO, TEST AGAIN
        MOV   ADDBR, (R4) +  ;YES, PLACE DATA IN BUFFER
        CMP   ADMUX, #77     ;LAST LINE?
        BEQ   DONE           ;YES, GO TO DONE
        INC   ADMUX          ;NO, GO TO NEXT INPUT
        BR    LOOP           ;GO TO LOOP
DONE:   RTS   R7             ;EXIT FROM SUBROUTINE
```

```
WHERE:  BUFADR IS A LOCATION IN CORE CONTAINING THE ADDRESS
            OF THE FIRST WORD ON A 64-WORD BUFFER
        ADCSR IS THE INTERFACE STATUS REGISTER
        ADMUX IS THE MULTIPLEXER REGISTER
        ADDBR IS THE DATA REGISTER
```

This subroutine is called by the instruction: JSR R7, MUXSCN. The subroutine initializes general register 4 as a pointer to the buffer; initializes the multiplexer register to zero; and sequentially reads the 64 inputs into the corresponding buffer location. When each input has been read once, control returns to the calling program with the contents of general register 4 as the address of the word after the last word of the buffer.

Since loading the multiplexer register starts operation of the device cycle, ADMUX should not be accessed as a destination operand except by a TST, BIT, or CMP instruction. In addition, the INC ADMUX instruction should follow the CMP instruction. This avoids initiating unwanted device operation and allows the subroutine to be immediately recalled.

7.3 INTERRUPT SERVICED INTERFACE

The interface to an analog-to-digital converter would be more versatile if it included an interrupt capability. An interrupt serviced interface with this capability can be formed simply by adding an M7820 Interrupt Control Module and one bit to one of the registers in the programmed device interface described in Paragraph 7.2.

The interrupt serviced interface allows the processor to concurrently execute instructions of another program while the analog-to-digital converter (ADC) performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the data after it has been collected. This interface eliminates requiring the processor to spend time testing for a ready signal, such as in the case of the programmed device interface.

Whenever a device interface is required, the designer must compare the cost of additional interrupt hardware with the device requirements in terms of transfer speed, frequency of transfers, and amount of use, to determine whether a programmed device interface or interrupt serviced interface is more economical.

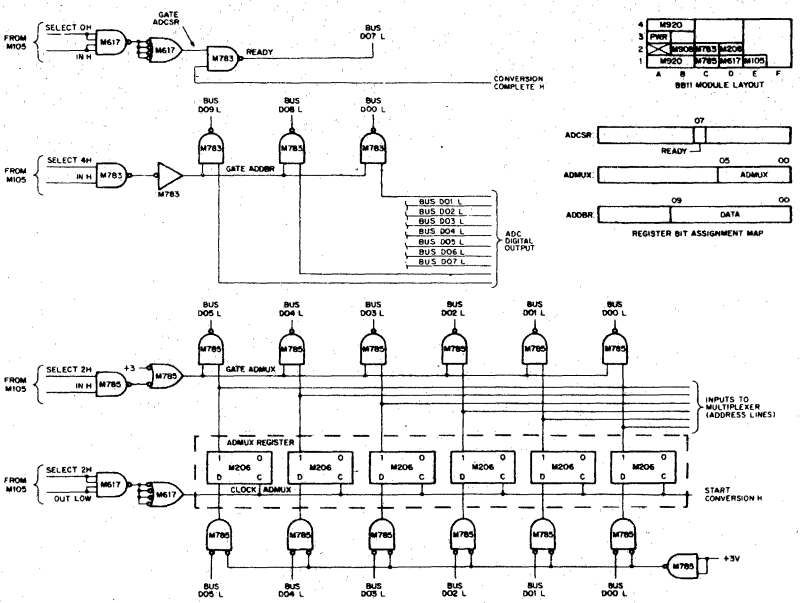


Figure 7-4 Programmed Device Interface (schematic diagram)

7.3.1 Interface Description

Figure 7-5 is a block diagram of the interrupt serviced interface which consists of the programmed device interface with the addition of an M7820 Interrupt Control Module, one flip-flop, and one bus driver. This interface can operate either in the same manner as the interface de-

scribed in Paragraph 7.2 or in an interrupt mode. The additional flip-flop is used to enable or disable interrupt operations. If the flip-flop (which is bit 6 of the control status register) is set by the program, the CONVERSION COMPLETE signal from the ADC causes the M7820 Interrupt Control Module to initiate an interrupt.

7.3.2 DR11-C Implementation

A convenient method of implementing an interrupt serviced interface is to use a DR11-C 16-Bit General Interface, Figure 7-6. A layout of the module mounted in a DD11-A System Unit, shows the savings in space and interconnections. The DR11-C is functionally equivalent to an M105, M7820, and M786. The DD11-A System unit is prewired to accept four small peripheral interfaces; e.g., DR11-C. A discussion of the DR11-C, including specifications, is presented in Chapter 4.

Figure 7-7 is similar to Figure 7-5 because the DR11-C logic is used in the same manner and with the same programs as any other logic used to implement an interrupt serviced interface. The DR11-C provides cable connectors; therefore, no additional wiring or connectors are required.

Connections between the ADC and the DR11-C are made as follows:

CONNECTOR	DR11-C	ADC
1	OUT (06:00)	Multiplexer inputs
	NEW DATA READY	Start conversion
2	IN (09:00)	Digital outputs
	REQUEST A	Conversion complete

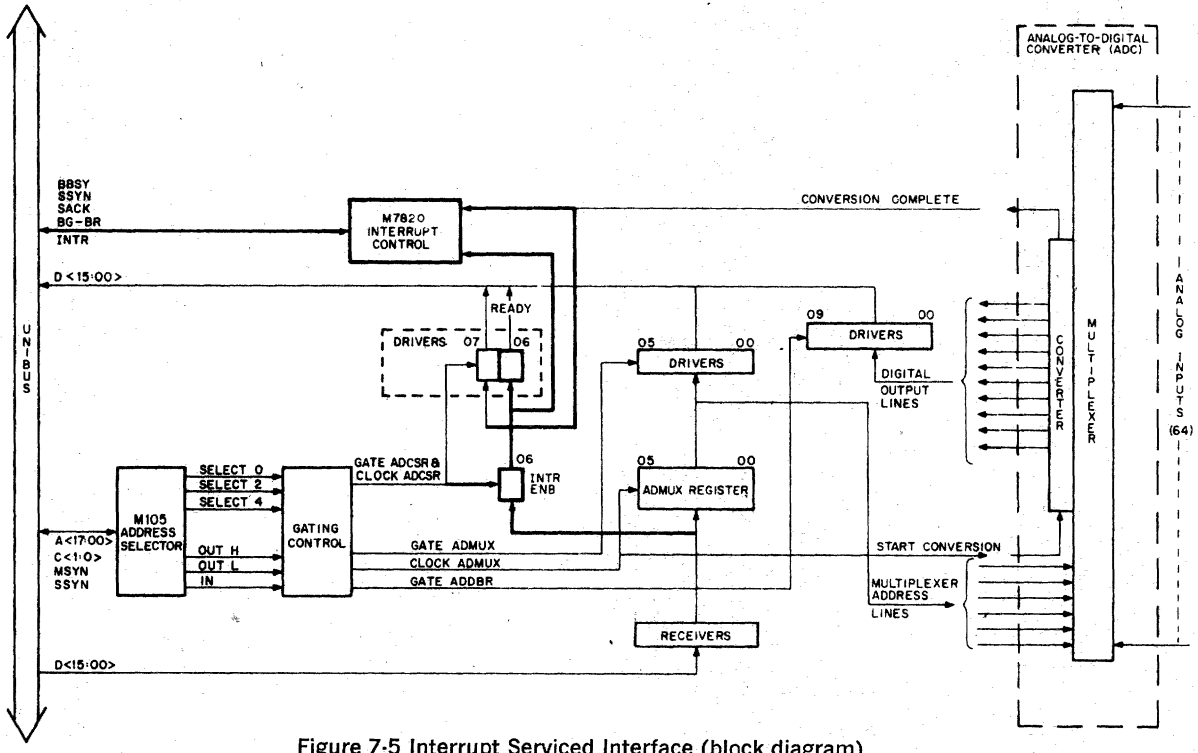


Figure 7-5 Interrupt Serviced Interface (block diagram)

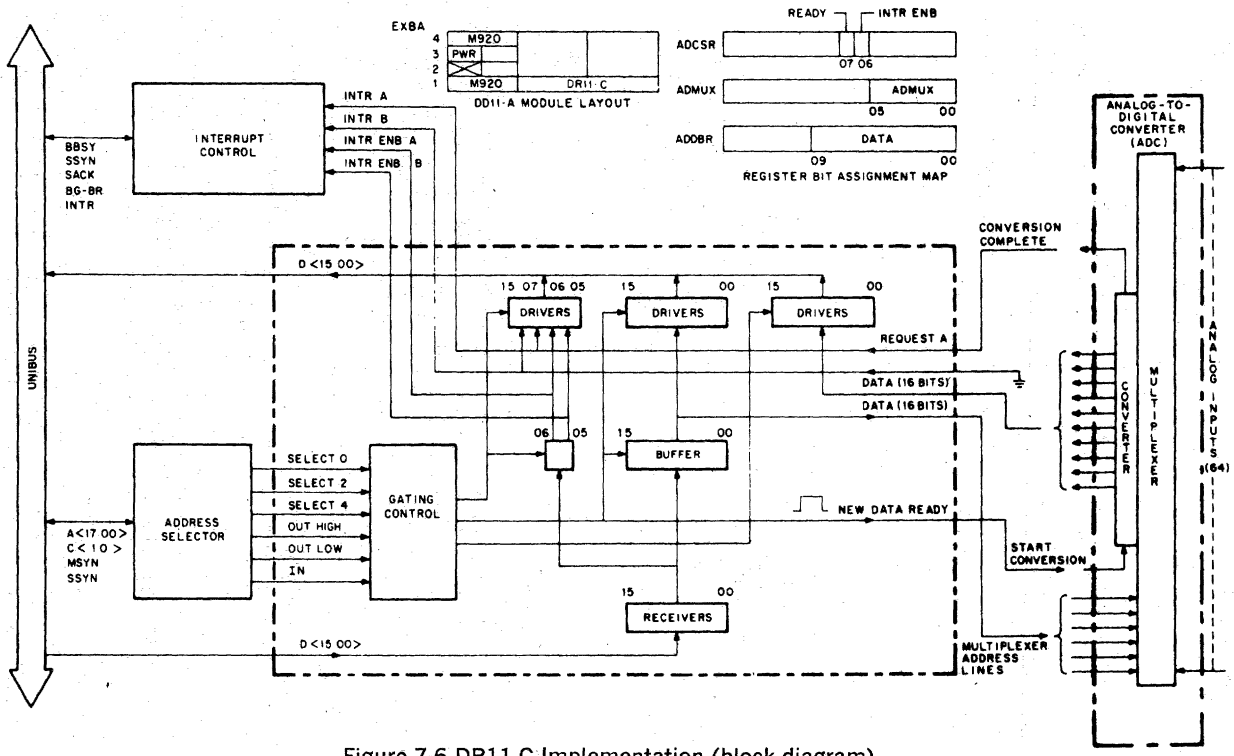


Figure 7-6 DR11-C Implementation (block diagram)

7.3.3 Interface Programming

The following program is a typical interrupt service routine that collects data from the ADC and enters an evaluation routine after the final conversion cycle.

```
ADCVEC:  ADCSER                          ;SET UP ADC VECTOR AREA
         240                             ;STATUS INCLUDES PRIORITY
                                         LEVEL 5
           .
           .
           .                             ;MAIN PROGRAM FOLLOWS
BEGIN:   MOV BUFSTRT,BUFADR              ;INITIALIZE BUFFER POINTER
         CLR ADMUX                       ;START MULTIPLEXER AT
                                         CHANNEL 0
         MOV #100,ADCSR                  ;ENABLE INTERRUPT
           .
           .
ADCSER:  MOV ADDBR,@BUFADR               ;COLLECT DATA
         CMP BUFADR,BUFSTRT + 174        ;LAST ONE?
         BEQ DONE                        ;YES, GO TO DONE
         ADD #2,BUFADR                   ;NO, INCREMENT POINTER
         INC ADMUX                       ;INCREMENT MULTIPLEXER AND
                                         ;START CONVERSION
         RTI                             ;RETURN TO MAIN LINE
DONE:    CLR ADCSR                       ;CLEAR INTERRUPT ENABLE
           .
           .                             ;FOLLOW THIS WITH THE
                                         ;EVALUATION ROUTINES
```

```
WHERE:   ADCSR,ADMUX AND ADDBR ARE THE DEVICE REGISTERS
                IN THE INTERFACE
         BUFSTRT CONTAINS THE STARTING ADDRESS OF A BUFFER
         ADCVEC  IS THE ADDRESS SPECIFIED BY JUMPERS ON THE
                 M782 MODULE AND CONTAINS THE ADDRESS OF
                 THE DEVICE SERVICE ROUTINE TAGGED ADCSER
         ADCSER DEVICE SERVICE ROUTINE

BUFADR IS A LOCATION TO BE USED BY THE DEVICE SERVICE ROUTINE
```

After the initiation instructions in the main program are executed, the interrupts cause the processor to execute the ADCSER routine. The last time this is performed, the evaluation routine is also executed.

The CLR ADMUX instruction should precede the MOV #100, ADCSR instruction to prevent the interface from causing an immediate interrupt, which could occur if the interrupt enable bit is set when the device has the CONVERSION COMPLETE signal asserted.

If the evaluation routine is to return control to the interrupted main program, this may be accomplished by terminating the evaluation routine with an RTI instruction. If any other type of return is used, the program must remove the old PC and PS that were placed on the stack by the interrupt operation. Removal is accomplished by executing an ADD #4, R6 instruction.

7.4 DIRECT MEMORY ACCESS (DMA) INTERFACE

The direct memory access (DMA) interface conducts data transfer operations to place data from the device directly into memory. A DMA interface performs a large number of transfers with minimal processor intervention thereby reducing program and execution time overhead. After the interface device registers are initialized, all transfers take place under control of the interface, thereby eliminating processing time. The processor is notified by an interrupt when all the data has been transferred and the program responds appropriately.

Figure 7-7 is a block diagram of a DMA interface for the Analog-to-Digital Converter (ADC). The DMA is designed by adding circuits to the interrupt serviced device interface. The Interface is composed of two interface registers: the ADCSR register, which contains flag and error bits; and the combined ADBAR/ADMUX register, which holds the bus address and multiplexer bits.

7.4.1 Interface Description

Interface operation begins when the program loads the bus address register (ADBAR) with the address of the first memory location where data is to be stored. The interface starts an ADC conversion cycle. When the digital data is available from the ADC, the interface requests bus use by asserting an NPR request. When the device becomes bus master, it transfers the data to core memory. Completion of the bus transfer causes the multiplexer register (ADMUX) to be incremented, thereby selecting the next input channel. The multiplexer register is part of the bus address register; therefore, the next memory location is also selected. At this point, a new conversion cycle begins. This process is repeated until each input channel is read and the digital data is stored in a core memory location. The interface then sets the ready flip-flop, which causes an interrupt.

7.4.2 Interface Implementation

The DMA interface is constructed by adding one set of bus drivers and the bus transfer control logic to the interrupt serviced interface; therefore, the functions assigned to the registers differ in this case, and implementation differs accordingly. The multiplexer register, expanded to 15 bits, also serves as a bus address register. Nine of these bits (15:07) are under program control and serve as a base address for a series of locations used as a data collection buffer by the interface. The remaining six bits (06:01) are implemented as a counter that steps through the 64 inputs and also addresses 64 successive word locations in the core memory. The six multiplexer bits are not accessible from the bus and cannot be read nor altered by the program. Whenever the high or low byte of the address register is loaded, the six multiplexer bits are cleared to zero; therefore, transfers always start on 64 word boundaries.

The interface uses an interrupt to signal completion of the series of transfers. The interrupt enable (INTR ENB) and READY bits of the ADCSR operate similar to the interrupt serviced interface. Refer to Figure 7-7.

Loading the ADBAR register (SELECT 2 OUT HIGH and/or SELECT 2 · OUT LOW) also clears the multiplexer counter and the READY flip-

flop, thereby initiating a conversion cycle by causing START CONVERSION H to become asserted.

When the conversion is complete, the CONVERSION COMPLETE H signal sets the REQUEST BUS flip-flop, which causes the M7820 Interrupt Control to assert an NPR request. When bus control is granted, the M7820 asserts BBSY on the UNIBUS and asserts the MASTER A L signal. The MASTER A L signal is tied to the M796 UNIBUS Master Control module in order to produce the START signal. Since the C1 control line is high and the C0 control line is grounded, the M796 performs a DATO bus cycle. An ADRS TO BUS H is produced to gate the nine bits of the ADBAR register and the six bits of the ADMUX register to bus address lines A<15:01>. DATA TO BUS places the converted digital value on bus data lines D<09:00>. After a minimum delay of 150 ns, BUS MSYN L is asserted.

When the slave device responds with BUS SSYN L, both ADRS TO BUS and DATA TO BUS are negated and BUS MYN L is dropped. The END CYCLE H pulse is used to clear the REQUEST BUS flip-flop, which in turn causes the M7820 Interrupt Control to drop BUS BBSY.

END CYCLE L is used to trigger a one-shot to produce the COUNT DELAY H signal. This signal serves as the count input (COUNT IN) to the multiplexer counter (ADMUX). After 600 ns, the one-shot times out and its output returns to a low (0V) level. If the READY flip-flop has not been set by a count overflow from the ADMUX counter, START CONVERSION H is asserted to start the next conversion cycle. If, however, the ADMUX counter has overflowed and set the READY flip-flop, no ADC operation is started and an interrupt bus request is made.

A TIME-OUT flip-flop is provided on the M796 module. This flip-flop is set if the slave does not respond within 20 μs to the BUS MSYN L signal that is produced by the M796 module. If TIME OUT becomes set, the bus cycle is stopped, READY is set, and further conversions are inhibited. The TIME-OUT ERROR is indicated by a 1 in bit 15 of the ADCSR. TIME-OUT is cleared by loading bit 15 of the ADCSR with a 0.

The modules required to implement this interface fit into one BB11 System Unit. All interface modules, including the M7820 Interrupt Control, M105 Address Selector, and a device cable connector, can be inserted into the logic slots of one system unit containing power and UNIBUS connectors.

7.4.3 Programming the Interface

The following is an instruction sequence to initiate device operation:

```
MOV   #BUFADR, ADBAR     ;LOAD ADDRESS AND START
MOV   #100, ADCSR        ;ENABLE INTERRUPT
```

WHERE: BUFADR IS THE ADDRESS OF THE FIRST WORD OF A BUFFER AND IS RESTRICTED TO ALL 0'S IN BITS 0 THROUGH 6.

The interrupt routine for this interface is equivalent to the data evaluation routine suggested in the interrupt serviced interface. The routine should begin with a CLR ADCSR instruction to disable further interrupts

(unless serviced at a higher priority level) and should terminate with an RTI instruction.

The ADBAR register can be read as a source operand without spurious clocking of the device operation cycle, but the ADMUX counter is not accessible from the bus.

The interrupt enable flip-flop (bit 6 of the ADCSR) is entirely under program control but the TIME-OUT flip-flop is set by TIME-OUT ERROR conditions in the interface. The ready bit of the ADCSR (bit 7) is not under program control. It may be read by the program but cannot be altered except by initiating operation of the device.

7.4.4 Interface Operation Timing

Figure 7-8 illustrates the timing relationship among signals in the DMA interface. The curved lines indicate the changes in signal level that generate the indicated results.

7.4.5 Interface Options

As described above, operation of the DMA interface is restrictive, because it must always scan 64 channels. A simple method of reducing the number of channels scanned is to alter the set/reset inputs to the M211 Binary Counter module, thereby preloading it with a non-zero constant from which it can begin counting up.

An even more flexible arrangement could be designed by separating the ADBAR and ADMUX registers, thereby allowing independent bus addressing and multiplexer scanning.

7.5 OUTPUT INTERFACE WITH INTERRUPT CONTROL

Preceding examples have illustrated various types of interfaces for peripheral devices that provide inputs to the UNIBUS data lines. This example, as well as the example in Paragraph 7.6, covers interface design for a device that accepts UNIBUS outputs. The device shown is meant to be typical of output devices which may be interfaced by designs similar to the following examples.

7.5.1 Device Description

A digital-to-analog converter (DAC) is a device that accepts UNIBUS outputs. The DAC converts a binary weighed number into a scaled analog voltage. The device is single-buffered and the analog output corresponds to the digital input.

The interface provides 10 binary level inputs to the DAC. These inputs represent the digital value equivalent to the analog voltage desired as an output. The binary levels are 0V for logic 0 and + 3V for logic 1.

The DAC provides an update request output signal for the interface. This signal requests a new digital input from the interface. At intervals determined by the DAC, a high level (+ 3V) pulse is provided as the update request signal. This level remains low (0V) between pulses.

7.5.2 Interface Description

The output interface with interrupt control provides a buffer register for outputs to the DAC and an interrupt control to service the DAC with an interrupt service routine. Figure 7-9 is a block diagram of the output interface.

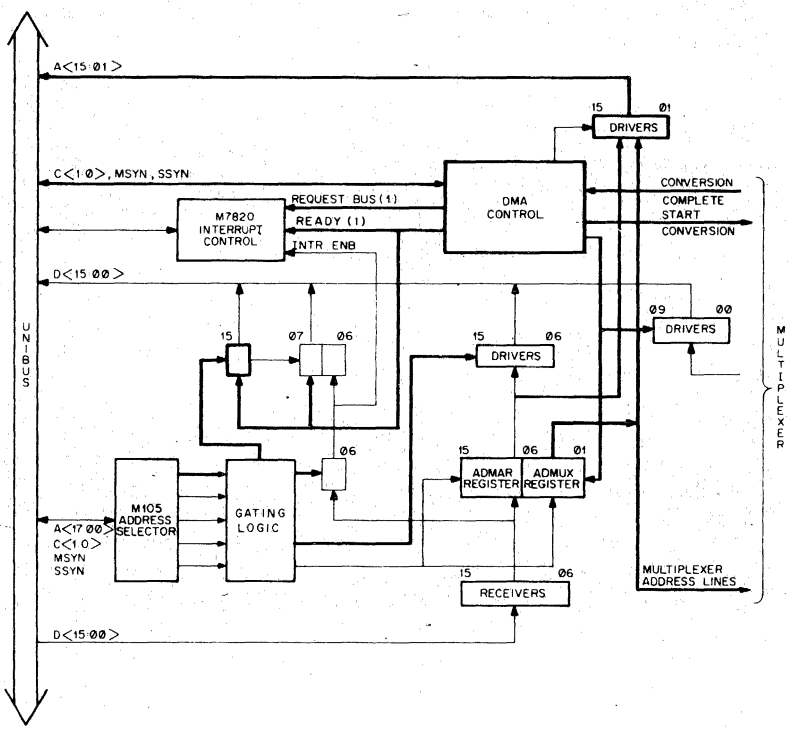


Figure 7-7 DMA Interface (block diagram)

The interface consists of two registers, an M105 Address Selector Module, an M7820 Interrupt Control Module, bus receivers, and two sets of bus drivers. The two registers are the data buffer register (DADBR) and the control status register (DACSR). The request bit (bit 7) of the DACSR can be read by the bus but cannot be loaded directly from the bus. All other register bits are under direct bus control.

7.5.3 Interface Operation

When the UNIBUS addresses the data buffer register during a DATO transfer, the interface clocks the information from the bus data lines into the register, which then applies the information to the DAC as the 10 binary level inputs. At the same time data is clocked into the register, the REQUEST flip-flop (bit 7 of the DACSR) is cleared. After this transfer is complete, when the peripheral device requests another value, the REQUEST flip-flop is clocked high by an UPDATE REQUEST signal from the DAC. If the interrupt enable flip-flop (bit 6 of the DACSR) is set, the interface asserts a bus request line. On becoming bus master, the interface performs an interrupt operation to transfer program control to a service routine. This routine loads new data into the buffer register and then returns control to the interrupted program.

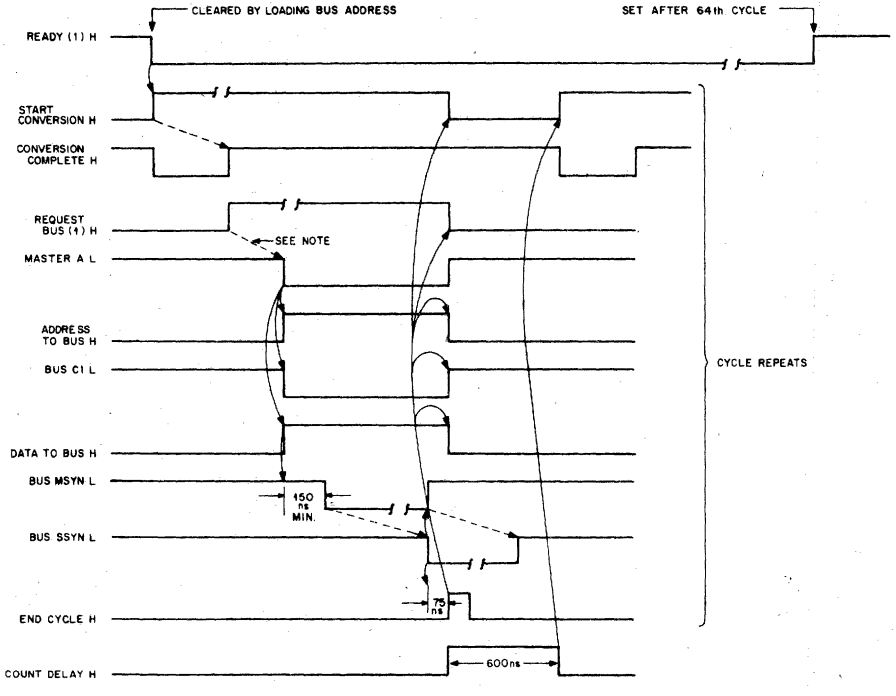


Figure 7-8 DMA Interface (timing diagram)

During normal operation, data is loaded into the buffer register and transferred to the peripheral device. When an UPDATE REQUEST from the DAC starts an interface cycle, the interrupt vector is transferred to the processor. The processor again initiates the data flow by transferring a new word of data into DADBR.

7.5.4 Interface Programming

The programs described in this paragraph cause the DAC to output a time-varying signal by loading the DADBR with an initial value and then changing that value by small increments until it reaches a final value determined by the program. The analog output is 100 cycles of a triangular waveform (actually, a stepped triangular waveform) with the slope of the ascending portion equal to half the slope of the descending portion. The period of the waveform is 150 times the period between update request pulses.

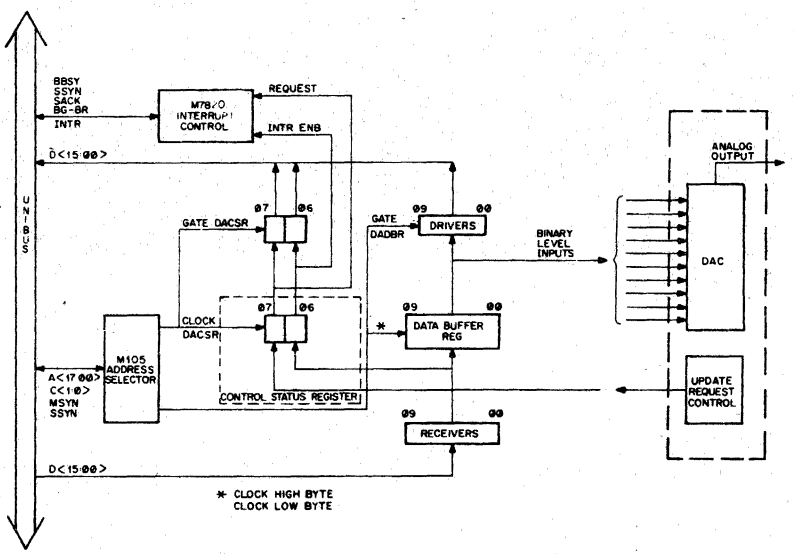


Figure 7-9 Output Interface with Interrupt Control (block diagram)

In the interface program, the DAC output is reset to a higher value by the ADD #10. DADBR instruction or reset to a lower value by the SUB #20, DADBR instruction. In either case, the value in the DADBR is read, modified by an arithmetic operation, and the new value is stored in the DADBR. All these operations are under processor control.

The ability of the UNIBUS to access device registers as though they were memory locations allows the processor to directly perform tests and modifications on the device register. This program compares the value in the DADBR with the test values. The program uses a minimum of stored data because it is not necessary to use memory locations for counters or storage of temporary values.

The processor initializes operation by executing the following sequence of instructions:

```
CLR     DADBR           ;CLEAR DATA BUFFER REGISTER
CLR     DASW            ;RESET UP/DOWN SWITCH
MOV     #144, DACNT     ;INITIALIZE CYCLE COUNTER
MOV     #100, DACSR     ;SET INTERRUPT ENABLE
```

The interrupt service routine includes the following instructions:

```
DAVEC:  DASERV                      ;POINTER TO SERVICE ROUTINE
        240                         ;PROCESSOR PRIORITY = 5

DASERV: TST     DASW                ;SWITCH SET?
        BPL     UP                  ;NO, GO UP
        SUB     #20, DADBR          ;YES GO DOWN
        BNE     CONT                ;OUTPUT VALUE EQUALS 0?
        CLR     DASW                ;YES, RESET SWITCH
        DEC     DACNT               ;REDUCE COUNT BY ONE
        BNE     CONT                ;COUNT EQUALS 0?
        CLR     DACSR               ;YES, DISABLE INTERRUPT
                                    AND EXIT
        RTI

UP:     ADD     #10, DADBR          ;OUTPUT VALUE GOES UP
        CMP     DADBR, #1000        ;1000 IS TOP LIMIT ON VALUE
        BNE     CONT                ;DOES VALUE EQUAL TOP LIMIT
        COM     DASW                ;YES, SET SWITCH

CONT:   RTI                         ;EXIT FOR INTERMEDIATE
                                    VALUES
```

7.6 DAC-DMA INTERFACE

A direct memory access (DMA) interface designed for a digital-to-analog converter (DAC) allows a specified number of words from memory to be transferred directly to the interface without processor intervention.

The previous interface example (paragraph 7.5) described a digital-to-analog converter interface that was serviced (controlled) by the vectored interrupt structure. In a real-time system where the time to service repetitive interrupts demands too much processor time, it may become necessary to expand the control section of the interface, so that the interface is less dependent on processor control, thereby reducing processor overhead.

This interface example uses the same DAC as the one discussed in the previous example. However, the interface to the UNIBUS differs. Added to the interface control section are direct bus access logic circuits, a word count register, and a bus address register. These additions allow a specified number of words from a particular group of memory addresses to be transferred directly to the interface, independent of processor control. This interface may be used, for example, to drive the X-Y deflection circuits of a CRT display scope in a refresh direct from memory mode.

7.6.1 Interface Description

A block diagram of the DAC-DMA interface is shown in Figure 7-10. The

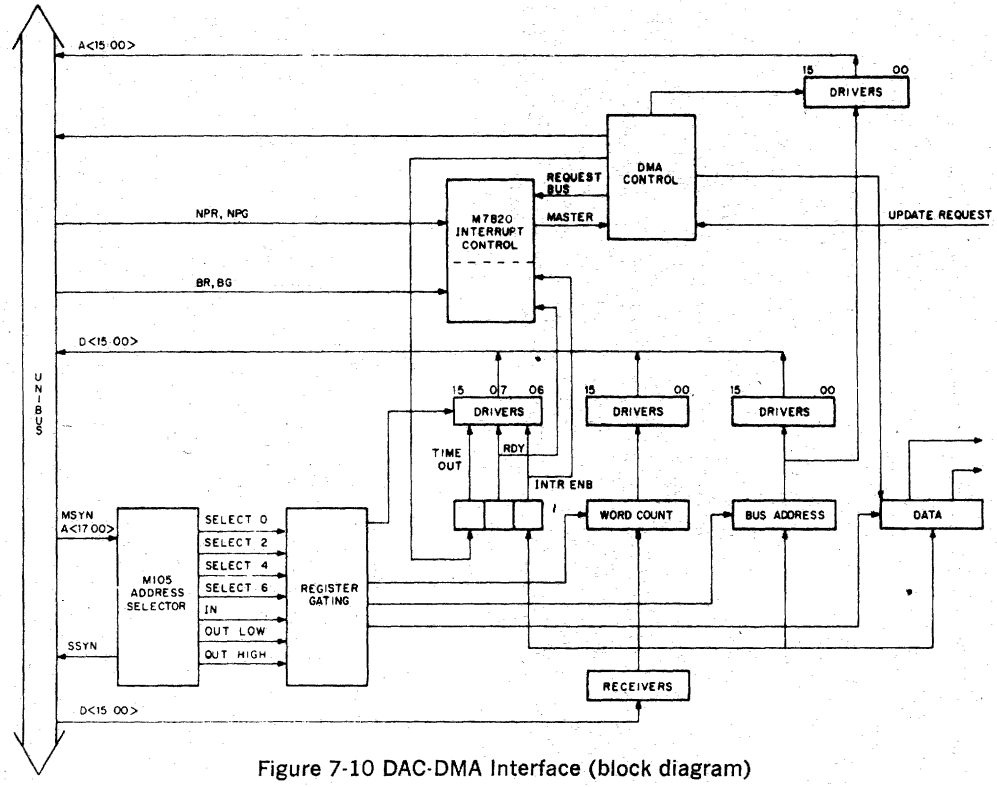


Figure 7-10 DAC-DMA Interface (block diagram)

interface contains four registers: a DAC control and status register (DACSR) which contains control and status information; a DAC word count register (DAWC) which holds the 2's complement of the number of words to be transferred; a DAC bus address register (DABA) which indicates where the block of information is held in memory; and a DAC data buffer register (DADB) which buffers information during bus cycles and which can also be loaded under program control.

A typical method of programming this interface is to first initialize the control by loading the DAWC and DABA registers. The next step is to set the GO bit in the DACSR. Words of data are then sequentially taken from memory and loaded into the DADB register at a rate set by the DAC or by an external clock. After each transfer (which is under the control of the interface rather than the processor), the DAWC and DABA registers are incremented. Data transfers continue until the DAWC register overflows (goes to all 0s). At this point, a READY bit in the DACSR is set. The READY bit can cause an interrupt to occur (provided INTR ENB is set), thereby notifying the processor that the block transfer is now complete, and another block transfer can be started.

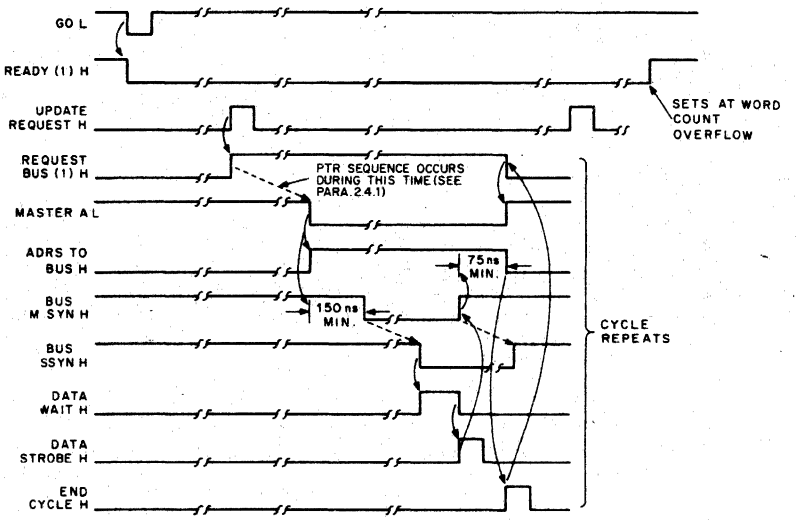


Figure 7-11 DAC-DMA Interface (timing diagram)

CHAPTER 8

SITE PLANNING

8.1 GENERAL

8.1.1 Scope

This chapter provides electrical, physical, and environmental data to aid in planning a successful computer installation. Since there is a wide choice for the Central Processor Unit (CPU) among the 11 Family, and numerous combinations of peripherals within a system, all possibilities cannot be covered. However, pertinent and useful information is given that will apply to most configurations.

8.1.2 Planning Assistance

Digital Equipment Corporation will provide customer assistance in all phases of site planning. Sales Engineers and Field Service Engineers are available for advice regarding site and installation planning. Various maintenance and service options are available for your systems. In general, trained DEC people will perform the detailed configuration work required.

8.1.3 Installation Constraints

The route that the equipment is to travel from the receiving area to the installation site should be studied and measurements taken to facilitate and assure delivery of the equipment. Check the size of doors, passageways, ramps, etc. for height, width, and turning radius to see if there are any receiving or installation problems. Take into account the size of the moving equipment and the shipping skid (wooden platform for moving) under the equipment cabinets. If an elevator is to be used, DIGITAL should be notified of any size or gross weight limitations. If problems in movement are found, DIGITAL must be notified at least 1 month prior to the shipping date. Special packing and shipping provisions can then be made.

8.2 COMPUTER SITE

8.2.1 Site Considerations

Although each system site will differ, the following points should be considered:

a) Space for the equipment and the working and servicing area.

b) Availability and location of adequate power (voltages, current, tolerances on voltage and frequency).

c) Proper fire and safety precautions.

d) Environmental requirements (air conditioning and/or humidifying equipment).

e) Building requirements (floor load, location of cables and other equipment).

f) Efficient work-flow pattern to other work areas, ease of visual observation of input/output devices.

g) Sufficient storage space for supplies necessary to the operation of the system.

h) Future system expansion.

Operational requirements determine the specific location of the various free-standing peripherals of the system. Peripherals must be located so that the length of connecting cables will not exceed maximum limits.

Fire and Safety Precautions

The following fire and safety precautions are presented as an aid in providing an installation that affords adequate operational safeguards for personnel and system components.

a) If an overhead sprinkler system is used, a "dry pipe" system is recommended. This type of system, upon detection of a fire, removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

b) If the fire detection system is of the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.

c) If an automatic carbon-dioxide fire protection system is used, an alarm should sound on release of the CO_2 to warn personnel within the installation.

d) If power connections are made beneath the floor of a raised-floor installation, waterproof electrical receptacles and connections should be used.

e) An adequate earth ground connection must be provided for the protection of operating personnel.

All personnel working in the computer area should be trained in such emergency measures as:

a) Proper method of shutting off all electrical power.

b) Handling fire extinguishers in the correct manner.

c) Evacuating personnel and records and calling the fire department.

Protection of Data

Special safeguards should be taken to protect vital data such as business records or other data which are either very expensive or impossible to duplicate. Adequate duplicate copies of vital data should be stored away from the computer system site, normally in a fire-proof storage

vault. In most cases, a regular program of updating the duplicate data is necessary to maintain the value of such back-up storage.

Floors
Most office buildings and industrial plant floors are rated for at least 50 lbs/ft² (244 kg/m²) and will sustain the weight of any standard PDP-11 system.

Small systems with few peripherals do not require raised flooring; even larger PDP-11 systems can be installed without it. However, a raised floor is a desirable feature for several reasons:

a) Protection of power and interconnecting cabling

b) Safety to personnel (no cabling to trip on)

c) Minimum cost for future layout changes

8.2.2 System Reliability
The reliability of a computer system is a complex function of the task it is expected to perform and its environment. The task establishes criteria which define when the system has failed and to what extent. A computerized telephone switching center might allow a total of only two hours of complete inoperativeness in twenty years but might not consider computation errors or failure of parts of the system as serious errors. An on-line laboratory computer, on the other hand, may require complete error-free operation for several hours, but allow substantial amounts of scheduled down-time before and after the experiment. Some of the non-environmental factors to be considered are listed below:

a) Time interval before data is irretrievably lost.

b) Use of a small, independent subsystem for data capture.

c) Significance of a data error.

d) Significance of extended down-time.

e) Partially or completely redundant system with manual or automatic system changeover.

f) Graceful system degradation upon subsystem failure.

g) I/O device-independent software.

High temperatures increase the rate of deterioration of virtually every material. Temperature cycling and thermal gradients induce temporary and permanent microscopic changes in materials. High absolute humidity (dewpoint) causes moisture absorption and dimensional and handling changes in paper and plastic media (line printer paper, cards, paper tape, magnetic tape, etc.).

Low humidity allows the build up of static electricity. Lack of air cleanliness results in reduced life of tapes, excessive head wear, and early data errors in all moving magnetic storage media (drums, disks).

The combination of static electricity and air-borne dust is particularly detrimental to magnetic tapes. Vibration can cause slow degradation of mechanical parts and, when severe, may cause data errors on disks and drums.

High power radio frequency pulses conducted through the power mains or radiated through space, when severe, may cause hardware logic errors. Such pulses can come from radar installations or nearby broadcasting stations and welding operations; and from less obvious sources such as nearby arcing relay or motor contacts and the arcs which occur when static electricity is discharged. In extreme circumstances, filtered or isolated power mains and/or radio frequency shielding (a screened room) may be required.

All these environmental factors cause slowly accumulated sources of eventual failure.

8.2.3 System Environment

General

The recommended computer room environment has an air distribution system which provides cool, well-filtered, humidified air. The room air pressure should be kept higher than the pressure of adjacent areas to prevent dust infiltration.

Most equipment is air cooled, the air being circulated internally by blowers in each unit. On standard PDP-11 cabinets, air enters the unit through a filter and blower in the top of the cabinet and exits through the bottom.

For efficient equipment cooling, a minimum clearance of 30 inches (76 cm) above the equipment cabinets is recommended. If this requirement cannot be met, other means of allowing free air flow above and around the equipment must be devised.

Because the electronic equipment is constructed mainly from low power integrated circuits, PDP-11 systems do not dissipate much power. Air conditioning requirements can be estimated conservatively by figuring on an average dissipation of 1400 watts (4700 BTU/hr) for each cabinet in the system. A single, heavily loaded cabinet may dissipate as much as 2300 watts.

Temperature and Humidity

PDP-11 CPU's were designed to operate in a temperature range of 10°C to 50°C, and relative humidity of 20% to 95% (non-condensing). However, the properties of paper cards, line printer paper, and magnetic tape limit the environment of systems which use these media.

Table 8-1 shows recommended and permissible operating conditions. Storage conditions mean that the equipment is in an operating configuration, but primary power is not applied. No condensation should occur.

Table 8-1 Equipment Operating and Storage Conditions

	Recommended Operating Conditions		Storage Conditions	
	Temp. Range	Relative Humidity (%)	Temp. Range	Relative Humidity (%)
PDP-11 Central Processor	10°C to 50°C	20 to 95	0°C to 65°C	10 to 95
Magnetic Tape	15°C to 27°C	40 to 60	15°C to 27°C	40 to 60
Magnetic Disks	17°C to 33°C	20 to 55	5°C to 45°C	20 to 80
Punch Cards	18°C to 24°C	40 to 60	5°C to 50°C	30 to 65
Line Printer Paper	15°C to 30°C	40 to 50	10°C to 43°C	10 to 80
PDP-11 System	18° to 24°C	40 to 50%		
Power Source	115 VAC ± 10%, 60 Hz ± 3% 230 VAC ± 10%, 50 Hz ± 4%			

A factor that should be considered in equipment layout is that certain equipment (notably disks and drums) is sensitive to sudden changes in temperature such as are produced by the cycling of certain types of air-conditioning equipment. These sensitive units should be located where they will not be subject to sudden changes in the air temperature. Also, the storage area for supplies, particularly paper punch cards, should be held at the same conditions as the computer room and isolated from sudden temperature changes.

Other Considerations

The following precautions are recommended:

a) Do not use steel wool for cleaning floors in the computer room. The metal fibers can enter the cabinets and short out electrical components.

b) To prevent air flow interference, do not place material on top of the cabinets.

c) Use a nonconductor type nozzle when vacuuming to minimize the possibility of an electrical accident.

d) Avoid spilling liquids (coffee, soda, etc.) on the equipment and operating controls (e.g. console switches, teletype keys and controls).

Static Electricity

Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the PDP-11 and related peripheral equipment. If carpeting is installed on the installation room floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded. Static resistant wax is commercially available.

Acoustical Damping
Some peripheral devices (such as line printers and magnetic tape transports) have a high noise level. In installations that use a group of high noise-level devices, an acoustically damped ceiling reduces the noise.

Lighting
If cathode-ray tube peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to conveniently observe the display.

Special Mounting Conditions
If the PDP-11 will be subjected to rolling, pitching, or vibration of the the mounting surface (e.g., aboard ship), the cabinets should be securely anchored to the installation floor by mounting bolts.

8.2.4 Size of Systems

Figure 8-1 shows the size of a 1 cabinet system. Dimensions are given for the physical cabinet, service area requirements, and also the size of the shipping skid (wooden platform used in moving). Information is also given for typical power dissipation and weight for 1 cabinet of equipment. A 15 foot power cord is supplied with each cabinet.

Figure 8-2 shows dimensions for 2 and 3 cabinet systems. Allow 9" in width and 12" in depth extra for the shipping skid. Figure 8-3 shows the space requirements for the LA30 DECwriter terminal. About the same amount of space should be allowed if an ASR33 Teletype terminal is used.

Appendix E shows the space requirements for the free standing peripherals.

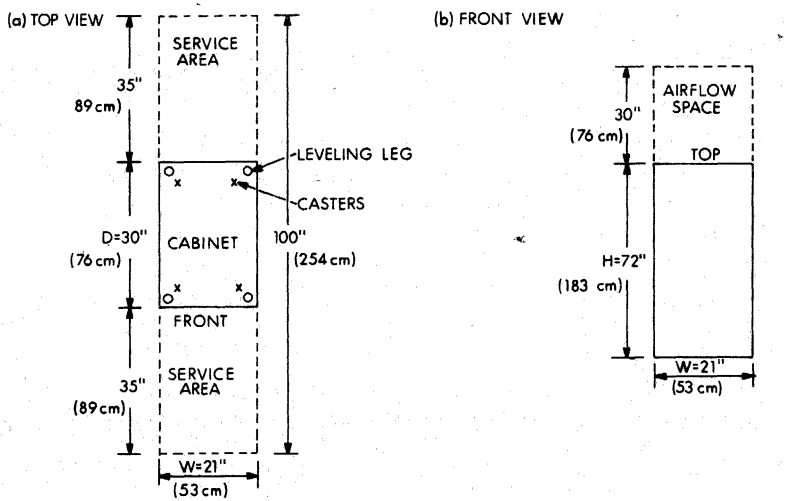
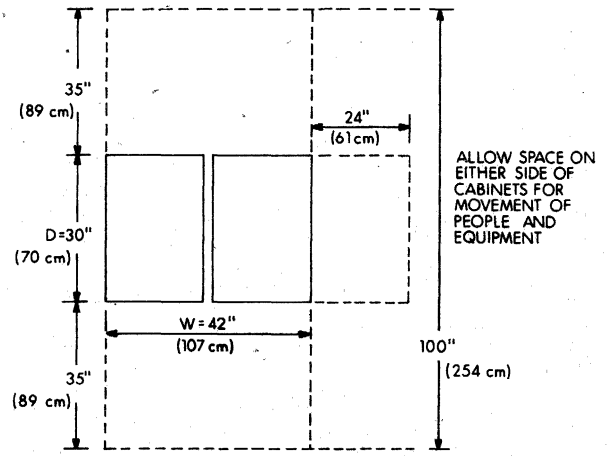


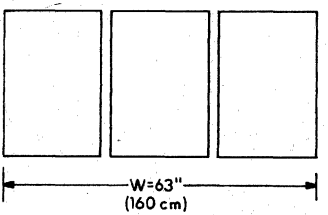
Figure 8-1 Space for 1 Cabinet

	Amps at 115 VAC	Watts	BTU/hr	Weight (lbs)
Empty Cabinet	—	—	—	120
Typ Cab	12	1400	4700	400
Heavily Loaded	20	2300	7800	600

(a) 2 CABINETS



(b) 3 CABINETS



FOR EACH CABINET, ALLOW 21 INCHES FOR WIDTH. (53 cm)

Figure 8-2 Space For 2 & 3 Cabinet Systems

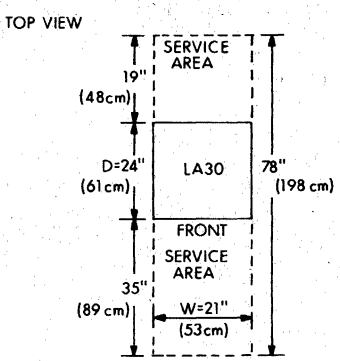


Figure 8-3 Space for LA30 DECwriter

8.3 POWER

8.3.1 Power Origination and Connections

Most AC power generated for industrial and commercial use is either a nominal 115V or 230V at 60 or 50 Hz. Figure 8-4 shows standard power generation wiring. Note the wire designation convention, as summarized in Table 8-2.

Table 8-2 Power Wiring Convention

Code	Color	Name	Function
W	White	neutral	Carries load current
X	Red	hot leads — phase 1	Carries load current
Y	Black	hot leads — phase 2	
Z	Yellow or other color	hot leads — phase 3	
G	Green	frame or equipment ground	protection line, NOT for load current

8.3.2 Grounding

For three-phase power, the fifth wire is used as the equipment ground; for single phase, the third wire. However, in both cases the ground must be connected to the metal frame of the cabinet. Ground straps must connect all the metal cabinets together.

The AC neutral **MUST NOT** be confused with protective (frame) ground. The protective equipment ground is the green conductor used in a multiconductor cable, and is used to prevent the buildup of dangerous voltages on equipment as protection for personnel, and to assure that any short circuit between a power phase and the cabinet will draw enough current to trip the circuit's protective device immediately, rather than raising the potential of the equipment to a dangerous level. **THE AC**

NEUTRAL MUST NEVER BE CONNECTED TO THE FRAME OF ANY EQUIPMENT OR TO THE PROTECTIVE GROUND, (except at the building's main electrical service entrance).

A single-point ground system should be used, and all "green wire" grounds tied together at the circuit breaker load center. The load center panel should have a copper ground bus to which all equipment grounds can be attached.

To prevent unwanted electrical signals and noise from being introduced into the computer system, the AC neutral must be isolated from all building structures, equipment frames, cabinets, panels, and grounds.

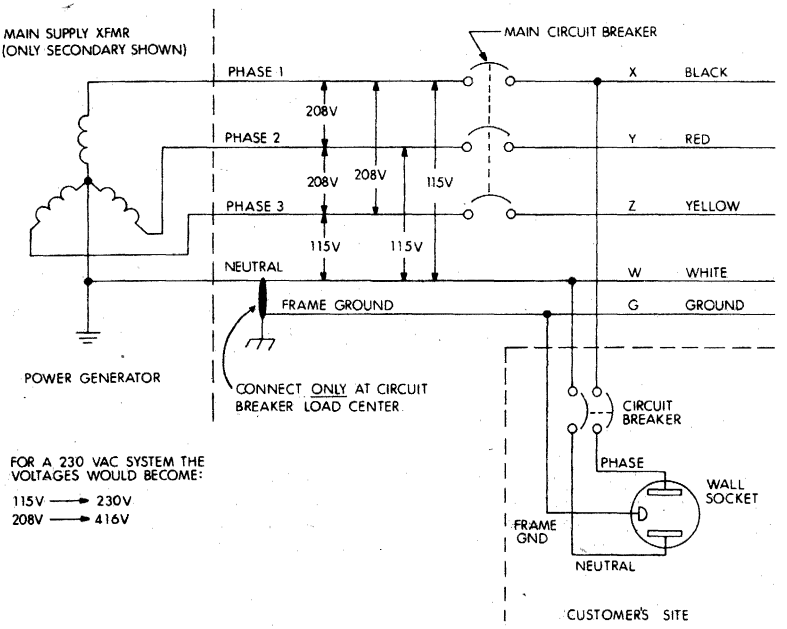


Figure 8-4 Power Wiring Schematic for 115 VAC

A system involving a digital/analog interface usually requires that the digital system ground be tied to the analog system ground at a single point, often at the analog/digital interface. A good ground connection is required in these cases. In small systems where no analog interface is involved, the grounding provided by a large electrical conduit may be adequate, although electrical conduit systems often are connected together poorly in terms of a low resistance path to ground. In large systems, additional connections to earth ground may also be advisable. All of these ground connections are in addition to (not in place of) the ground leads carried through the various signal buses and the ground conductors contained in the power cables. The green grounding wire in the power cable must also be returned to ground, usually through the conduit of the electrical distribution system.

In addition to power, each computer system should have a substantial earth ground connection to the processor frame ground made with No. 4 AWG (0.20 in., 5mm) copper wire. A building beam or large cold water pipe is adequate in many cases, although some systems may require direct connection to a grounding stake or other high-quality earth ground.

8.3.3 Customer Supplied Power

The standard PDP-11 cabinet contains a power control (mounted at the bottom of the cabinet) for the control of power to each cabinet. One 15 ft. line cord with a male plug is supplied for each cabinet, see Figure 8-5.

The customer site must supply 1 outlet for each cabinet and 1 for each free standing peripheral. In most systems it is convenient to provide a separate load center or circuit breaker panel for the computer system, and to connect each receptacle to its own circuit breaker. Diagrams and designations of applicable plugs and receptacles are shown in Figure 8-5.

Each cabinet in the system should be furnished with a separate 30 amp, 115VAC single phase circuit (15 amp, 230VAC), except the PDP-11/45 CPU cabinet uses 2-phase 115VAC. The average current drawn is about 12 amps per cabinet (6 amps at 230VAC). Thermal rather than magnetic breakers should be provided.

Duplex AC outlets should be provided for test equipment when maintenance tasks are performed. The duplex outlet should be located near the PDP-11 System and should be rated at 115VAC ± 15%, 15 or 20 amps. These outlets should be separately fused and switch-controlled and installed approximately 10 feet apart.

8.4 POWER CONTROL SYSTEM

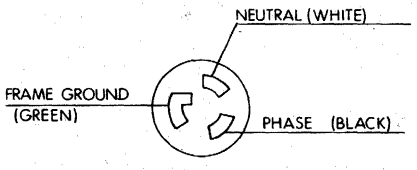
Each cabinet in a PDP-11 System has a Cabinet Power Control which is used to switch and distribute AC power to two groups of outlets located inside the cabinet, see Figure 8-6. One group provides switched AC and the other unswitched AC (for operating equipment such as magnetic disk drives that require continuous power). Use of a Cabinet Power Control also means that only one AC cord leaves the cabinet.

There are 2 pilot lights on the line side of the cabinet circuit breaker which will light whenever the AC line cord is plugged into power.

All Power Controls are connected by a 3-wire bus that carries a Power Request signal, an Emergency Shutdown signal, and Ground. There are 3 connectors on each Power Control for the 3-wire bus. A cable is supplied with each cabinet to connect the Power Control of that cabinet to the next cabinet.

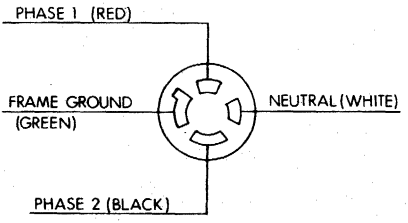
Equipment may be added to the system by connecting them to the bus in parallel at any convenient point. No terminators are required on the bus and "T" connections may be made without restriction. Interconnecting equipment into a system simply requires connecting the units together with Power Control Bus Cables and plugging AC line cords into either unswitched or switched AC. No internal wiring or jumpering is required.

(a) 115 VAC, SINGLE PHASE, 24 AMPS, (SOCKET VIEW OF FEMALE RECEPTACLE)



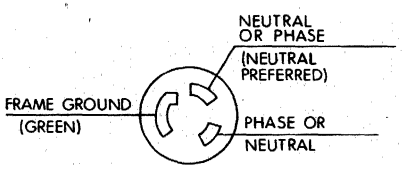
L5-30R

(b) 115 VAC, 2 PHASE, 32 AMPS (TOTAL)



L14-20R

(c) 230 VAC, SINGLE PHASE, 16 AMPS



L6-20R

		NEMA NO.	POWER CONTROL
115 VAC	Receptacle	L5-30R	861-C
single phase	Plug	L5-30P	
115 VAC	Receptacle	L14-20R	861-A
two phase	Plug	L14-20P	
230 VAC	Receptacle	L6-20R	861-B
single phase	Plug	L6-20P	

Figure 8-5 Plugs and Receptacles

In normal operation the REMOTE-OFF-LOCAL switch is set to the REMOTE position, so that the control circuit is connected to (monitors) Power Request, Line 1. One switch within the system is designated as the Master Switch and is used to control the operation of the entire system. When the Master Switch closes and connects the Power Request line to Ground, all switched AC outlets in the whole system are energized and all equipment is turned ON at the same time, (unless the Emergency Shutdown line is grounded). With the switch in the OFF position, all equipment connected to the switched AC strip will be OFF, regardless of the position of any other switches in the system. In LOCAL position, the cabinet switched AC will be ON, (unless the Emergency Shutdown line is grounded). A normally open cabinet thermostat removes switched AC power from the entire system by shorting the Emergency Shutdown line to ground whenever the temperature gets too hot, such as in case of a fire. Tables 8-3 & 8-4 summarize the operation.

In a single processor system, the console switch on the processor can be used as the Master Switch for the system as well as the device switch for the processor.

All the necessary configuring, wiring, and routing will be done by the factory in accordance with best practices. Unless there are special requirements or an unusually complex system, the customer will not have to concern himself with the details of the Power Control System.

Table 8-3 Power Control Lines

Line	Name of Line	Line State	Status of Switched AC
1	Power Request	Ground	allows turn ON
		open or +3V or greater	OFF
2	Emergency Shutdown	Ground	OFF (overrides line 1)
		open or +3V or greater	allows turn ON
3	Ground	always tied to equipment ground	

Line 2 can be used as an EMERGENCY OFF by switching it to Ground, line 3.

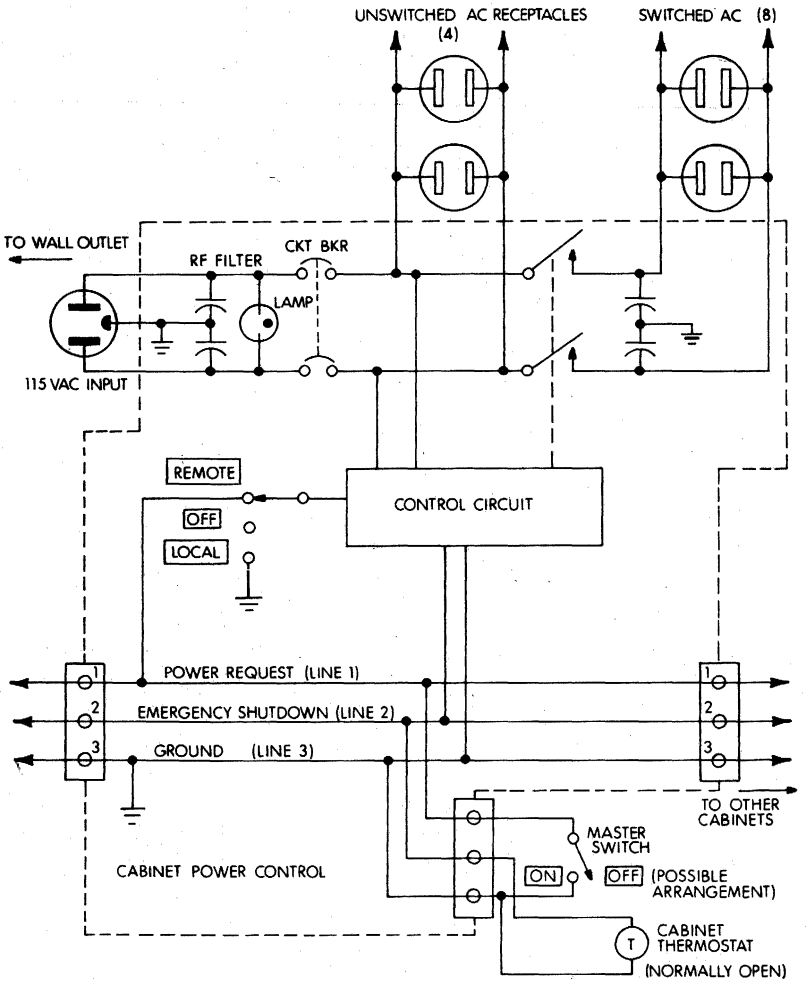


Figure 8-6 Power Control System

Table 8-4 Power Control Switch Positions

Switch Position	Function
REMOTE	Allows switched AC to be controlled by the Master Switch. To turn a system ON when all switches are in REMOTE requires at least 1 switch to actually connect lines 1 & 3 together (grounding the Power Request line).
OFF	Switched AC in the cabinet is OFF.
LOCAL	Switched AC is turned ON, if line 2 is not grounded, such as by a hot thermostat shorting and turning OFF the whole system.

CHAPTER 9

CONFIGURATION GUIDE

9.1 GENERAL

9.1.1 Configuring a System

In order to physically assemble and make the connections among the various individual units of a computer system, and to have the system operate as intended, the individual units or options must be configured. The various units such as CPU, memory, peripherals, disks, magtapes, display, printer, terminals, etc. must be mounted in a sensible and workable arrangement within the equipment cabinets. Some equipment must be close to each other for speed reasons; some equipment must be located at various points along the UNIBUS because of timing restrictions; some equipment must be located only at certain heights for ease of operator use, and some equipment must be spread out so as not to overload an individual power supply.

Standard PDP-11 systems, described in PDP-11 Price Lists, are offered and are intended to satisfy most customer requirements. These systems have been tested and documented, have been arranged in an optimum configuration, and have had all details such as UNIBUS routing, cable lengths, power requirements, etc. already determined.

9.1.2 UNIBUS

The UNIBUS acts like a transmission line for the high speed signals traveling along it. In order to preserve its electrical properties, the following points must be observed:

a) Each signal line connected to the UNIBUS must be buffered by a standard bus driver and receiver.

b) The UNIBUS is rated to drive 20 bus loads and a length of 50 feet.

c) For additional loads or length, a Bus Repeater, DB11-A, is used; thereby dividing the UNIBUS into sections. The DB11-A imposes 1 bus load on the first UNIBUS section, but then can drive an additional 19 bus loads and 50 feet.

d) Each bus section must be terminated at each end by a UNIBUS Terminator Module, M930, or its equivalent.

9.1.3 Latency

Latency is defined as the delay between the time a device requests service and the time when the service actually starts. It is essentially the response time of the system, and it is a random delay depending on what else is happening within the system. A device, with data available in a temporary buffer, could raise an interrupt flag, and then wait until the central processor initiated a service routine to read in this data. The wait time, or latency time, would depend on such things as the relative priority of the interrupt compared to the current program, the priority and occurrence of any other interrupting devices, and the overhead delays in recognizing an interrupt.

The Allowable NPR Latency is the longest time that an NPR device can be refused bus mastership before it misses the data available at that time. The NPR Latency is affected by hardware only. The Allowable BR Latency is the longest time the central processor can take to service an interrupt before the requesting device misses the data available at that time. The service time includes the execution of all higher priority interrupts and programs that may be pending plus the time spent in the interrupt subroutine. The BR Latency is mostly software dependent, in contrast to the NPR Latency.

It may be possible to recover the missed data by using a software recovery routine, such as re-reading a location from a spinning disk; sometimes as with real time data acquisition, the data will be irretrievably lost. In any case, latency problems cause a deterioration in system throughput.

One technique used to increase the Allowable Latency time is to multiple buffer the data by providing several registers for data storage. The instantaneous (as opposed to average) Allowable Latency time is increased, but the contents of all registers would eventually have to be transferred.

9.1.4 References

The following publications contain supplementary and useful information.

Computer Site Preparation Handbook
PDP-11 Processor Handbook
PDP-11 Configuration Worksheet
PDP-11 Site Preparation Worksheet
PDP-11 Price Lists (several)

Appendix E contains a summary of Equipment Specifications.

9.2 MOUNTING EQUIPMENT

System Unit
The basic mounting assembly for PDP-11 logic is the System Unit (SU), see Figure 9-1. Logic modules and cable connectors plug into the System Unit, and backplane wiring on the other side connects pins together. There are a total of 24 single module slots, but several of them are committed to UNIBUS connections. Logic modules are 8.5" long and the height can be single, double, quad, or hex (taking up 1, 2, 4, or 6 modules slots), see Figure 9-2. A System Unit is connected to other System Units only via the UNIBUS.

Mounting Box
An extension Mounting Box, BA11-ES, can hold up to 6 Systems Units plus a power supply. The Box uses 10½" of front panel space, and is supplied with tilt and lock chassis slides, see Figure 9-3.

Basic Cabinet
The basic PDP-11 cabinet, H960-CA (or H961 without end panels), has front panel capacity of six 10½" mounting spaces for Extension Mounting Boxes or peripherals, see Figure 9-4.

Cabinets With Drawers
Cabinets are available with a sliding drawer (H960-D) accommodating a

total of 9 Systems Units. The drawer is located in the bottom half of the cabinet, and uses three 10½" mounting spaces.

Other Mounting Equipment
There is expansion space in the basic CPU mounting assemblies.

The Peripheral Mounting Panel, DD11-A, is a prewired System Unit that can hold 4 small peripheral controllers (SPC). In addition to that, the DD11-B has the 2 center slots prewired for 2 DF11's. The DD11-B cannot mount in a BA11-ES.

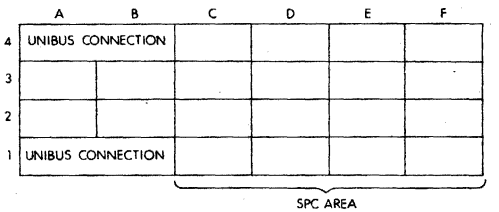


Figure 9-1 System Unit (SU) & DD11

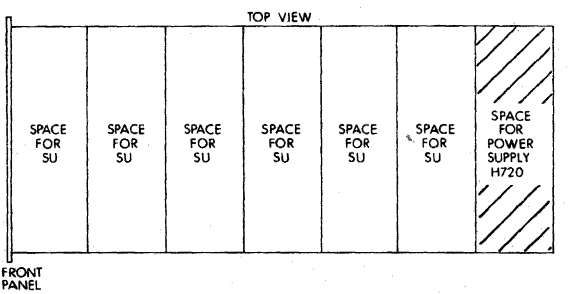


Figure 9-3 Extension Mounting Box (BA11)

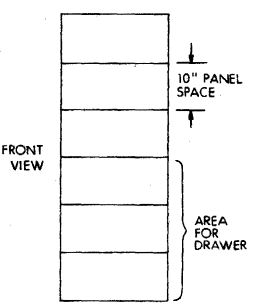


Figure 9-4 Basic Cabinet (H960 or H961)

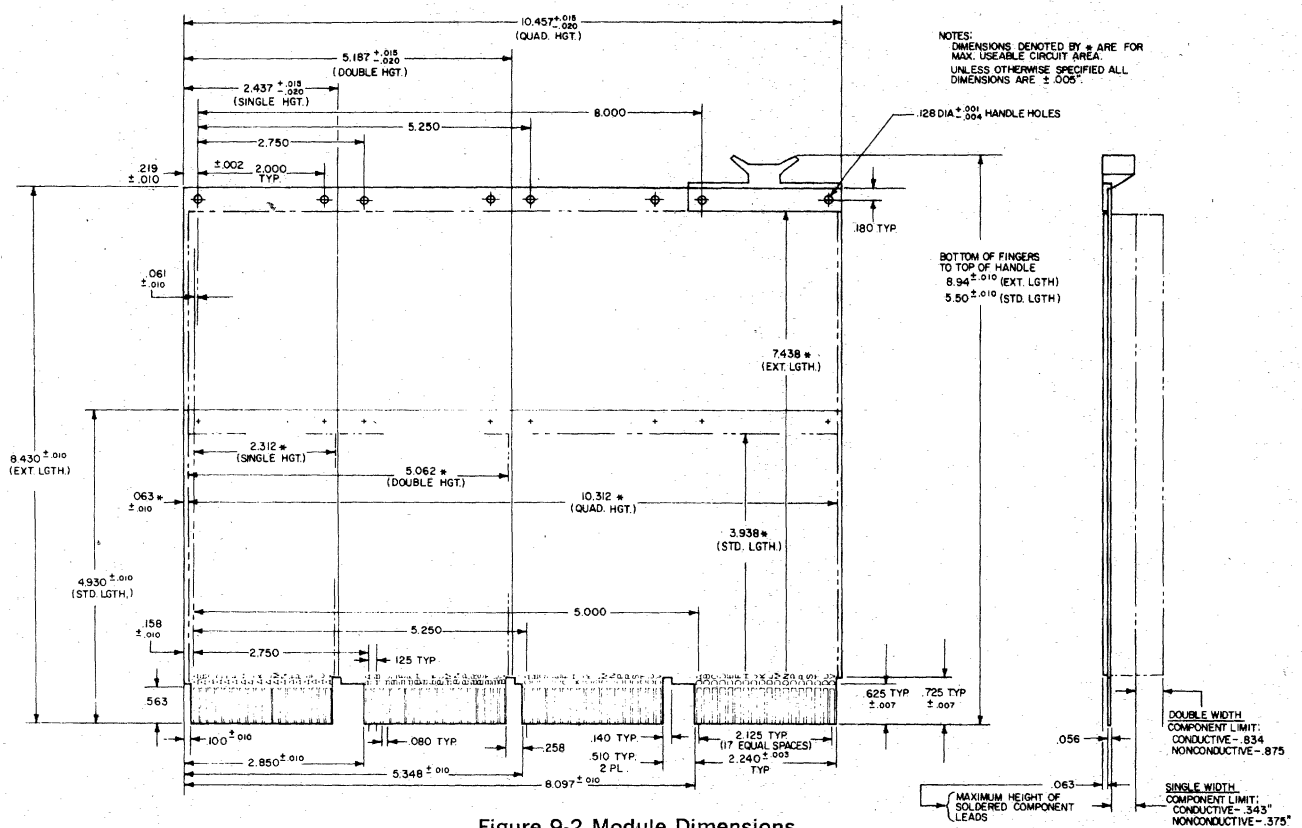


Figure 9-2 Module Dimensions

The Blank Mounting Panel BB11, is a System Unit that can be used for independent interface design. It is prewired for UNIBUS and power connections only.

Table 9-1 gives a summary of the basic mounting equipment.

Table 9-1 Summary of Basic Mounting Equipment

Option No.	Description	SU Capacity	Notes
BB11	Blank Mounting Panel	1	prewired only for UNIBUS & power
DD11	Peripheral Mounting Panel	1	prewired for logic & power
BA11-ES	Extension Mounting Box	6	power supply (H720-E or -F) not included
H960-D	Cabinet with 1 Drawer	9	power supply included
H960-CA	Basic PDP-11 Cabinet		(space for six 10½" front panels)

9.3 CONFIGURATIONS

9.3.1 Configuration Diagrams

Figure 9-5 shows the system arrangement of the major components. Prerequisites and the maximum number of peripheral units per control are indicated.

Figure 9-6 shows the preferred mounting location of peripherals, and gives weight and power dissipation for the cabinet arrangements.

9.3.2 Configuration Guidelines

a) In a cabinet, the top level (level 1) should be used only for rigidly fixed equipment. Levels 2 through 5 may be used for either rigidly fixed or slide mounted equipment. The bottom level (level 6) is reserved for power supplies and cable entry and should not be used for UNIBUS interfaces.

b) Full cabinets are reserved for some peripherals to allow for future expansion and to provide space for power supplies and internal cables.

c) Certain panel mounted equipment must be located according to the following rules:
   1. The CPU console should be at level 4.
   2. The AD01 A/D converter can be mounted at any level except 6.
   3. The DM11 distribution panel may be at level 6.
   4. The display scopes (VR01, VR14, VT01) must be at either level 2 or 3.
   5. High speed papertape equipment must be at level 3 and the controller (SPC) must be in an adjacent level of the same cabinet.

6. The RC11/RS64 disk can be at levels 2 through 5, but the second RS64 must be immediately above or below the first one.
7. BA11 Mounting Boxes can be at levels 2 through 5.

d) Additional cabinet mounted equipment is generally arranged to the left of the processor cabinet, except for special requirements.

e) Panel and cabinet mounted equipment come with all necessary power supplies already installed. However, power should not be tapped from these supplies for customer applications.

SYSTEM ARCHITECTURE

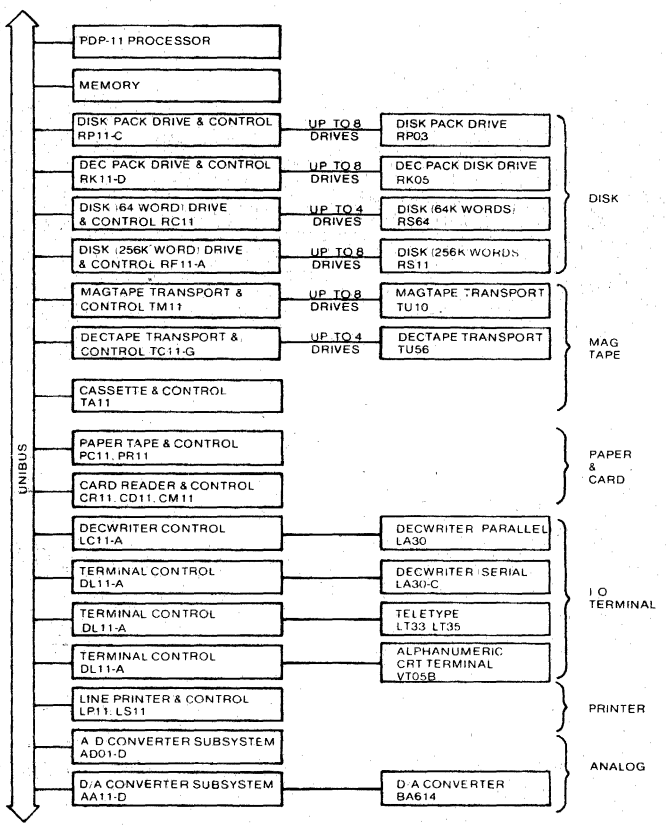


Figure 9-5 System Architecture of Major Components

In general, any device that interfaces to the UNIBUS imposes 1 bus load. The UNIBUS can handle a maximum of 20 bus loads and a total length of 50 ft. If either number is exceeded, a DB11-A UNIBUS repeater must be used.

Level	6L	5L	4L	3L	2L	1L	00
1	TU10	TM11 (tape unit)	TC11	RF11			AD01
2			DECtape #1		DECpack #1	RC11	RC11/RS64 or Display or BA11-ES
3			TU56 #2	RS11 #2	RK05 #2	Display or RS64	PC11 or TA11
4		(control unit)	TU56 #3 or BA11-ES		RK05 #3	BA11-ES or RS64	PDP-11 CPU
5			TU56 #4 or BA11-ES		RK05 #4	BA11-ES or RS64	
6				DISK #1			
Weight (lbs.)	450	510	470	600	580	470	500
Power Dis. (Watts)	1000	1030	1900	1050	800		

NOTES:

For referencing the location of contiguous cabinets, the CPU is considered to be in location 00. 3L means 3 cabinets to the left.

A PDP-11/10 CPU would be located at level 4,
PDP-11/40 CPU levels 4 & 5,
PDP-11/45 CPU levels 4, 5, & 6.

Figure 9-6 Preferred Locations of Peripherals

APPENDIX A

UNIBUS ADDRESSES

A.1 INTERRUPT & TRAP VECTORS

000	(reserved)
004	Time Out & other errors
010	Illegal & reserved instructions
014	BPT, breakpoint trap
020	IOT, input/output trap
024	Power Fail
030	EMT, emulator trap
034	TRAP instruction
040	System software
044	System software
050	System software
054	System software
060	Console Terminal, keyboard/reader
064	Console Terminal, printer/punch
070	PC11, paper tape reader
074	PC11, paper tape punch
100	KW11-L, line clock
104	KW11-P, programmable clock
110	
114	Memory parity error
120	XY Plotter
124	DR11-B DMA interface; (DA11-B)
130	ADO1, A/D subsystem
134	AFC11, analog subsystem
140	AA11, display
144	AA11, light pen
150	
154	
160	
164	
170	User reserved
174	User reserved
200	LP11/LS11, line printer
204	RF11, disk
210	RC11, disk
214	TC11, DECtape
220	RK11, disk
224	TM11, magnetic tape
230	CD11/CM11/CR11, card reader

234 UDC11, digital control subsystem
240 PIRQ, Program Interrupt Request (11/45)
244 Floating Point Error
250 Memory Segmentation
254 RP11, disk
260 TA11, cassette
264

270 User reserved
274 User reserved

300 (start of floating vectors)

A.2 FLOATING VECTORS

There is a floating vector convention used for communications (and other) devices that interface with the PDP-11. These vector addresses are assigned in order starting at 300 and proceeding upwards to 777. The following Table shows the assigned sequence. It can be seen that the first vector address, 300, is assigned to the first DC11 in the system. If another DC11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all the DC11's (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL11 or DP11 or DM11, etc.), then to the other devices in accordance with the priority ranking.

Priority Ranking for Floating Vectors

(starting at 300 and proceeding upwards)

Rank	Device	Vector Size (in octal)	Max No.
1	DC11	$(10)_8$	32
2	KL11, DL11-A, DL11-C	10	16
3	DP11	10	32
4	DM11-A	10	16
5	DN11	4	16
6	DM11-BB	4	16
7	DR11-A	10*	32
8	DR11-C	10*	32
9	PA611 Reader	4*	16
10	PA611 Punch	4*	16
11	DT11	10*	8
12	DX11	10*	4
13	DL11-C, DL11-D, DL11-E	10	31
14	DJ11	10	16
15	DH11	10	16
16	GT40	10	1
17	LPS11	30*	1
18	VT20	20	2

*—The first vector for the first device of this type must always be on a $(10)_8$ boundary.

A.3 FLOATING ADDRESSES

There is a floating address convention used for communications (and other) devices interfacing with the PDP-11. These addresses are assigned in order starting at 760 010 and proceeding upwards to 763 776.

Floating addresses are assigned in the following sequence:

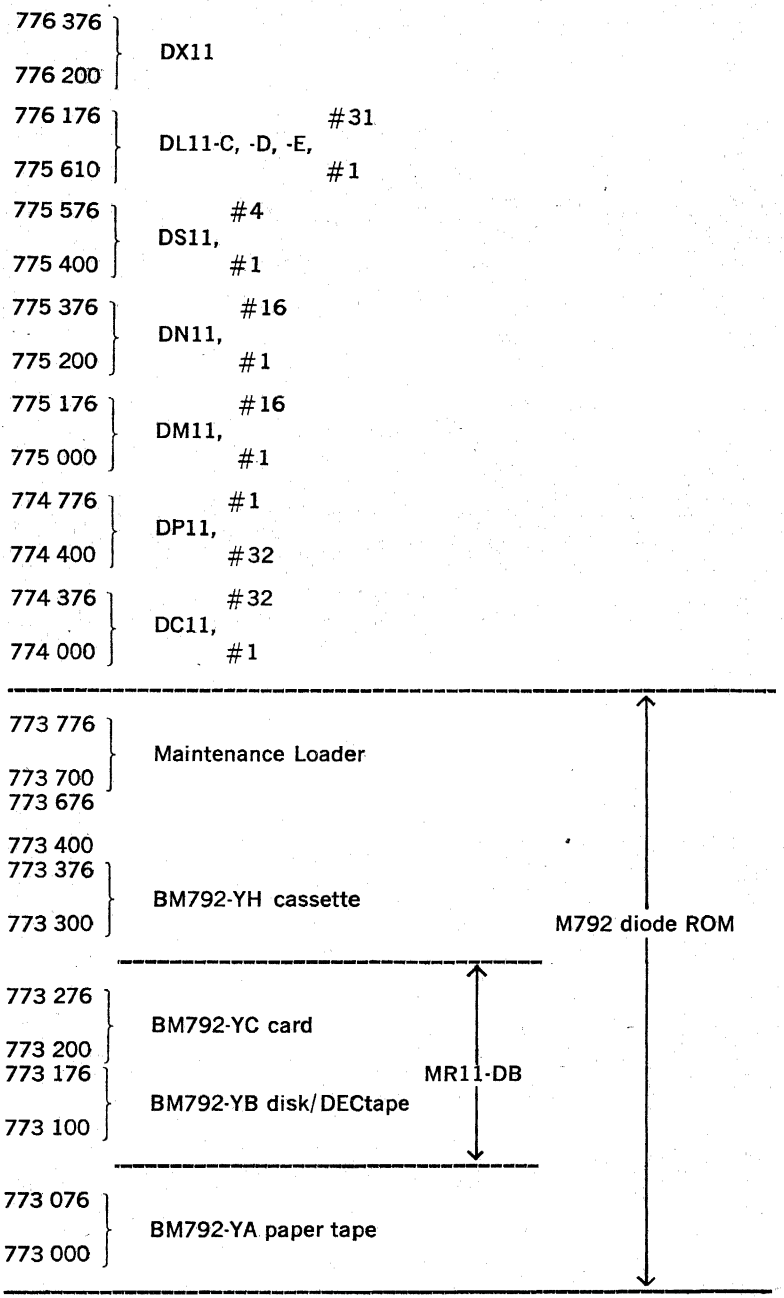
Rank	Device	First Address (if only floating address device in the system)
1	DJ11	760 010
2	DH11	760 020
3	GT40	760 040
4	LPS11	760 100
5	VT20	760 120

A.4 DEVICE ADDRESSES

777 776	Processor Status word (PS)	
777 774	Stack Limit	
777 772	Program Interrupt Request (PIRQ)	
777 716 ⎫	CPU registers	
777 710 ⎭		
777 707		R7 (PC)
777 706		R6 (SP)
777 705		R5
777 704	General registers,	R4
777 703		R3
777 702		R2
777 701		R1
777 700		R0
777 676 ⎫	Memory Management	
777 600 ⎭		
777 576		(SR2)
777 574	Memory Mgt status regs,	(SR1)
777 572		(SR0)
777 570	Console Switch & Display Register	
777 566		printer/punch data
777 564	Console Terminal,	printer/punch status
777 562		keyboard/reader data
777 560		keyboard/reader status
777 556		punch data (PPB)
777 554	PC11/PR11,	punch status (PPS)
777 552		reader data (PRB)
777 550		reader status (PRS)

777 546	KW11-L, clock status (LKS)	
777 516		printer data
777 514	LP11/LS11/LV11,	printer status
777 512		
777 510		
777 506		
777 504		
777 502	TA11,	cassette data (TADB)
777 500		cassette status (TACS)
777 476		look ahead (ADS)
777 474		maintenance (MA)
777 472		disk data (DBR)
777 470	RF11,	adrs ext error (DAE)
777 466		disk address (DAR)
777 464		current mem adrs (CMA)
777 462		word count (WC)
777 460		disk status (DCS)
777 456		disk data (RCDB)
777 454		maintenance (RCMN)
777 452		current address (RCCA)
777 450	RC11,	word count (RCWC)
777 446		disk status (RCCS)
777 444		error status (RCER)
777 442		disk address (RCDA)
777 440		look ahead (RCLA)
777 436		#8
777 434		#7
777 432		#6
777 430	DT11, bus switch	#5
777 426		#4
777 424		#3
777 422		#2
777 420		#1
777 416		disk data (RKDB)
777 414		maintenance
777 412		disk address (RKDA)
777 410	RK11,	bus address (RKBA)
777 406		word count (RKWC)
777 404		disk status (RKCS)
777 402		error (RKER)
777 400		drive status (RKCS)
777 356		
777 354		
777 352		
777 350		DECtape data (TCDT)
777 346	TC11,	bus address (TCBA)
777 344		word count (TCWC)
777 342		command (TCCM)
777 340		DECtape status (TCST)

777 336	KE11-A, EAE #2	
777 320		
777 316		arithmetic shift
777 314		logical shift
777 312		normalize
777 310	KE11-A, EAE #1,	step count/status register
777 306		multiply
777 304		multiplier quotient
777 302		accumulator
777 300		divide
777 166		
777 164		card data (CRB2), compressed
777 162	CR11/CM11,	card data (CRB1)
777 160		card status (CRS)
776 776		
776 774		
776 772	AD01,	A/D data (ADDB)
776 770		A/D status (ADCS)
776 766		register 4 (DAC4)
776 764		register 3 (DAC3)
776 762		register 2 (DAC2)
776 760	AA11 #1,	register 1 (DAC1)
776 756		D/A status (CSR)
776 754		
776 752		
776 750		
776 736		silo memory (SILO)
776 734		sel unit cyl adrs (SUCA)
776 732		maintenance 3 (RPM3)
776 730		maintenance 2 (RPM2)
776 726		maintenance 1 (RPM1)
776 724	RP11,	disk address (RPDA)
776 722		cyclinder address (RPCA)
776 720		bus address (RPBA)
776 716		word count (RPWC)
776 714		disk status (RPCS)
776 712		error (RPER)
776 710		disk status (RPDS)
776 676	#16	
	DL11-A, -B,	
776 500	#1	
776 476	#5	
	AA11,	
776 400	#2	


776 376
DX11
776 200
776 176
#31
DL11-C, -D, -E,
775 610
#1
775 576
#4
DS11,
775 400
#1
775 376
#16
DN11,
775 200
#1
775 176
#16
DM11,
775 000
#1
774 776
#1
DP11,
774 400
#32
774 376
#32
DC11,
774 000
#1
773 776
Maintenance Loader
773 700
773 676
773 400
773 376
BM792-YH cassette
773 300
M792 diode ROM
773 276
BM792-YC card
773 200
773 176
MR11-DB
BM792-YB disk/DECtape
773 100
773 076
BM792-YA paper tape
773 000

772 776		
		PA611 typeset punch
772 700		
772 676		
		PA611 typeset reader
772 600		
772 576		maintenance (AFMR)
772 574	AFC11,	MX channel/gain (AFCG)
772 572		flying cap data (AFBR)
772 570		flying cap status (AFCS)
772 556		
		XY11 plotter
772 550		
772 546		
772 544		counter
772 542	KW11-P,	count set
772 540		clock status
772 536		
772 534		
772 532		read lines (MTRD)
772 530		tape data (MTD)
772 526	TM11,	memory address (MTCMA)
772 524		byte record counter (MTBRC)
772 522		command (MTC)
772 520		tape status (MTS)
772 516		Memory Mgt status reg (SR3)
772 512		CSR
772 510		EADRS1,2
772 506	OST	ADRS2
772 504		ADRS1
772 502		MASK2
772 500		MASK1
772 476		
		DR11-B #4
772 470		
772 466		card data (CDDB)
772 464	CD11,	current address (CDBA)
772 462		column count (CDCC)
772 460		card status (CDST)
772 456		
		DR11-B #3
772 450		
772 436		
		DR11-B #2
772 430		

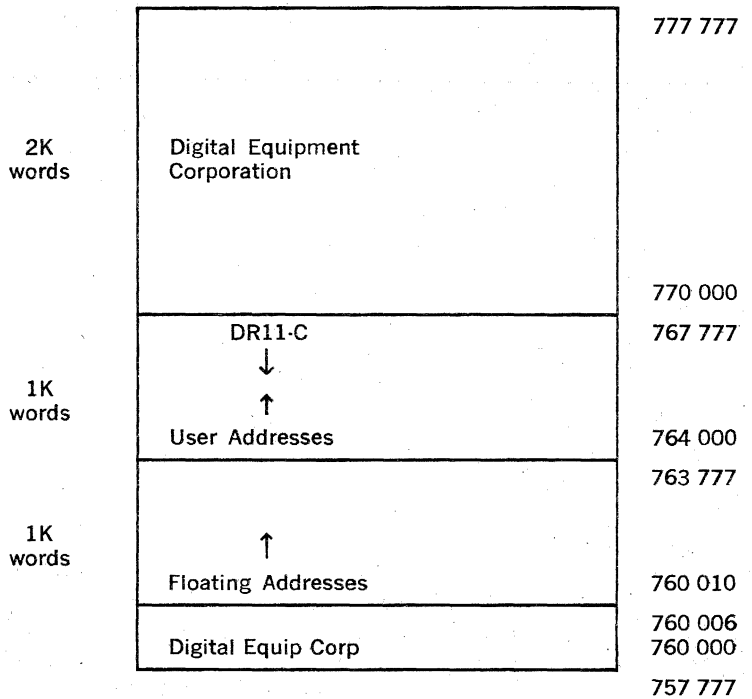
772 416		data (DRDB)
772 414	DR11-B #1,	status (DRST)
772 412		bus address (DRBA)
772 410		word count (DRWC)
772 376		
	Memory Management	
772 200		
772 136		
	Memory Parity	
772 110		
771 776		status (UDCS)
771 774	UDC11,	scan (UDSR)
771 772		
771 770		
771 776		
	UDC functional I/O modules	
771 000		
770 776	#8	
	KG11,	
770 700	#1	
770 676	#16	
	DM11-BB,	
770 500	#1	
767 776		
767 774		input buffer
767 772	DR11-C #1,	output buffer
767 770		status
767 766		
	DR11-C #2	
767 760		
767 756		
	DR11-C #3	
767 750		
764 000	(start here and assign upwards to 767 776)	
763 776	(top of floating addresses)	
760 010	(start here and assign upwards to 763 776)	

User Addresses

Floating Addresses

760 006
760 000 } (diagnostics)

A.5 ADDRESS MAP



APPENDIX B

MISCELLANEOUS TABLES AND DATA

SLOTS A1 AND B1 (A4 AND B4) ARE WIRED AS SHOWN IN TABLES B–1 AND B–2.

TABLE B–1 UNIBUS PIN ASSIGNMENTS (BY PIN NUMBERS)

PIN	SIGNAL	PIN	SIGNAL
AA1	INIT L	BA1	BG 6 H
AA2	POWER(+ 5V)	BA2	POWER(+ 5V)
AB1	INTR L	BB1	BG 5 H
AB2	GROUND	BB2	GROUND
AC1	DOO L	BC1	BR 5 L
AC2	GROUND	BC2	GROUND
AD1	DO2 L	BD1	GROUND
AD2	DOI L	BD2	BR 4 L
AE1	DO4 L	BE1	GROUND
AE2	DO3 L	BE2	BG 4 H
AF1	DO6 L	BF1	ACLO L
AF2	DO5 L	BF2	DCLO L
AH1	DO8 L	BH1	AO1 L
AH2	DO7 L	BH2	AOO L
AJ1	D10 L	BJ1	AO3 L
AJ2	DO9 L	BJ2	AO2 L
AK1	D12 L	BK1	AO5 L
AK2	D11 L	BK2	AO4 L
AL1	D14 L	BL1	AO7 L
AL2	D13 L	BL2	AO6 L
AM1	PA L	BM1	AO9 L
AM2	D15 L	BM2	AO8 L
AN1	GROUND	BN1	A11 L
AN2	PB L	BN2	A10 L
AP1	GROUND	BP1	A13 L
AP2	BBSY L	BP2	A12 L
AR1	GROUND	BR1	A15 L
AR2	SACK L	BR2	A14 L
AS1	GROUND	BS1	A17 L
AS2	NPR L	BS2	A16 L
AT1	GROUND	BT1	GROUND
AT2	BR 7 L	BT2	C1 L
AU1	NPG H	BU1	SSYN L
AU2	BR 6 L	BU2	CO L
AV1	BG 7 H	BV1	MSYN L
AV2	GROUND	BV2	GROUND

TABLE B–2 UNIBUS PIN ASSIGNMENTS (BY SIGNAL NAME)

SIGNAL	PIN	SIGNAL	PIN
AOO L	BH2	DO6 L	AF1
AO1 L	BH1	DO7 L	AH2
AO2 L	BJ2	DO8 L	AH1
AO3 L	BJ1	DO9 L	AJ2
AO4 L	BK2	D10 L	AJ1
AO5 L	BK1	D11 L	AK2
AO6 L	BL2	D12 L	AK1
AO7 L	BL1	D13 L	AL2
AO8 L	BM2	D14 L	AL1
AO9 L	BM1	D15 L	AM2
A10 L	BN2	GROUND	AB2
A11 L	BN1	GROUND	AC2
A12 L	BP2	GROUND	AN1
A13 L	BP1	GROUND	AP1
A14 L	BR2	GROUND	AR1
A15 L	BR1	GROUND	AS1
A16 L	BS2	GROUND	AT1
A17 L	BS1	GROUND	AV2
ACLO L	BF1	GROUND	BB2
BBSY L	AP2	GROUND	BC2
BG4 H	BE2	GROUND	BD1
BG5 H	BB1	GROUND	BE1
BG6 H	BA1	GROUND	BT1
BG7 H	AV1	GROUND	BV2
BR4 L	BD2	INIT L	AA1
BR5 L	BC1	INTR L	AB1
BR6 L	AU2	MSYN L	BV1
BR7 L	AT2	NPG H	AU1
CO L	BU2	NPR L	AS2
C1 L	BT2	PA L	AM1
DOO L	AC1	PB L	AN2
DO1 L	AD2	+ 5V*	AA2
DO2 L	AD1	+ 5V*	BA2
DO3 L	AE2	SACK L	AR2
DO4 L	AE1	DCLO L	BF2
DO5 L	AF2	SSYN L	BU1

* + 5V IS WIRED TO THESE PINS TO SUPPLY POWER TO THE BUS TERMINATOR ONLY.

+ 5V SHOULD NEVER BE CONNECTED VIA THE UNIBUS BETWEEN SYSTEM UNITS.

TABLE B–3 BB11 POWER PIN ASSIGNMENTS

PIN	POWER
A1	–15V
A2	+5V
B1	–15V
B2	–15V
C1	–15V
C2	GND
D1	–15V
D2	GND
E1	–15V
E2	GND
F1	–15V
F2	GND
H1	–15V
H2	+5V
J1	–15V
J2	+5V
K1	–15V
K2	+5V
L1	–15V
L2	+5V
M1	–15V
M2	+5V
N1	GND
N2	–25V
P1	GND
P2	LTC L
R1	GND
R2	ACLO L
S1	GND
S2	DCLO L
T1	GND
T2	+8V
U1	GND
U2	+8V
V1	GND
V2	+8V

NOTE

POWER IS IN MODULE SLOT A3 OF ALL SYSTEM UNITS MOUNTED IN BA11 MOUNTING BOXES EQUIPPED WITH H720 POWER SUPPLIES.

B.4 ASCII CODE

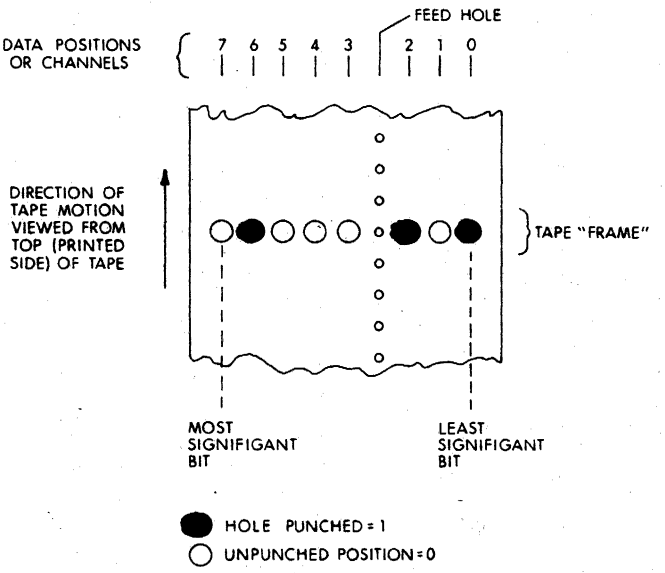
7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	`
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	—	177	DEL

To convert to the modified ASCII code used by the LT33:

8-Bit Teletype Code = (7-Bit ASCII Code) + $(200)_8$

B.5 PAPER TAPE FORMAT



NOTE:
FRAME SHOWN IS PUNCHED WITH OCTAL CODE 105

Paper-Tape Format

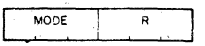
B.6 PUNCHED CARD FORMAT

Card Code		Compressed Code (octal)	Character	Card Code		Compressed Code (octal)	Character
Zone	Number			Zone	Number		
—	—	000	Blank	11	0	—	Invalid
12	8-2	212	¢	11	1	101	J
12	8-3	213	.	11	2	102	K
12	8-4	214	)	11	3	103	L
12	8-5	215	]	11	4	104	M
12	8-6	216	<	11	5	105	N
12	8-7	217	←	11	6	106	O
12	—	200	+	11	7	107	P
11	8-2	112	!	11	8	110	Q
11	8-3	113	$	11	9	120	R
11	8-4	114	*	0	8-2	012	;
11	8-5	115	[	0	2	002	S
11	8-6	116	>	0	3	003	T
11	8-7	117	&	0	4	004	U
11	—	100	—	0	5	005	V
0	1	051	/	0	6	006	W
0	8-3	053	,	0	7	007	X
0	8-4	054	(	0	8	010	Y
0	8-5	055	"	0	9	020	Z
0	8-6	056	#	—	0	040	0
0	8-7	057	%	—	1	001	1
—	8-2	—	Invalid	—	2	002	2
—	8-3	013	=	—	3	003	3
—	8-4	014	@	—	4	004	4
—	8-5	015	↑	—	5	005	5
—	8-6	016	,	—	6	006	6
—	8-7	017	\	—	7	007	7
12	0	—	Invalid	—	8	010	8
12	1	201	A	—	9	020	9
12	2	202	B				
12	3	203	C				
12	4	204	D				
12	5	205	E				
12	6	206	F				
12	7	207	G				
12	8	210	H				
12	9	220	I				

APPENDIX C

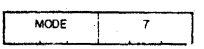
SUMMARY OF PDP11 INSTRUCTIONS

GENERAL REGISTER ADDRESSING



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2 = %2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R)+(1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R)+2
4	auto-decrement	−(R)	(R) − (1 or 2); (R) is adrs
5	auto-decr deferred	@−(R)	(R) − 2; (R) is adrs of adrs
6	index	X(R)	(R)+X is adrs
7	index deferred	@X(R)	(R)+X is adrs of adrs

PROGRAM COUNTER ADDRESSING



Reg = 7

2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs +4+X is adrs
7	relative deferred	@A	instr adrs +4+X is adrs of adrs

LEGEND

Op Codes

■ = 0 for word/1 for byte
SS = source field (6 bits)
DD = destination field (6 bits)
R = gen register (3 bits), 0 to 7
XXX = offset (8 bits), +127 to −128
N = number (3 bits)
NN = number (6 bits)

Operations

( ) = contents of
s = contents of source
d = contents of destination
r = contents of register
← = becomes
X = relative address
% = register definition

Boolaen

∧ = AND
∨ = inclusive OR
∨ = exclusive OR
~ = NOT

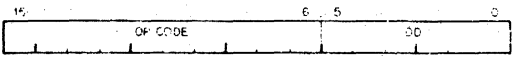
Condition Codes

* = conditionally set or cleared
— = not affected
0 = cleared
1 = set

NOTE:

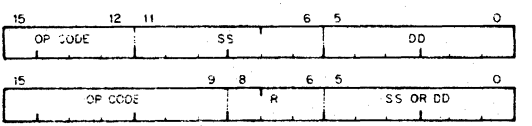
▲ = Applies to the 11/35, 11/40, & 11/45 computers
● = Applies to the 11/45 computer

SINGLE OPERAND: OPR dst



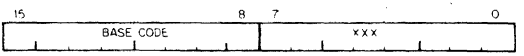
Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■050DD	clear	0	0	1	0	0
COM(B)	■051DD	complement (1's)	~d	*	*	0	1
INC(B)	■052DD	increment	d + 1	*	*	*	_
DEC(B)	■053DD	decrement	d − 1	*	*	*	_
NEG(B)	■054DD	negate (2's compl)	−d	*	*	*	*
TST(B)	■057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■060DD	rotate right		*	*	*	*
ROL(B)	■061DD	rotate left		*	*	*	*
ASR(B)	■062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	*	0
Multiple Precision							
ADC(B)	■055DD	add carry	d + C	*	*	*	*
SBC(B)	■056DD	subtract carry	d − C	*	*	*	*
▲ SXT	0067DD	sign extend	0 or −1	_	*	*	_

DOUBLE OPERAND: OPR src,dst OPR scr,R or OPR R,dst



Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■1SSDD	move	d ← s	*	*	0	_
CMP(B)	■2SSDD	compare	s − d	*	*	*	*
ADD	06SSDD	add	d ← s + d	*	*	*	*
SUB	16SSDD	subtract	d ← d − s	*	*	*	*
Logical							
BIT(B)	■3SSDD	bit test (AND)	s ∧ d	*	*	0	_
BIC(B)	■4SSDD	bit clear	d ← (~s) ∧ d	*	*	0	_
BIS(B)	■5SSDD	bit set (OR)	d ← s ∨ d	*	*	0	_
▲ **Register**							
MUL	070RSS	multiply	r ← r x s	*	*	0	*
DIV	071RSS	divide	r ← r/s	*	*	*	*
ASH	072RSS	shift arithmetically		*	*	*	*
ASHC	073RSS	arith shift combined		*	*	*	*
XOR	074RDD	exclusive OR	d ← r ∨ d	*	*	0	_

BRANCH B _ _ location



If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)

Op Code = Base Code + XXX

adrs of br instr +2

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	$\neq 0$	$Z = 0$
BEQ	001400	br if equal (to 0)	$= 0$	$Z = 1$
BPL	100000	branch if plus	$+$	$N = 0$
BMI	100400	branch if minus	$-$	$N = 1$
BVC	102000	br if overflow is clear		$V = 0$
BVS	102400	br if overflow is set		$V = 1$
BCC	103000	br if carry is clear		$C = 0$
BCS	103400	br if carry is set		$C = 1$
Signed Conditional Branches				
BGE	002000	br if greater or eq (to 0)	$\geqslant 0$	$N \veebar V = 0$
BLT	002400	br if less than (0)	< 0	$N \veebar V = 1$
BGT	003000	br if greater than (0)	> 0	$Z \vee (N \veebar V) = 0$
BLE	003400	br if less or equal (to 0)	$\leqslant 0$	$Z \vee (N \veebar V) = 1$
Unsigned Conditional Branches				
BHI	101000	branch if higher	$>$	$C \vee Z = 0$
BLOS	101400	branch if lower or same	$\leqslant$	$C \vee Z = 1$
BHIS	103000	branch if higher or same	$\geqslant$	$C = 0$
BLO	103400	branch if lower	$<$	$C = 1$

JUMP & SUBROUTINE:

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
▲MARK	0064NN	mark	aid in subr return
▲SOB	077RNN	subtract 1 & br (if $\neq 0$)	(R) − 1, then if (R) $\neq$ 0: PC ← Updated PC − (2 x NN)

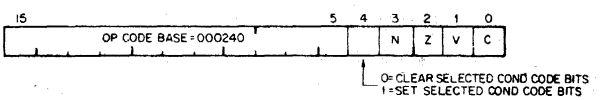
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
▲RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)
● SPL	00023N	set priority level (to N)
▲ MFPI	0065SS	move from previous instr space
▲ MTPI	0066DD	move to previous instr space
● MFPD	1065SS	move from previous data space
● MTPD	1066DD	move to previous data space

CONDITION CODE OPERATORS:



Mnemonic	Op Code	Instruction	N Z V C
CLC	000241	clear C	_ _ _ 0
CLV	000242	clear V	_ _ 0 _
CLZ	000244	clear Z	_ 0 _ _
CLN	000250	clear N	0 _ _ _
CCC	000257	clear all cc bits	0 0 0 0
SEC	000261	set C	_ _ _ 1
SEV	000262	set V	_ _ 1 _
SEZ	000264	set Z	_ 1 _ _
SEN	000270	set N	1 _ _ _
SCC	000277	set all cc bits	1 1 1 1

PDP-11 ASSEMBLY LANGUAGE

PAL-11 ASSEMBLY LANGUAGE
The Program Assembly Language for the PDP-11, called PAL-11, allows the writing of programs using letters, numbers, and symbols instead of only octal or binary numbers.

D.1 Character Set
A symbolic program is composed of letters, numbers, expressions, symbolic instructions, directions for the assembler, argument separators, and line terminators written using the following ASCII characters. (ASCII stands for American Standard Code for Information Interchange.)

1. The letters A through Z.
2. The numbers 0 through 9.
3. The characters . and $ (reserved for system software).
4. The separation or terminating symbols:
   . : = % @ ( ) , ; ' " + − & !
   carriage return tab space line feed form feed

D.2 Statements
A program is composed of a sequence of statements, where each statement is on a single line. The statement is terminated by a carriage return character and must be immediately followed by either a line feed or form feed character.

A statement may be composed of up to four fields which are identified in their order of appearance and by specified terminating characters as explained below. The four fields are:

Label Operator Operand Comment

The label and comment fields are optional. The operator and operand fields are interdependent; either may be omitted depending upon the contents of the other.

Label
A label is a user-defined symbol which is assigned the value of the current location counter. It is a symbolic means of referring to a specific location within a program. If present, a label always occurs first in a statement and must be terminated by a colon. For example, if the current location is 100, the statement

```
ABCD:    MOV A, B
```

will assign the value 100 to the label ABCD so that subsequent reference to ABCD will be to location 100. More than one label may appear within a single label field; each label within the field will have the same value. For example, if the current location is 100, multiple labels in the statement

```
ABC:  NOW:  PLACE:  MOV, A, B
```

will equate each of the three labels ABC, NOW, and PLACE with the value 100.

Operator

An operator follows the label field in a statement, and may be an instruction mnemonic or an assembler directive. When it is an instruction mnemonic, it specifies what action is to be performed on any operand(s) which follow it. When it is an assembler directive, it specifies a certain function or action to be performed during assembly.

The operator may be preceded only by one or more labels and may be followed by one or more operands and/or a comment. An operator is legally terminated by a space, tab, or any of the following characters.

```
# + - @ ( " ' % ! & , ;
line feed      form feed      carriage return
```

Consider the following examples:

```
MOV    A, B     ; (TAB) terminates operator MOV
MOV  @A, B      ;@ terminates operator MOV
```

When the operator stands alone without an operand or comment, it is terminated by a carriage return followed by a line feed or form feed character.

Operand

An operand is that part of a statement which is operated on by the operator, an instruction mnemonic, or assembler directive. Operands may be symbols, expressions, or numbers. When multiple operands appear within a statement, each is separated from the next by a comma. The operand field is terminated by a semicolon when followed by a comment, or by a carriage return followed by a line feed or form feed character when the operand ends the statement. For example:

```
LABEL:    MOV GEORGE,BOB    ;THIS IS A COMMENT
```

where the space between MOV and GEORGE terminated the operator field and began the operand field; the comma separated the operands GEORGE and BOB; the semicolon terminated the operand field and began the comment.

Comments

The comment field is optional and may contain any character previously mentioned except null, rubout, carriage return, line feed or form feed. All other characters, even those with special significance are ignored by the Assembler when used in the comment field.

The comment field may be preceded by none, any, or all of the other three fields. It must begin with the semicolon and end with a carriage return followed by a line feed or form feed character. For example:

```
LABEL:    CLR HERE    ;THIS IS A $1.00 COMMENT
```

Comments do not affect assembly processing or program execution, but they are useful in program listings for later analysis, checkout or documentation purposes.

Format Control
The format is controlled by the space and tab characters. They have no effect on the assembling process of the source program unless they are embedded within a symbol, number, or ASCII text; or are used as the operator field terminator. Thus, they can be used to provide a neat, readable program. A statement can be written

```
LABEL: MOV (SP)+,TAG;POP VALUE OFF STACK
```

or, using formatting characters it can be written

```
LABEL:   MOV (SP)+, TAG   ;POP VALUE OFF STACK
```

which is much easier to read.

D.3 Symbols
There are two types of symbols, permanent and user-defined. Both are stored in the Assembler's symbol table. Initially, the symbol table contains the permanent symbols, but as the source program is assembled, user defined symbols are added to the table.

Permanent Symbols
Permanent symbols consist of the instruction mnemonics and assembler directives. These symbols are a permanent part of the Assembler's symbol table and need not be defined before being used in the source program.

User-Defined Symbols
User-defined symbols are those defined as labels or by direct assignment. These symbols are added to the symbol table as they are encountered during the assembly. They can be composed of alphanumeric characters, dollar signs, and periods only; again, dollar signs and periods are reserved for use by the system software. Any other character is illegal. The following rules also apply to user-defined symbols:

1. The first character must not be a number.

2. Each symbol must be unique within the first six characters.

3. A symbol may be written with more than six legal characters but the seventh and subsequent characters are only checked for legality, and are not otherwise recognized by the Assembler.

4. Spaces and tabs must not be embedded within a symbol.

A user-defined symbol may duplicate a permanent symbol. The value associated with a permanent symbol that is also user-defined depends upon its use:

1. A permanent symbol encountered in the operator field is associated with its corresponding machine op-code.

2. If a permanent symbol in the operand field is also user-defined, its user-defined value is associated with the symbol. If the symbol is not found to be user-defined, then the corresponding machine op-code value is associated with the symbol.

Direct Assignment
A direct assignment statement associates a symbol with a value. When a direct assignment statement defines a symbol for the first time, that symbol is entered into the Assembler's symbol table and the specified value associated with it. A symbol may be redefined by assigning a new value to a previously defined symbol. The newly assigned value will replace the previous value assigned to the symbol.

The general format for a direct assignment statement is

symbol = expression

The following conventions apply:

1. An equal sign (=) must separate the symbol from the expression defining the symbol.
2. A direct assignment statement may be preceded by a label and may be followed by a comment.
3. Only one symbol can be defined by any one direct assignment statement.
4. Only one level of forward referencing is allowed.

Examples:

```
    A = 1       ;THE SYMBOL A IS EQUATED WITH THE VALUE 1
    B = A-1     ;THE SYMBOL B IS EQUATED WITH THE EXPRES-
                ;SION'S VALUE
C:  D = 3       ;THE SYMBOL D IS EQUATED WITH 3.
```

Register Symbols
The eight general registers of the PDP-11 are numbered 0 through 7. These registers may be referenced by use of a register symbol, that is, a symbolic name for a register.

Registers are defined by use of the percentage sign (%).

```
R0=%0           ;DEFINE R0 AS REGISTER 0
R3=%3           ;DEFINE R3 AS REGISTER 3
```

It is important to note that all register symbols must be defined before they are referenced.
The statement,

```
CLR %6
```

will clear register 6 while the statement,

```
CLR 6
```

will clear the word at memory address 6.

D.4 Expressions
Arithmetic and logical operators may be used to form expressions. A term of an expression may be a permanent or user-defined symbol, a number, data, or the present value of the assembly location counter represented by the period. Expressions are evaluated from left to right. Parenthetical grouping is not allowed.

Numbers
The Assembler accepts both octal and decimal numbers. Octal numbers consist of the digits 0 through 7 only. Decimal numbers consist of the digits 0 through 9 followed by a decimal point. Negative numbers may be expressed as a number preceded by a minus sign rather than in a two's complement form. Positive numbers may be preceded by a plus sign although this is not required.

If a number is too large to fit into 16 bits, the number is truncated from the left.

ASCII Conversion
When preceded by an apostrophe, any ASCII character (except null, rubout, carriage return, line feed, or form feed) is assigned the 7-bit ASCII value of the character. For example,

'A

is assigned the value 101_8.

When preceded by a quotation mark, two ASCII characters (not including null, rubout, carriage return, line feed, or form feed) are assigned the 7-bit ASCII values of each of the characters to be used. Each 7-bit value is stored in an 8-bit byte and the bytes are combined to form a word. For example, "AB will store the ASCII value of A in the low-order (even) byte and the value of B in the high-order (odd) byte, see Figure D-1.

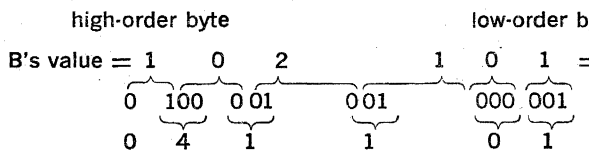


Figure D-1 ASCII Representation ("AB = 041 101)

D.5 Assembly Location Counter
The period (.) is the symbol for the assembly location counter. Note difference of Program Counter. (. ≠ PC.) When used in the operand field of an instruction, it represents the address of the first word of the instruction. When used in the operand field of an assembler directive, it represents the address of the current byte or word.

```
A: MOV #.,R0    ;.REFERS TO LOCATION A,I.E.,
                ;THE ADDRESS OF THE MOV INSTRUCTION
```

At the beginning of the assembly, the Assembler clears the location counter. Normally, consecutive memory locations are assigned to each byte of object data generated. However, the location where the object data is stored may be changed by a direct assignment altering the location counter.

D.6 Addressing
The Program Counter (register 7 of the eight general registers) always

contains the address of the next word to be fetched; i.e., the address of the next instruction to be executed, or the second or third word of the current instruction.

In order to understand how the address modes operate and how they assemble, the action of the Program Counter must be understood. The key rule is:

> **Whenever the processor implicitly uses the Program Counter (PC) to fetch a word from memory, the Program Counter is automatically incremented by two after the fetch.**

That is, when an instruction is fetched, the PC is incremented by two, so that it is pointing to the next word in memory; and, if an instruction uses indexing, the processor uses the Program Counter to fetch the base from memory. Hence, using the rule above, the PC increments by two, and now points to the next word.

D.7 Assembler Directives

Assembler directives (sometimes called pseudo-ops) direct the assembly process and may generate data. They are always preceded by a period(.). The assembler directive occupies the operator field. Only one directive may be placed in any one statement. One or more operands may occupy the operand field or it may be void; allowable operands vary from directive to directive.

.EVEN

The .EVEN directive ensures that the assembly location counter is even by adding one if it is odd. Any operands following a .EVEN directive will be ignored.

.END

The .END directive indicates the logical and physical end of the source program. The .END directive may be followed by only one operand, an expression indicating the program's entry point.

At load time, the object tape will be loaded and program execution will begin at the entry point indicated by the .END directive.

.WORD

The .WORD assembler directive may have one or more operands, separated by commas. Each operand is stored in a word of the object program. If there are more than one operand, they are stored in successive words. The operands may be any legally formed expressions. For example,

```
.=1420
.WORD 177535   ;STORED IN WORD LOCATIONS 1420, 1422, AND
.WORD 1426,0   ;1424 WILL BE 177535, 1426, AND 0.
```

.BYTE

The .BYTE assembler directive may have one or more operands separated by commas. Each operand is stored in a byte of the object pro-

gram. If multiple operands are specified, they are stored in successive bytes. The operands may be any legally formed expression with a result of 8 bits or less. For example,

```
SAM=5           ;STORED IN LOCATION 410 WILL BE
.=410           ;060 (THE OCTAL EQUIVALENT OF 48).
.BYTE 48.,SAM   ;IN 411 WILL BE 5.
```

.ASCII

The .ASCII directive translates strings of ASCII characters into their 7-bit ASCII codes with the exception of null, rubout, carriage return, line feed, and form feed. The text to be translated is delimited by a character at the beginning and the end of the text. The delimiting character may be any printing ASCII character except colon and equal sign and those used in the text string. The 7-bit ASCII code generated for each character will be stored in successive bytes of the object program. For example,

```
.=500           ;THE ASCII CODE FOR "Y" WILL BE
.ASCII /YES/    ;STORED IN 500, THE CODE FOR "E"
                ;IN 501, THE CODE FOR "S" IN 502.

.ASCII /5+3/2/  ;THE DELIMITING CHARACTER OCCURS
                ;AMONG THE OPERANDS. THE ASCII
                ;CODES FOR "5", "+", AND
                "3" ARE
                ;STORED IN BYTES 503, 504, AND
                ;505. 2/ IS NOT ASSEMBLED.
```

The ASCII directive must be terminated by a space or a tab.

APPENDIX E

SUMMARY OF EQUIPMENT SPECIFICATIONS & INDEX

The following table (starting on the next page) gives mechanical, environmental, and programming information for the equipment described in this Handbook. The equipment is arranged in alphanumeric order by Model Number. Page number references are made for more detailed information within the Handbook.

NOTES FOR THE TABLE

1. Mounting Codes

   CAB = Cabinet mounted. If a cabinet is included with the option, it is indicated by an X in the "Cab Incl" column.

   FS = Free standing unit. Height × Width × Depth dimensions are shown in inches.

   TT = Table top unit.

   PAN = Panel mounted. Front panel height is shown in inches. An included cabinet is indicated when applicable.

   SU = System Unit. SU mounting assembly is included with the option.

   SPC = Small Peripheral Controller. Option is a module that mounts in a quad module, SPC slot.

   MOD = Module. Height is single, double, or quad.

   ( ) = Option mounts in the same space as the equipment shown within the parentheses.

   Some options include 2 separate physical parts and are indicated by use of a plus (+) sign.

2. Cabinet and peripheral equipment (such as magnetic tape) are included in the specifications.
3. Relative humidity specifications mean without condensation.
4. Equipment that can supply current is indicated by parentheses ( ) around the number of amps in the POWER section.
5. Non-Processor Request devices are indicated by an X in the "NPR" column.

CONVERSION FACTORS

(inches) × 2.54 = (cm)

(lbs) × 0.454 = (kg)

(Watts) × 3.41 = (BTU/hr)

$[(°C) \times \frac{9}{5}] + 32 = (°F)$

		MECHANICAL				ENVIRON-MENTAL	
Model Number	Description	Mounting Code	Size (H x W x D)	Cab Incl	Weight	Oper Temp	Rel Humid
			(inches)		(lbs)	(°C)	(%)
AA11-D AD01-D AFC11	D/A Subsystem A/D Subsystem A/D Subsystem	SU PAN CAB	5¼			10-50 0-55 10-50	20-95 10-95 10-95
BA11-ES BA614 BB11	Mounting Box D/A Converter Blank Mntg Panel	PAN (AA11-D) SU	10½		100		
BC11A BM792-Y CD11-A	UNIBUS Cable Bootstrap Loader Card Reader	 SPC SU + TT	14 x 24 x 18		85	10-50	10-90
CD11-E CM11-F CR11	Card Reader Card Reader Card Reader	SU + TT SPC +TT SPC +TT	38 x 24 x 38 11 x 19 x 14 11 x 19 x 14		200 60 60	10-50 10-50 10-50	10-90 10-90 10-90
DA11-B DA11-F DB11-A	UNIBUS Link UNIBUS Window Bus Repeater	SU SU SU				5-50	10-95
DC11-A DD11 DF01-A	Asynch Line Inter Periph Mntg Panel Acoustic Coupler	SU SU TT	6 x 7 x 12		6	10-50 0-60	20-90
DF11 DH11 DJ11	Line Sig Cond Asynch Line MX Asynch Line MX	DF slot 2 SU SU				5-45	10-95
DL11-A DL11 DM11-BB	Terminal Control Asynch Line Inter Line Multiplexer	SPC SPC (DH11)					
DN11 DP11 DR11-B	Auto Calling Unit Synch Line Inter DMA Interface	SU SU SU				0-40 0-40 10-50	20-90 20-90 20-90
DR11-C DT03-F GT40	General Interface UNIBUS Switch Graphics Terminal	SPC PAN TT	5¼ 18 x 20 x 24		150	10-50 15-35	20-90 20-80
H312-A H720-E H722	Null Modem Power Supply Transformer	 (BA11) (PC11-A)			30	0-50	20-95
H742 H744 H745	Power Supply +5V Regulator −15V Regulator	(H960-D) (H742) (H742)					

POWER			PROGRAMMING		UNIBUS				
Cur needed/(supplied)		Power Dis	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	Page No.	Model Number
+5V	115 VAC/Other								
(amps)		(W)							
3	0.5	60	776 756	140,144	4,5		1	4-5	AA11-D
—	0.5	60	776 770	130	4 - 7		1	4-9	AD01-D
—	15	1700	772 570	134	4		1	4-13	AFC11
—	—						—	4-19	BA11-ES
	—						—	4-5	BA614
—	—						—	4-21	BB11
—	—						—	6-8	BC11A
0.3	—						1	4-22	BM792-Y
2.5	4	450	772 460	230	4	X	1	4-24	CD11-A
2.5	6	700	772 460	230	4	X	1	4-24	CD11-E
1.5	4	400	777 160	230	4		1	4-24	CM11-F
1.5	4	400	777 160	230	6		1	4-37	CR11
4	—			124	5	X	1	4-46	DA11-B
5	—			float	7	X	1	4-51	DA11-F
3.2	—						1 + 1	4-59	DB11-A
	—		774 000	float	5		1	4-60	DC11-A
—	—						—	4-68	DD11-A
—	0.3						—	4-72	DF01-A
	—						—	4-74	DF11
8.4	— 0.24A @ −15V		float	float		X	2	4-82	DH11
5	—		float	float			1	4-107	DJ11
1.8	— 0.15A @ −15V		777 560	060,064	4		1	4-233	DL11-A
1.8	— 0.15A @ −15V		776 500	float			1	4-124	DL11
2.8			775 000	float			1	4-82	DM11-BB
1.4	—		775 200	float	4		1	4-141	DN11
2.5	—		774 400	float			1	4-149	DP11
3.3	—		772 410	124	5	X	1	4-160	DR11-B
1.5	—		767 770	float	5		1	4-165	DR11C
	2			user	7		1 + 1	4-175	DT03-F
—	15	1500	float	float		X	1	4-179	GT40
—	—						—	4-185	H312-A
(22)	6 (10A) @ −15V	700					—	4-19	H720
—	— 1.5A @ 230VAC						—	4-259	H722
—	8 (1A) @ +15V						—	4-187	H742
(25)	—						—	4-187	H744
—	— (10A) @ −15V						—	4-187	H745

		MECHANICAL				ENVIRONMENTAL	
Model Number	Description	Mounting Code	Size (H x W x D)	Cab Incl	Weight	Oper Temp	Rel Humid
			(inches)		(lbs)	(°C)	(%)
H960-C	Cabinet	FS	72 x 21 x 30	X	120		
H960-D	Cab (1 drawer)	FS	72 x 21 x 30	X	300		
H960-E	Cab (2 drawers)	FS	72 x 21 x 30	X	470		
H961-A	Cab w/o side pan	FS	72 x 21 x 30	X	120		
KG11-A	Comm Arith Unit	SPC					
KW11-L	Line Clock	MOD	single ht				
KW11-P	Programmable Clock	SPC					
LA30	DECwriter	FS	31 x 21 x 24		110	15-35	20-80
LC11-A	LA30 Control	SPC					
LP11-F	Printer (80 col)	SPC + FS	46 x 24 x 22		200	10-43	15-80
LP11-J	Printer (132 col)	SPC + FS	46 x 48 x 25		575	10-43	15-80
LP11-R	Ptr (heavy duty)	SPC + FS	48 x 49 x 36		800	10-43	15-80
LPS11	Lab Periph System	PAN	5¼		80	5-43	20-80
LS11	Line Printer	SPC + TT	12 x 28 x 20		155	5-38	5-90
LT33	Teletype	FS	34 x 22 x 19		60	15-35	20-80
LV11	Electrostatic Ptr	SPC + FS	38 x 19 x 18		160	10-43	20-80
M105	Adrs Select Module	MOD	single ht				
M783	Bus Transmitter	MOD	single ht				
M784	Bus Receiver	MOD	single ht				
M785	Bus Transceiver	MOD	single ht				
M792	Diode ROM	SPC					
M795	Word Count	MOD					
M796	Bus Control	MOD					
M920	Bus Jumper	MOD					
M930	Bus Terminator	MOD	double ht				
M7820	Interrupt Control	MOD	single ht				
M7821	Interrupt Control	MOD	single ht				
ME11-L	Core Memory (8K)	PAN	5¼			0-50	10-90
MF11-L	Core Memory (8K)	2 SU				0-50	10-90
MM11-L	Core Memory (8K)	(MF11-L)				0-50	10-90
MR11-DB	Bootstrap	2 SPC					
MS11	Semiconductor Mem	(11/45)				0-50	10-80
PC11	Paper Tape	SPC + PAN	10½		50	13-38	20-95
PR11	Paper Tape (rdr)	SPC + PAN	10½		50	13-38	20-95
RC11-A	Disk & Control	PAN	10½		115	17-50	20-80
RF11-A	Disk & Control	PAN + PAN	16 + 16	X	500	17-33	20-55

POWER				PROGRAMMING		UNIBUS				
Cur needed/(supplied)			Power Dis	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	Page No.	Model Number
+5V	115 VAC	Other								
(amps)			(W)							
—			900					—	4-186	H960-C
(75)	8	(20A) @ −15V						—	4-186	H960-D
(150)	16	(40A) @ −15V	1800					—	4-186	H960-E
—								—	4-186	H961-A
1.5	—			770 700				1	4-188	KG11-A
0.8	—			777 546	100	6		1	4-197	KW11-L
1	—			772 540	104	6		1	4-198	KW11-P
—	3		300					—	4-201	LA30
1.5	—			777 560	060,064	4		1	4-201	LC11-A
1.5	2		250	777 514	200	4		1	4-208	LP11-F
1.5	4		500	777 514	200	4		1	4-208	LP11-J
1.5	17		2000	777 514	200	4		1	4-208	LP11-R
—	3		300	float	float	4 · 6	opt	2	4-218	LPS11-S
1.5	3		300	777 514	200	4		1	4-227	LS11
—	2		200					—	4-233	LT33
1.5	5		600	777 514	200	4		1	4-241	LV11
0.34	—								6-9	M105
0.2	—								6-11	M783
0.2	—								6-11	M784
0.3	—								6-13	M785
0.23	—			773 000				1	4-22	M792
	—								6-14	M795
	—								6-17	M796
	—								6-24	M920
1.25	—								6-24	M930
	—								6-25	M7820
	—								6-29	M7821
—	5		125					1	4-245	ME11-L
3.4	—	6A @ −15V	125					1	4-245	MF11-L
1.7	—	0.5A @ −15V	125					1	4-245	MM11-L
0.6	—							2	4-22	MR11-DB
	—			772 100	114			1	4-249	MS11
1.5	3		350	777 550	070,074	4		1	4-252	PC11
1.5	3		350	777 550	070	4		1	4-252	PR11
—	2.2		250	777 440	210	5	X	1	4-260	RC11-A
—	6.5		750	777 460	204	5	X	1	4-272	RF11-A

		MECHANICAL				ENVIRONMENTAL	
Model Number	Description	Mounting Code	Size (H x W x D)	Cab Incl	Weight	Oper Temp	Rel Humid
			(inches)		(lbs)	(C)	(%)
RK05	Disk Drive	PAN	10½		110	15-43	20-80
RK11-D	Disk & Control	SU + PAN	10½	X	250	15-43	20-80
RP03	Disk Drive	FS	40 x 30 x 24		415	15-33	10-80
RP11-C	Disk & Control	CAB + FS		X	740	15-33	10-80
RS11	Disk Drive	PAN	16		100	17-33	20-55
RS64	Disk	PAN	10½		65	17-50	20-80
TA11	Cassette	SPC + PAN	5¼			10-40	20-80
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250	15-27	40-60
TM11	Magtape & Control	PAN + PAN	26 + 10½	X	500	15-27	40-60
TU10	Magtape Transport	PAN	26	X	450	15-27	40-60
TU56	DECtape Transport	PAN	10½		80	15-27	40-60
UDC11	I/O Subsystem	CAB				5-50	10-90
VR01	Display	PAN	10½		30	10-50	10-90
VR14	Display	PAN	10½		75	10-50	10-90
VT01	Display	TT	12 x 12 x 23		50	0-50	10-80
VT05	Alphanum Terminal	TT	12 x 19 x 30		55	10-43	8-90

POWER			PROGRAMMING		UNIBUS				
Cur needed/(supplied)		Power Dis	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	Page No.	Model Number
+5V	115 VAC/Other								
(amps)		(W)							
—	2	160					—	4-282	RK05
7.5	2	200	777 400	220	5	X	1	4-282	RK11-D
—	— 6A @ 230VAC	1300					—	4-294	RF03
—	7 6A @ 230VAC	2100	776 710	254	5	X	1	4-294	RP11-C
—	2	200					—	4-272	RS11
—	2.2	250					—	4-260	RS64
1.5	1	120	777 500	260	6		1	4-304	TA11
—	9	870	777 340	214	6	X	1	4-309	TC11-G
—	9	1000	772 520	224	5	X	1	4-322	TM11
—	9	1000					—	4-322	TU10
—	3	350					—	4-309	TU56
—	15	1700	771 774	234	4,6		2	4-336	UDC11
	1	120					—	4-343	VR01
	4	400					—	4-344	VR14
	2.2	250					—	4-346	VT01
—	2	130					—	4-347	VT05

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